Recommended Practices for the use of VMEbus in Physics Applications

Draft 0.4
October 1,1995

This document has been prepared by the
ESONE/CERN VMEbus Steering Committee.
(Note that some parts of the document are marked as "under development". These parts should not be used to specify or claim conformance).

Contact:
C.Parkman
ECP Division
CERN - European Organisation for Nuclear Research
CH - 1211 Geneva 23

Tel. +41 22 767 3963
Fax. +41 22 767 5924
Email parkman@cern.ch
WWW http://www.cern.ch/ECP-ESS/VSC/VSC_Welcome.html

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Abstract

This document defines the use of optional features described in other specification documents and details a number of features specific to the use of VMEbus and related standards in physics applications.

Foreword

VMEbus has been very successful as a backplane bus standard for modular computer systems in industry at large as well as in physics research. However, in recent years this very popularity and consequent availability of numerous functions off-the-shelf from a very large number of suppliers, has engendered other more diverse applications. This expansion has lead to extensions to the basic standard by the responsible standards body, on a proprietary basis by manufacturers, and in in-house designs.

The proliferation of such extensions in "front-end" and other applications has been the subject of much debate in recent years. Preliminary recommendations on the use of VMEbus extensions were made to CERN management at the end of 1992, but during the course of 1993 it became evident that the subject warranted a more profound study and a wider discussion.

Discussions with physics groups, within management committees at CERN and contacts with other European laboratories via the committee for European Studies On Norms for Electronics (ESONE)[1] as well as with the VITA Standards Organisation (VSO)[2] culminated in a workshop held at CERN on March 15th 1994 attended by some 70 engineers and physicists, users, developers and suppliers of VMEbus equipment in physics.

This workshop concluded that there was a need to clarify the use of VMEbus and related standards in physics applications. The CERN VMEbus Steering Committee (VSC)[3] was mandated to continue its previous work and to ensure the widest possible consensus for the resulting recommendations within the physics community of manufacturers, suppliers and users.

In September 1994, the CERN VSC was co-opted by ESONE as a technical working group, and soon after co-founded the VMEbus International Physics Association (VIPA) with the North American NIM committee's VME-P working group and VITA.

Subsequently, another major meeting ("VMEbus in Physics '95), numerous local discussions and contacts with the NIM VME-P committee and colleagues in Japan have served to refine the technical recommendations.

This present document complements the relevant standards documents and provides the basis for a coherent approach to be taken by industry as well as design groups in relevant establishments to the supply of VMEbus equipment for use in physics data acquisition and controls applications.

1 ESONE - the committee for European Studies On Norms for Electronics, c/o P.Ponting, ECP Division, CERN, 1211 Geneva 23, Switzerland

2 VSO - VITA Standards Organisation, 10229, N.Scottsdale Road, Suite B, Scottsdale, AZ 85253, USA

3 VSC- CERN VMEbus Steering Committee. VSC convenor: C.Parkman, ECP Division, CERN. 121 Geneva 23, Switzerland, Email pmn@cernvm.cern.ch

Acknowledgements

This document has been prepared by the CERN VMEbus Steering Committee an internal body of the European Organisation for Nuclear Research (CERN) which is also a working group of the committee for European Standards On Norms for Electronics (ESONE) and forms part of the VMEbus International Physics Association (VIPA). Notwithstanding its collective origin, much of the contents are the result of individual efforts, from within the VSC and from other collaborators.

Any comments on the contents of the document or for general information should be directed to:

C. Parkman
CERN VSC Convenor
ECP Division
CERN
1211 Geneva 23
Switzerland
Tel. + 41 22 767 3963
Fax. + 41 22 767 5490
Email. parkman@cern.ch

This document is available via Internet on the WWW at URL:

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Contributors to this document

VSC: J.Buytaert, D.Kemp, M.Merkel, C.Parkman L.Pregernig, P.Ponting, R.Rausch (all from CERN)

Others include: M.Chorowicz (Creative Electronic Systems), J.Niewold (CERN), D.Notz, J.Pett (CERN) and U.Uhmeyer (LeCroy Corporation).

The Editor thanks to all those who have contributed by their constructive criticism.

Further information

World Wide Web

The ESONE/CERN VSC, in common with its associate organisations in VIPA, publishes relevant information on its activities via the Internet, World Wide Web.

The VSC “Welcome” page provides access to all this information:

http://www.cern.ch/ECP-ESS/VSC/VSC_Welcome.html

Other relevant information may be found on the VITA home page:

http://www.vita.com/

Chapter 1: Introduction

1.1 Objectives of the Recommended Practices

This document specifies an application dependent sub-set of options or "profile", which have been identified in the VMEbus family of specifications as applicable to the use of VMEbus in physics research. Designers and manufacturers of VMEbus equipment are encouraged to use this standard to take a consistent approach to the design and construction of such equipment for physics applications.

1.2 Document organisation

This document is organised as Chapters containing formal standardisation information, including rules and regulations, and a number of annexes which contain further specification as well as informative text, informal guidelines, etc.

1.3 References

The following publications are used in conjunction with this specification. When they are superseded by an approved revision, that revision shall apply.

Ref.	Specification	Origin	Referred to in this document as:
[1]	VITA-1 1995	VSO/ANSI VME64	**VME64**
[2]	VITA -1.1	VSO/ANSI VME64 Extensions (in preparation)	**VME64 Extensions**
[3]	VITA - 1.x	VSO/ANSI VME64 9U x 400mm Format (in preparation)	**VSO 9U**
[4]	IEEE 1101.1	IEEE Standard for Mechanical Core Specifications for Microcomputers using IEC603-2 Connectors	
[5]	IEEE 1101.10	IEEE Standard for additional Mechanical Specifications for Microcomputer using the IEEE 1101.1 Equipment Practice	
[6]	IEEE P1386.1	Physical and Environmental Layers for PCI Mezzanine Cards. April 1995 IEEE, Piscataway, New Jersey.	
[7]	VITA-4	IP Modules, Draft Standard VITA 4-, 1995. VITA, Phoenix, Arizona.	
[8]	PCI Local Bus Specification, Revision 2.0. April 1993.	PCI Special Interest Group, Hillsboro, Oregon.	
[9]	IEEE P1386.0	Proposed Standard for a Common Mezzanine Card Family." April 1995. IEEE, Piscataway, New Jersey.	
[10]	Specification for VMEbus Crate V430	CERN EP Test and Instrumentation Group, G.Bianchetti et al, 1990.	**CERN V430**

Chapter 2: Additional features

2.1 Introduction

This section describes and specifies features in the Recommended Practices which are additional to or which modify those specified in the VME64 and VME64 Extensions documents.

Two formats are specified, 6U and 9U. The 6U format conforms to the VME64 specification and defines the use of certain of the optional features described in the VME64 Extensions specifications. The 9U format follows the 6U specification but with dimensions conforming to the IEEE 1101.1 [4] specification, and with the optional addition of an extra, J3, connector. The 9U format is the subject of an ANSI/VITA draft standard [3].

The backplane connectors conform to the VME64 Extensions specification in all aspects as far as the J1/P1 and J2/P2 connectors are concerned. However the J0 space between J1/P1 and J2/P2, is occupied by an alternative to the J0/P0 described in known as Jaux ("aux" for "auxiliary").

It should be noted that the IEEE 1101.10 [5] keying mechanism is used to avoid incompatible combinations of modules and backplanes.

Note that the only mandatory requirement is that either the VME64 96 pin or the VME64 Extensions 160 pin connector be used (without one of which the module cannot comply to the VMEbus[4] specifications.)

Table 2.1 summarises the use and applicability of backplane connectors.

2.2 Autoslot ID

The VME64 Autoslot ID principle has been superseded by the inclusion of a "real" geographical address in VME64 Extensions as a means of assigning the CR/CSR base address of VMEbus boards.

> ***RULE 2.1***
> If an automatic means of setting the base address of a module's CR/CSR space is to be used, geographical addressing as described in the VME64 Extensions specification and in this document SHALL be used.

> ***OBSERVATION 2.1***
> Rule 2.1 implies that the VME64 Autoslot ID mechanism is not recommended.

2.3 Additional backplane power supplies

Although on-board power conversion may be used in many circumstances to provide non-VMEbus standard power supply voltages, it is very often convenient and cost-effective to draw power from the backplane. This document describes two such power supply requirements: for Emitter Coupled Logic (ECL), and for analogue circuits.

4 The generic term "VMEbus " is used in this document to indicate VME64 or VME64 Extensions as applicable in the context of the text.

2.3.1 ECL power

Power at -5.2V and -2V is supplied from the backplane via the Jaux/Paux connector specified in section 2.7.1. With a conservative current rating of 1.5A/pin, 9A is available at -5.2V and 4.5A at -2V (with a 30 pin Jaux).

2.3.2 Analogue power and reference

Backplane power supplies at ±15V ware specified which are primarily intended for analogue circuits. With a conservative current rating of 1.5A/pin, 1.5A is available at each of +15V and -15V (with a 30 pin Jaux).

The analogue reference is an unbussed pin intended for the direct connection of a transducer signal reference onto the module. The connection through the backplane is to be made in such a way as to minimise capacitive coupling with other signals and power supplies.

Refer to Chapter 8 for further specifications for an analogue environment.

2.4 Service signals

In front-end applications, it is often necessary to fan-out signals to different modules. For example: fast clear, common start/stop, ADC gate and common clock. The specified service signals provide a convenient mechanism to make these signals available without the need for extra cabling. Differential ECL has been chosen to minimise switching noise.

Three differential ECL service signals, CK/CK*, SG/SG* and CL/CL* are specified for use in applications when common signals have to be sent to all front-end modules (e.g. Clock, Gate, Clear).

The negative "*" signal has the ECL level -1.6 V when active and the positive signal has the ECL level -0.8 V when active.

> ***RULE 2.2***
> If a common clock. start/stop gate or clear signals are required in an implementation the service signals SHALL be used as specified in Table 2.4.

2.4.1 Electrical characteristics

The bussed service lines shall have a characteristic impedance of 100 Ω.

The terminations shall be done in such a way that when there are no drivers the voltage difference between the X* line DC voltage and the X line DC voltage is higher than 180 mV. Both lines shall have a 100Ω termination to -2V at both ends. A possible implementation is shown in Figure 2.1.

2.4.2 Drivers

Any ECL differential driver can be used to drive the Service Signal lines The distance between the driver and the connector has to be kept as short as possible and the capacitance presented to the bus should not exceed 12 pF.

The drivers shall be operated at -5.2 V within 5%. The specified output voltages when terminated into a 50 Ω load (which corresponds to 100Ω on the bus line terminated at both ends) to -2V are shown in Figure 2.1.

Additional features

Figure 2.1 Service line backplane termination

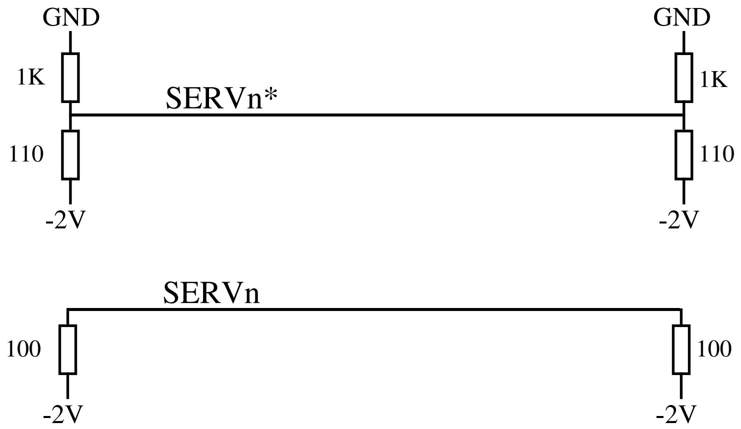


Table 2.1 Service signal logic levels

Output	Logic level	Voltage
high	1	-1V min., -0.7V max.
low	0	-1.6V max.

Pull-down resistors are not necessary.

OBSERVATION 2.2
It is not intended to have more than one Service Signal driver in a crate.

2.4.3 Receivers

Any ECL differential receivers with an input sensitivity of 150 mV peak to peak can be used. The receivers should be located as close as possible to the connector and the capacitance presented to the bus should not exceed 12 pF.

2.5 Large format VMEbus ("9U")

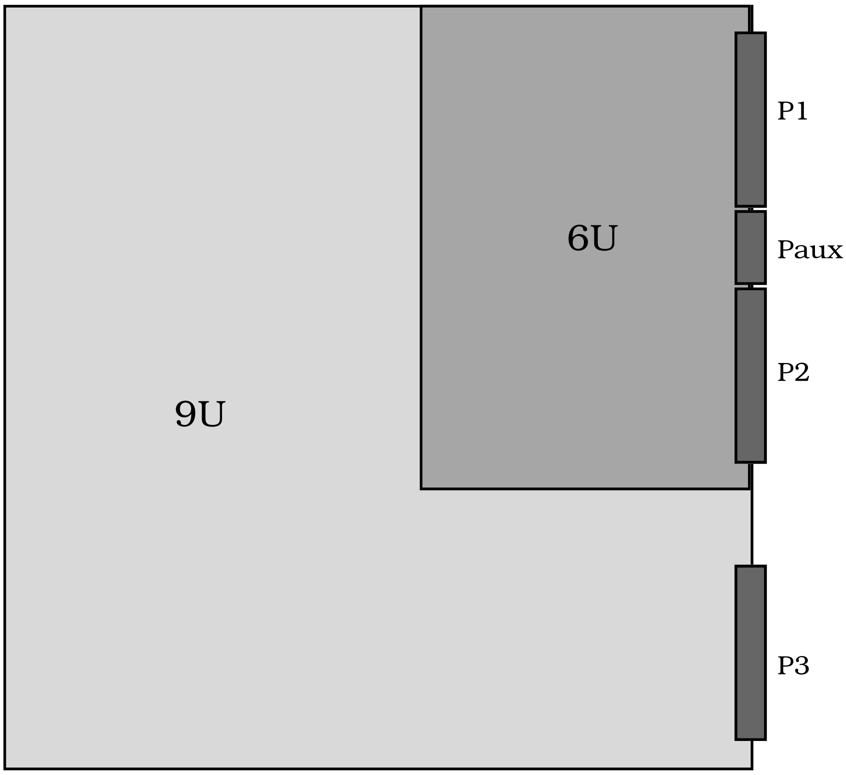
The dimensions, connector and front-panel positions, etc. are fully described in [3] and [4].

The choice of position relative to P1 and P2 of the additional P3 connector (above P1, or below P3) has been made to ensure a maximum of commonality with the market for 9U modules already existing at the time that the choice was made, as well as with the choice made within the VSO [3] and in order to group the connectors carrying I/O signals (P2 rows a & c and P3) together.

RULE 2.3
9U modules SHALL have the layout shown in Figure 2.2.

RULE 2.4
The dimensions of a 9U format module SHALL be specified according to VSO 9U [3] and IEEE 1101.1, IEEE Standard for Mechanical Core Specifications for Microcomputers using IEC603-2 Connectors [4].

Figure 2.2 6U and 9U module layout



2.6 J1/P1 and J2/P2 connectors

This document allows the use of either the VME64 96 pin or the VME64 Extensions 160 pin connectors for the J1/P1 and J2/P2 positions. The 96 pin connectors may be used for economy or other implementation dependent reasons at the expense of the availability of the full functionality of VME64 Extensions.

Table 2.2 Connector summary

Space	Connector	Specification	Status	Comment
J1/P1	96 or 160 pin	VME64 / VME64 Extensions	J1/P1 mandatory	Minimum sub-set for VME64 compliance, geographical addressing
J0	30 pin (42 pin under development)	Recommended Practices	Jaux/Paux optional	ECL and analogue power, bussed service signals
J2/P2	96 or 160 pin	VME64 / VME64 Extensions	J2/P2 optional	VME64 32 bit address/data extension, User defined input/output
J4	-	VSO 9U	J4 not recommended	-
J3/P3	96 or 160 pin recommended (others allowed)	Recommended Practices	J3/P3 optional	User defined input/output

Additional features

2.7 Jaux connector

This section describes an optional 30 pin (3x10) Jaux/Paux connector, based on and backwards compatible to the CERN-developed Jaux/Paux [10], but with improved signal specification, and with VME64 Extensions compliant Geographical Address (Slot Number), which is also available on the VME64 Extensions 160 pin, J1/P1 connector.

Any implementation using the 30 pin Jaux/Paux will be incompatible with a VME64 Extensions implementation whose 42 or 70 pin J0/P0 is specified for user defined input/output. It is therefore suggested that, whenever possible, the use of the Jaux be considered in the total system context, and that it should only be used when the use of its additional features cannot be avoided.

RECOMMENDATION 2.1
Whenever the current required by ECL or analogue circuits is of a sufficiently low value, power them from one of the VMEbus standard power supplies by means of on-board DC to DC converters.

OBSERVATION 2.3
The 30 pin Jaux/Paux specified in 2.7.1, below is mechanically and electrically incompatible with the J0/P0 specified in the VITA 1.1 VME64 Extensions document. Mechanical keying, as detailed in 2.6, below will prevent damage to incompatible assemblies of modules and backplanes.

OBSERVATION 2.4
Modules equipped with a 42 or 70 pin VME64 Extensions P0 will be incompatible with a backplane equipped with a 30 pin Jaux. Similarly, modules equipped with a 30 pin Paux will be incompatible with a 42 or 70 pin VME64 Extensions J0. Mechanical keying will be used to ensure that incompatible assemblies are not attempted.

Table 2.3 Comparison between CERN V430 and Recommended Practices Jaux/Paux

Feature	V430	Recommended Practices
Geographical addressing	SNn with positive logic	Geographical address as described for VME64 Extensions
Service signals	Differential or single-ended, differential termination with undefined values	Differential ECL with defined termination.

In addition to the 30 Jaux/Paux, an extension to 42 pins (3 x 14) is proposed, to allow compatibility with the VME64 Extensions document and to allow the additional functionality for a complete “3-row connector” solution. An extension to 70 pins (5 x 14) may also be developed, again in view of the VME64 Extensions proposals, if required.

2.7.1 Jaux/Paux connector pin assignments

RULE 2.5
If a 30 pin Jaux/Paux connector is implemented, its pin assignments SHALL be as described in Table 2.4.

Table 2.4 30 pin Jaux/Paux pin assignments

Pin no.	Row a	Row b	Row c
1	GA0*	GND	GA1*
2	GA2*	GND	GA3*
3	GA4*	GND	GND
4	CK*	GND	CK
5	SG*	GND	SG
6	CL*	GND	CL
7	-2V	-2V	-2V
8	-15V	AREF	+15V
9	-5.2V	-5.2V	-5.2V
10	-5.2V	-5.2V	-5.2V

RULE 2.6
If a 42 pin Jaux/Paux connector is implemented, its pin assignments SHALL be as described in Table 2.5.

Table 2.5 42 pin Jaux/Paux pin assignments

<<UNDER DEVELOPMENT>>

Pin no.	Row a	Row b	Row c
1	-48V	GND	+48V
2	-48V	RsvB	+48V
3	GA0*	GND	GA1*
4	GA2*	GND	GA3*
5	GA4*	GND	GND
6	CK*	GND	CK
7	SG*	GND	SG
8	CL*	GND	CL
9	-2V	-2V	-2V
10	-15V	AREF	+15V
11	-5.2V	-5.2V	-5.2V
12	-5.2V	-5.2V	-5.2V
13	-5.2V	-5.2V	-5.2V
14	-2V	GND	-2V

Table 2.6 Summary of Jaux signal definitions

Signal	Function	Notes
+15V, -15V	Analogue power	For general purpose analogue circuits
-5,2V, -2V	ECL power	
-48V, +48V	Bulk power	For high precision analogue circuits an non-standard voltages. Specified in VME64 Extensions
AREF	Analogue reference	Unbussed pins with low capacitive coupling
CK, CK*	Common clock	Bussed differential ECL
CL, CL*	Clear	Bussed differential ECL
GAn*	Geographical address	Hard-wired on backplane
RsvB	-	Reserved bussed line
SG, SG*	Start/stop gate	Bussed differential ECL

Additional features

OBSERVATION 2.5
The GAn* - Geographical Address - lines have opposite polarity to the CERN Jaux SNn lines [10], but the same polarity as the VME64 Extensions GAn* lines.

Table 2.7 Jaux Geographical Address pin assignments

Slot No	GA4*	GA3*	GA2*	GA1*	GA0*
1	Open	Open	Open	Open	GND
2	Open	Open	Open	GND	Open
3	Open	Open	Open	GND	GND
4	Open	Open	GND	Open	Open
5	Open	Open	GND	Open	GND
6	Open	Open	GND	GND	Open
7	Open	Open	GND	GND	GND
8	Open	GND	Open	Open	Open
9	Open	GND	Open	Open	GND
10	Open	GND	Open	GND	Open
11	Open	GND	Open	GND	GND
12	Open	GND	GND	Open	Open
13	Open	GND	GND	Open	GND
14	Open	GND	GND	GND	Open
15	Open	GND	GND	GND	GND
16	GND	Open	Open	Open	Open
17	GND	Open	Open	Open	GND
18	GND	Open	Open	GND	Open
19	GND	Open	Open	GND	GND
20	GND	Open	GND	Open	Open
21	GND	Open	GND	Open	GND

2.7.2 Jaux/Paux connector mechanical specification

The connectors for a 30 pin Jaux and Paux are defined in the CERN V430 document [10].

The connectors for a 42 pin Jaux and Paux are defined in the IEEE1101.10 [5] document.

2.7.3 Jaux/Paux connector position

The position of the 30 pin and proposed 42 pin Jaux/Paux connectors are defined in the CERN V430 [10] and IEEE1101.10 [5] documents, respectively.

2.8 J3 connector

An additional connector is placed below P2. This connector is known as J3/P3 and will normally be used exclusively for signal input/output. The J3 position in a chassis may be occupied by a backplane, may be left free for direct connections to modules or via a cable transition module. J3 may be a 96 pin or a 160 pin connector as defined in the VME64 [1] or VME64 Extensions [2] documents, if so, its preferred position is given in VSO 9U. Any other application-dependent connector,, is permitted

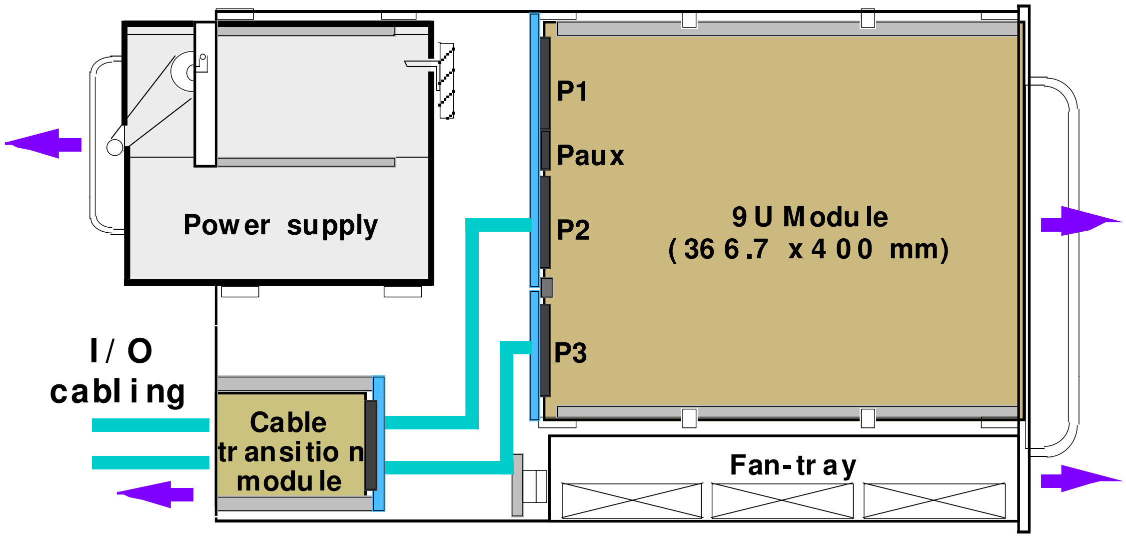
The sketch in Figure 2.3 shows a possible layout of connectors, backplanes and transition modules.

OBSERVATION 2.6
The VSO 9U specification alludes to 3U, 6U and 9U transition modules. Typical crate layouts with a rear-mounted power supply, as shown in Figure 2.3, will preclude transition modules with a height greater than 3U.

RECOMMENDATION 2.2
The J3/P3 position will normally be occupied by 96 pin or 160 pin connectors with the pin-out shown in Tables 2.8 and 2.9.

OBSERVATION 2.7
RECOMMENDATION 2.2 gives guidelines for the regular use of the J3/P3 position. In many instances other connectors (e.g. for optical connectors, etc.) will be required in an application dependent manner.

Figure 2.3 Typical 9U)chassis - schematic layout



If the connectors quoted in RECOMMENDATION 2.2 are used they will normally be mounted in a backplane whose dimensions are given in [4]. Since all the pins in J3/P3 are user definable, certain pins may be bussed to provide power to cable transition modules, or transmitted from a “mother” (9U) module

2.9 J4 connector

The VSO 9U specification describes the possibility of placing an additional connector in the space between J2/P2 and J3/P3 in a similar manner to J0/P0, known as J4. However, given the implications on backplane manufacture and connector insertion force as well as the difficulty of mounting a complete J1, J0, J2, J4, J3 backplane in a chassis, this possibility is not recommended.

RECOMMENDATION 2.3
The implementation of a J4/P4 connector between J2/P2 and J3/P3 is NOT RECOMMENDED.

RECOMMENDATION 2.4
For single-ended connections, connect the UDn- pin in Table 2.9 to ground.

Additional features

2.10 Mechanical keying

<<UNDER DEVELOPMENT>>

Within the broad framework of VME64 and its extensions mutually exclusive subsets can occur, particularly with respect to connectors and contact assignments. One method of ensuring both device protection and correct operation within a specific environment is to employ mechanical keying.

The keying patterns employed in this section permit the presence or absence of the Jaux connector to be detected and also provide an indication that operation within the VIPA environment can be sustained.

RULE 2.7
If implemented, programmed keying of modules and subracks SHALL be as (currently) specified in IEEE P 1101.10 [5].

RULE 2.8
Subrack keys E, positions 1 and 2, and F, position 1, SHALL be assigned as VIPA primary keying patterns.

RULE 2.9
Primary keying patterns SHALL be permanently installed in modules.
Primary keying patterns in subracks SHALL define the currently installed facilities.

RECOMMENDATION 2.5
Subrack key E, position 1, indicates the presence of the 30-pin Jaux connector as defined in Table 2.4.
Subrack key E, position 2, indicates the absence of the 30-pin Jaux connector as defined in Table 2.4.
Module key E, position 3, indicates the need for some feature of the 30-pin Jaux connector as defined in Table 2.4

RECOMMENDATION 2.6
Subrack key F, position 1, and module key F, position 3, defines the VIPA general environment key pattern.

OBSERVATION 2.8
When RECOMMENDATIONS 2.5 and 2.6 are implemented no other combinations of positions of keys E and F are possible.

OBSERVATION 2.9
Modules or subracks without keying facilities will retain full insertion capability and care must be taken in their use.

Table 2.8 Recommended J3/P3 pin assignments (160 pin connector)

Pin no	Row z	Row a	Row b	Row c	Row d
1	UD	UD	UD	UD	UD
2	UD	UD	UD	UD	UD
3	UD	UD	UD	UD	UD
4	UD	UD	UD	UD	UD
5	UD	UD	UD	UD	UD
6	UD	UD	UD	UD	UD
7	UD	UD	UD	UD	UD
8	UD	UD	UD	UD	UD
9	UD	UD	UD	UD	UD
10	UD	UD	UD	UD	UD
11	UD	UD	UD	UD	UD
12	UD	UD	UD	UD	UD
13	UD	UD	UD	UD	UD
14	UD	UD	UD	UD	UD
15	UD	UD	UD	UD	UD
16	UD	UD	UD	UD	UD
17	UD	UD	UD	UD	UD
18	UD	UD	UD	UD	UD
19	UD	UD	UD	UD	UD
20	UD	UD	UD	UD	UD
21	UD	UD	UD	UD	UD
22	UD	UD	UD	UD	UD
23	UD	UD	UD	UD	UD
24	UD	UD	UD	UD	UD
25	UD	UD	UD	UD	UD
26	UD	UD	UD	UD	UD
27	UD	UD	UD	UD	UD
28	UD	UD	UD	UD	UD
29	UD	UD	UD	UD	UD
30	UD	UD	UD	UD	UD
31	UD	UD	UD	UD	UD
32	UD	UD	UD	UD	UD

Table 2.9 Recommended J3/P3 pin assignments for twisted pair connections (160 pin connector)

Pin no	Row z	Row a	Row b	Row c	Row d
1	UD48+	UD00+	UD16+	UD32+	UD64+
2	UD48-	UD00-	UD16-	UD32-	UD64-
3	UD49+	UD01+	UD17+	UD33+	UD65+
4	UD49-	UD01-	UD17-	UD33-	UD65-
5	UD50+	UD02+	UD18+	UD34+	UD66+
6	UD50-	UD02-	UD18-	UD34-	UD66-
7	UD51+	UD03+	UD19+	UD35+	UD67+
8	UD51-	UD03-	UD19-	UD35-	UD67-
9	UD52+	UD04+	UD20+	UD36+	UD68+
10	UD52-	UD04-	UD20-	UD36-	UD68-
11	UD53+	UD05+	UD21+	UD37+	UD69+
12	UD53-	UD05-	UD21-	UD37-	UD69-
13	UD54+	UD06+	UD22+	UD38+	UD70+
14	UD54-	UD06-	UD22-	UD38-	UD70-
15	UD55+	UD07+	UD23+	UD39+	UD71+
16	UD55-	UD07-	UD23-	UD39-	UD71-
17	UD56+	UD08+	UD24+	UD40+	UD72+
18	UD56-	UD08-	UD24-	UD40-	UD72-
19	UD57+	UD09+	UD25+	UD41+	UD73+
20	UD57-	UD09-	UD25-	UD41-	UD73-
21	UD58+	UD10+	UD26+	UD42+	UD74+
22	UD58-	UD10-	UD26-	UD42-	UD74-
23	UD59+	UD11+	UD27+	UD43+	UD75+
24	UD59-	UD11-	UD27-	UD43-	UD75-
25	UD60+	UD12+	UD28+	UD44+	UD76+
26	UD60-	UD12-	UD28-	UD44-	UD76-
27	UD61+	UD13+	UD29+	UD45+	UD77+
28	UD61-	UD13-	UD29-	UD45-	UD77-
29	UD62+	UD14+	UD30+	UD46+	UD78+
30	UD62-	UD14-	UD30-	UD46-	UD78-
31	UD63+	UD15+	UD31+	UD47+	UD79+
32	UD63-	UD15-	UD31-	UD47-	UD79-

Chapter 3: Chained Block Transfers - CBLT

3.1 Introduction

The Chained Block Transfer (CBLT) mechanism allows the fast readout of large blocks of data of undetermined size from a series of modules housed in the same crate. At the start of a CBLT transaction the master has no knowledge of which of the slave modules contains data nor the size of the data.

All aspects of the CBLT mechanism including the readout of each module, the chaining, the end of transfer and exceptions are handled by a VME64 compliant mechanism requiring no specific features in the bus master, no additional backplane resources and which places no restriction on the use of VMEbus.

Note that slaves must have a minimum A32 capability.

Use of the CBLT mechanism will have the greatest effect on read-out performance when data is “sparse” that is when modules tend to contain little or no data. When consistently large blocks of data are read, the effect will be minimal.

3.2 Cycle identification

The eight most significant bits of an A32 address field (CBLT ADRS) signal a CBLT transaction (with the AM code defining the D32 or D64 transfer size) which will be recognised by all participating readout modules. The 23 low order bits are not significant.

All CBLT participating modules respond to the same value in bits A31-A24, the only restriction being that this address must be different to the address used to initialise the module.

RULE 3.1
CBLT readout SHALL be conditioned by the CBLTENB/CBLTDIS control bits (see Table 5.5)

RULE 3.2
Every CBLT readout module SHALL have a CBLT address register Read/Write accessible from the VMEbus, as shown in Table 3.1.

Table 3.1 CBLT Address Register

A31.............. A24	**A23...A01**
CBLT ADRS	Not significant

OBSERVATION 3.1
Since CBLT transactions are standard BLT or MBLT, the AM codes used will be 0F, 0C, 0B and 08.

RULE 3.3
Bits A23-A01 of the CBLT ADRS SHALL be user defined.

RECOMMENDATION 3.1
Use bits A23-A01 in CBLT ADRS to select a specific EVENT in a multi-event buffer.

3.3 Token mechanism

The VMEbus IACKIN*/IACKOUT* daisy chain is used to pass a token from one module to the next as each finishes its contribution to the data readout.

The first module in a CBLT chain is denoted by the setting the FIRST bit in its CSR space, and the last module by setting the LAST bit.

A certain number of regulations are required to ensure correct timing and for inter-operability with VMEbus interrupters.

> ***RULE 3.4***
> All slave modules concerned with CBLT readout SHALL be electrically contiguous on the VMEbus backplane.
>
> ***OBSERVATION 3.2***
> RULE 3.4 implies either that CBLT modules will be in contiguous slots, or the IACKIN*/IACKOUT* daisy-chain must be hardwired across any intervening slots.
>
> ***RULE 3.5***
> No non-CBLT VMEbus interrupters SHALL be inserted within a chain of CBLT modules.
>
> ***OBSERVATION 3.3***
> The timing rules given in Figure 3.1 are derived with the assumption that no modules which perform any treatment on the IACKIN*/IACKOUT* daisy-chain are installed within a chain of CBLT modules.
>
> ***RULE 3.6***
> When in a CBLT cycle, the LAST module in the CBLT chain SHALL NOT assert its IACKOUT* line.
>
> ***OBSERVATION 3.4***
> Rule 3.6 serves to protect down-stream VMEbus interrupters which may misbehave if they detect the assertion of IACKIN* while not in an interrupt acknowledge cycle.
>
> ***RULE 3.7***
> If its IACKIN* line is deasserted, a CBLT module SHALL NOT respond to a data transfer cycle and it SHALL NOT drive the data bus nor assert DTACK* or BERR*.
>
> ***RULE 3.8***
> The module configured as the FIRST in the CBLT chain SHALL NOT wait for IACKIN* low to assume the token.
>
> ***OBSERVATION 3.5***
> CBLT transactions observe VME64 timing rules which guarantee a minimum time between the assertion of the DSn* lines and the assertion of DTACK*. They also guarantee that the IACKIN* line is stable (high) when the CBLT transaction starts.
>
> ***RULE 3.9***
> When a module assuming the token is transferring its last data word, it SHALL NOT assert its IACKOUT* line low until both DSn* lines have been deasserted for that data transfer.

OBSERVATION 3.6
The token is received by the next module when IACKIN* is asserted which can occur before or after the DSn* lines are asserted.

OBSERVATION 3.7
When AS* is deasserted at the end of the cycle, each module deasserts its IACKOUT* line according to VME64 rules for interrupt acknowledge cycles. Thus CBLT transactions are compatible with VME64 interrupt acknowledge cycles.

3.4 Readout mechanism - the general case

The CBLT mechanism is specified for both D32 and D64 transfers. Certain optimisation of data transfers may be achieved by the suppression of readout from empty modules, with the CBLT token being passed without delay to the next participating module.

To start a CBLT transaction, the master asserts the specified address on the A31-A01 lines, the DSn* and the AS* lines, according to the VME64 specification. If the module configured as the FIRST in the CBLT chain is not PURGED, it provides DATA and DTACK* until it has transferred all of its data (and then becomes PURGED). It then asserts its IACKOUT* line after the deassertion of both DSn* line for the last data transfer to pass the token to the next module in the chain.

On the next assertion of DSn* lines this module will detect IACKIN* asserted and continue the data transfer.

If the FIRST module is PURGED it asserts its IACKOUT* line as soon as AS* and DSn* are asserted for a CBLT transaction. The next module detects that IACKIN* is asserted and continue with the data transfer.

This module if not PURGED provides DATA and DTACK* until it is PURGED. When it is PURGED it asserts IACKOUT* following the deassertion of DSn* for the last valid data in order to pass the token to the next module in the chain. On the next assertion of DSn*, this next module will detect IACKIN* asserted and continue the data transfer.

The LAST module in the chain does not assert IACKOUT*, but will transfer all its data and will terminate a transfer by asserting BERR* on the data phase following the last valid transfer (DTACK* assertion).

3.4.1 D64 readout

A D64 transfer starts with an address phase followed by one or more data phases. This section defines a mechanism to acknowledge the address phase whilst all CBLT modules wait for the data phase before starting to transfer data as specified for the D32 case.

RULE 3.10
During a D64 transaction, only the LAST module SHALL acknowledge the address phase.

RULE 3.11
All D64 CBLT modules SHALL wait for the data phase to start the token mechanism.

Chained block transfers

3.4.2 Data structure

RULE 3.12
CBLT slave modules SHALL supply data blocks structured as given in Table 3.2 for D32 and Table 3.3 for D64 transactions.

OBSERVATION 3.8
The minimum transfer count for D32 transactions is 8 bytes, and 16_{10} bytes for D64.

Table 3.2 CBLT D32 transactions

D32 ..... D27	**D26 . D24**	**D23 .... D16**	**D15 .... D00**
GEO	xxx	xxxxxxxx	xxxxxxxxxxxxxxxx
First Data			
Last Data			
GEO	Status	Transfer Count (bytes)	

Table 3.3 CBLT D64 transactions

D63-D59	**D58 .D56**	**D55 . D48**	**D47 .... D32**	**D31 .... D00**
GEO	xxx	xxxxxxxx	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Data Word 1				Data Word 2
Data Word n-1				Data Word n (last)
GEO	Status	xxxxxxxxxxxxxxxxxxxxxxxx		Transfer Count (bytes)

OBSERVATION 3.9
The transfer count field described in Tables 3.2 and 3.3 refers to the number of bytes actually transferred on the VMEbus. The meaningful data within the data may be less, and if so this count should be defined within the data structure.

3.4.3 Data structure field assignments

3.4.3.1 The GEO field

The GEO field (see Tables 3.2 and 3.3) contains a 5 bit value unique on any one backplane. This value will be derived from the module’s geographic address, from a register, or from on-board switches.

RULE 3.13
The GEO field SHALL contain a unique value for each module in one readout chain.

RULE 3.14
The module’s geographical address SHALL be used for the GEO field.

3.4.3.2 Transfer count

The Transfer Count is a 24 or 32-bit field containing the number of data bytes which have been readout from the module including the data frame information.

> ***RULE 3.15***
> Every CBLT module SHALL supply a transfer count corresponding to the number of bytes that have been readout from the module (this values includes the frame delimiters).
>
> ***OBSERVATION 3.10***
> The maximum data which can be transferred in one CBLT transaction for a D32 slave is 16 Mbyte and 4 Gbyte for a D64 slave.
>
> ***OBSERVATION 3.11***
> The CBLT protocol is designed to allow the efficient transfer of large blocks of data from a number of slaves on one backplane. The VME64 specification does not permit unbroken transfers of more than 256 cycles. Thus the implementation of CBLT should allow for the blocks to be broken in to VME64 compliant sub-blocks.

Editor's note:
With reference to OBSERVATION 3.11. The ESONE/CERN VSC asked for a derogation on this point in the VME64 specification to allow infinitely long block transfers in HEP front-end crates, where typically there is only one master with a large number of slaves, all involved in the same readout process. In this case the reason for the VME64 block-length limitations (bus arbitration latency) is not applicable. The VSC's request was not accepted.

3.4.3.3 Status

A 3-bit field reporting the status of the transferred data block.

> ***RULE 3.16z***
> The status field in described in Tables 3.2 and 3.3 SHALL contain a value as defined in Table 3.4

Table 3.4 CBLT Status return values

Status value	Meaning
0	Normal completion
1	Transfer ENDED (see section 3.5)
2	User defined status
3	User defined status
4	User defined error
5	User defined error
6	User defined error
7	User defined error

3.4.4 Empty modules

An empty module which chooses not to participate in a CBLT transaction can considerably decrease the overhead in both the readout and the subsequent software reconstruction.

Chained block transfers

PERMISSION 3.1
An EMPTY module may or may not choose to supply data in a CBLT transaction.

RULE 3.17
If an EMPTY module supplies data in a CBLT transaction it SHALL follow the data structure defined in Tables 16 or 17.

RULE 3.18
If an EMPTY module does not supply data in a CBLT transaction, then unless it is the LAST module in the CBLT chain, it SHALL only pass the token to the next module. It SHALL NOT drive the data bus, nor SHALL it assert DTACK*.

RULE 3.19
The LAST module SHALL supply data even if EMPTY as given in Tables 3.5 and 3.6.

OBSERVATION 3.12
Rule 3.19 ensures that the LAST module will terminate the transaction with the assertion of BERR* after providing a correct status field with an ENDED code.

Table 3.5 CBLT D32 empty transaction

D32 ..... D27	D26 . D24	D23 .... D16	D15 .... D00
GEO	xxx	xxxxxxxx	xxxxxxxxxxxxxxxx
GEO	Status	Transfer Count = 8_{10}	

Table 3.6 CBLT D64 empty transaction

D63-D59	D58 . D56	D55 .D48	D47........... D32	D31 .... D00
GEO	xxx	xxxxxxxx	xxxxxxxxxxxxxxxx	0
GEO	Status	xxxxxxxxxxxxxxxxxxxxxxxx		Transfer Count = 16_{10}

3.5 End of CBLT transaction

The CBLT makes a special use of the VMEbus BERR* to terminate the transfer.

The end of transfer occurs at the initiative of the slave when the token reaches the LAST module of the CBLT chain and this module has transferred its final data word. The slave then drives the BERR* line to signal the master to terminate the cycle.

The end of transfer should not be confused with an end of cycle which can occur at the master's initiative. The master aborts the cycle because it needs to regenerate the address or because the transfer size exceeds that permitted by VME64.

RULE 3.20
The LAST module in the chain SHALL terminate the CBLT transfer by asserting BERR* on the data phase following the termination of last valid data transfer by the assertion of DTACK*.

RULE 3.21
During a CBLT cycle BERR* SHALL only be used to terminate the transaction.

OBSERVATION 3.13
Rule 5.2 implies that only the LAST module is allowed to assert BERR* and only for the purpose of terminating the transfer when all of the data has been read-out.
A CBLT module will use the 3-bit status field to signal an internal error condition on the final data transfer.

The LAST module sets the status code to 1 inside the data structure when giving out its last data, to signal that it will assert BERR* on the next data phase. This is intended to enable the software to check for the correct end of transfer after BERR* is received rather than to be used by the VMEbus master to stop the transfer.

RULE 3.22
The master SHALL continues the CBLT transfer until it detects the assertion of BERR*.

It is always possible that a BERR* is generated during a CBLT transaction by the bus timer (BTO). All CBLT modules therefore must monitor BERR* and the CBLT address in order to detect the end of the transaction. Only when the assertion of BERR* is detected at the CBLT address is the transfer completed. When all CBLT modules may take the action necessary to acquire a new event. A BERR* at an address other than the CBLT address is possible and should not be confused with an end of CBLT transfer.

3.6 CSR space requirements

Every CBLT and MCST module requires a number of CSR resources. These are summarised in Chapter 5 and specified in detail below.

3.6.1 Regulations concerning CSR status bit handling

Refer to ???

RULE 3.23
A CBLT module SHALL set its PURGED bit to 1 during the transfer of its last data word.

OBSERVATION 3.14
RULE 3.21 ensures that on the next cycle the master will receive coherent status from the module.

RULE 3.24
An EMPTY module shall set its PURGED bit only when it detects the assertion of IACKIN* (the CBLT token).

OBSERVATION 3.15
An EMPTY module that supplies data will set its PURGED bit only when it supplies the last data of its empty frame.

RULE 3.25
An EMPTY module that does not supply data SHALL set its PURGED bit only when it asserts its IACKOUT* line and when detects the assertion of the DSn* lines.

Chained block transfers

PERMISSION 3.2
A EMPTY module that does not supply data that detects the assertion of its IACKIN* line need not wait for the DSn* line to be asserted before asserting its IACKOUT*.

PERMISSION 3.3
The PURGED bit may be resettable by software in order to permit a re-read of the data, where this is feasible.

3.6.2 Events

In the context of data acquisition we define the notion of *event*. The treatment of an event (the reading-out data from modules following one or more physics triggers) is reflected in two CSR status bits EMPTY and PURGED.

3.7 Multiple CBLT transactions

The length of a data block may be greater than the maximum allowed by the VME64 specification. For this and any other reason, the readout of an event may need multiple CBLT cycles to complete.

The CSR PURGED bit allows the differentiation of multiple CBLT transactions for one event, as well as the signalling readout of a new event.

RULE 3.26
Once the PURGED bit is set, it SHALL NOT be cleared until the end of the CBLT cycle BERR* is detected (see section 3.5) is detected and the module receives a new event.

PERMISSION 3.4
The PURGED bit may be overwritten by software to allow a module to re-transmit the data of an event.

OBSERVATION 3.16
RULE 3.26 states the minimum conditions to clear the PURGED bit. There may be some additional conditions under software control and/or front-panel signalling in relation with the trigger system.

RULE 3.27
When a CBLT transfer starts, a non-purged module (PURGED=0) SHALL obey the IACKOUT* assertion rules defined for the token mechanism.

RULE 3.28
When a CBLT transfer starts, a purged module (PURGED bit =1) SHALL asserts its IACKOUT* line as soon it detects the start of the data phase. (See Figure 3.1).

OBSERVATION 3.17
Rule 3.28 allow the daisy chain propagation delay to be short-circuited at the start of the CBLT cycle to improve speed in case of multiple CBLT transactions.

3.8 Timing specifications

RULE 3.29
All timings SHALL be as specified in VME64 with the exception that the assertion of IACKOUT* SHALL NOT occur before the deassertion of DSn*.

OBSERVATION 3.18
RULE 3.29 implies that the T1 in figues 3.1 and 3.2 has a minimum value of zero.

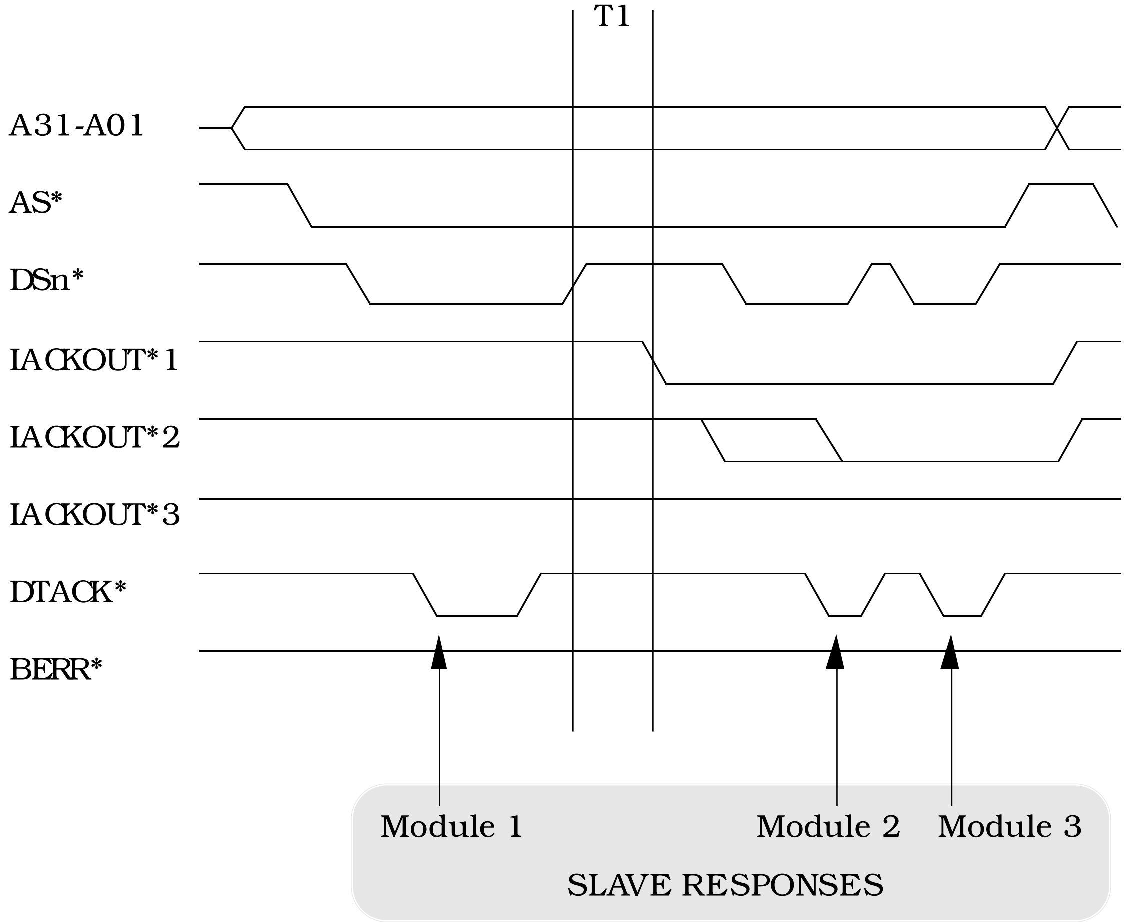


Figure 3.1 D32 CBLT timing

Chained block transfers

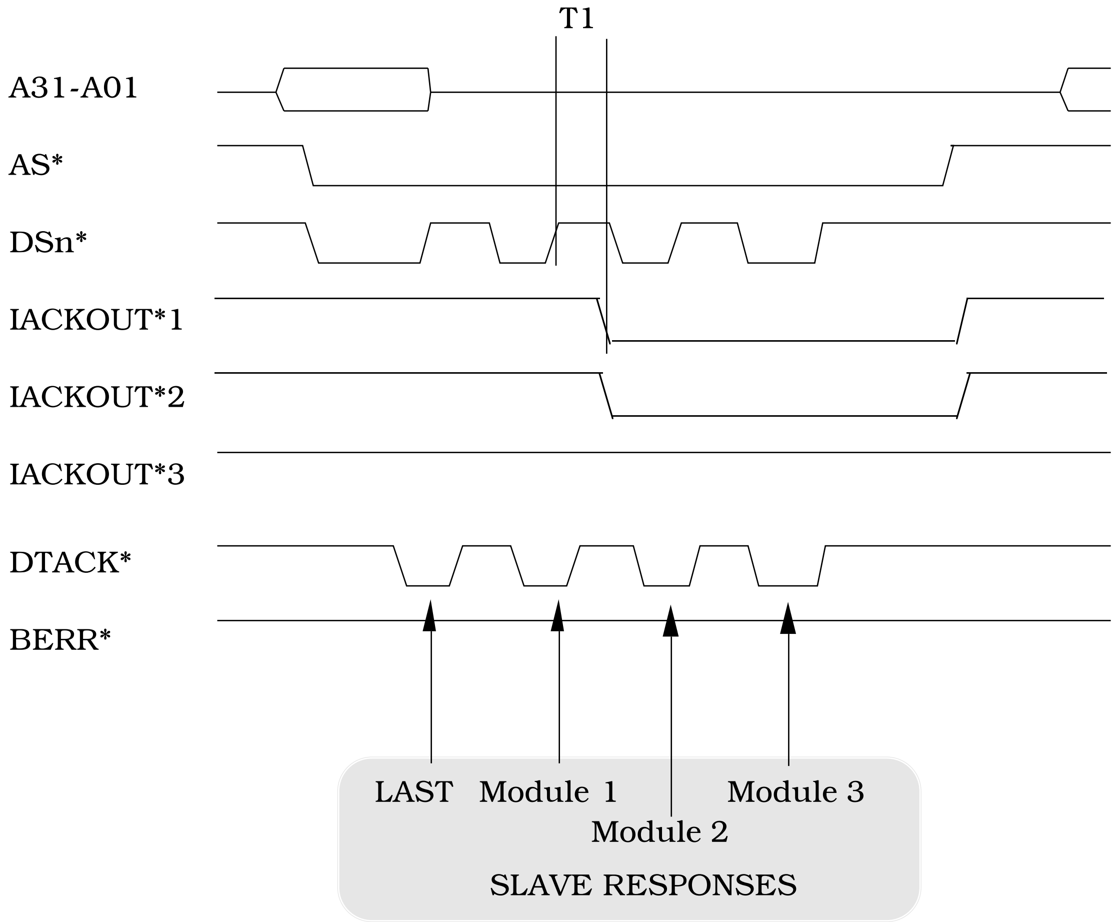


Figure 3.2 D64 CBLT timing

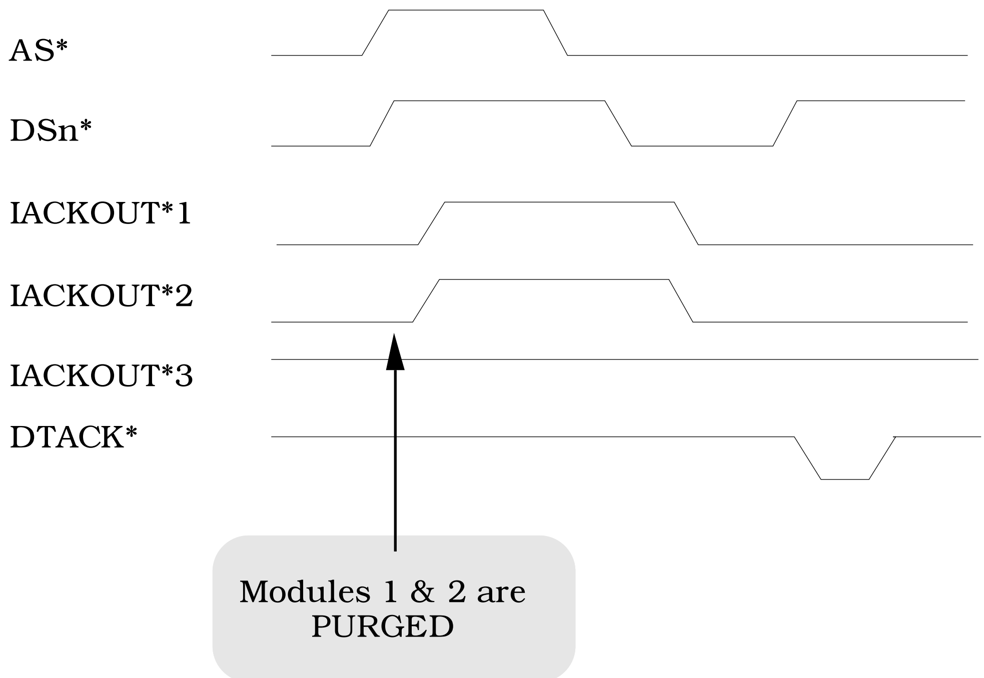


Figure 3.3 Multiple CBLT timing short cut

Chapter 4: Multicast commands - MCST

4.1 Introduction

In a data acquisition context it is often useful to define a global mechanism to give general commands such as *reset, fast clear, trigger ready, event selection,* etc. Multicast (MCST) transactions allow such commands to be sent to set of slave read-out modules in one DTB transaction and as such are essentially dataless write cycles. As for CBLT, all hardware mechanisms are implemented within the VMEbus slave so no non-standard features are required of a VMEbus master.

4.2 Cycle identification

The eight most significant bits of an A32 address field (MCST ADRS) signal a MCST transaction (with the AM code defining the D32 or D64 transfer size) which will be recognised by all participating modules. The 24 low order bits are not significant.

All MCST participating modules respond to the same value in A31-A24, the only restriction being that this address must be different from the address used to initialise the module.

RULE 4.1
CBLT readout SHALL be conditioned by the MCSTENB/MCSTDIS control bits (see Table5.5).

RULE 4.2
Every MCST readout module SHALL have a MSCT address register Read/Write accessible from the VMEbus, as shown below:

A31.............. A24	**A23...A01**
MCST ADRS	Not significant

RULE 4.3
Bits A23-A01 of the CBLT ADRS SHALL be user defined.

OBSERVATION 4.1
MCST transactions will use AM codes 0D or 09.

The CBLT mechanism of FIRST and LAST modules is used to acknowledge a multicast transaction and the IACKIN*/IACKOUT* daisy-chain is used to propagate the acknowledge from the FIRST module to LAST. Thus the same regulations defined for CBLT concerning electrical continuity, daisy-chain ordering, etc., apply to MCST transactions. The use of D64 transactions is not recommended since they are multiplexed and the use of one, single data phase inefficient.

Normally, software should not issue read cycles using the MCST address, however slaves modules should be protected against such an eventuality.

RULE 4.4
MCST read cycle shall be protected. If a read cycle directed to the MCST address is detected, all MSCT modules SHALL keep their VMEbus data drivers in 3-state. They SHALL NOT assert DTACK* nor BERR*.

Multicast commands

OBSERVATION 4.2
The LAST module may either drive BERR* or leave the cycle terminate with a BTO time-out.

Chapter 5: Configuration ROM and CSR space

5.1 Introduction

Since VMEbus in its IEEE1014-1987 and earlier forms lacks any system-level specification, individual manufacturers have each taken their own approach to the layout of the VMEbus address map, CSR space definition, etc. The VME64 specification includes a definition of a Configuration ROM and CSR space.

This chapter describes a number of optional extensions to the VME64 CR/CSR space, notably that required for CBLT and MCST transactions.

5.2 CR/CSR space

Modules need only supply the registers relevant to their implementation (e.g. no self-test status register and execute bit if self-test is not supported).

5.2.1 Configuration ROM

Table 5.1 Configuration ROM contents

Address	Content	Comments	Specification
0x03	Checksum		VME64
0x07, 0x0B, 0x0F	Length of ROM		VME64
0x13	Configuration ROM data access width		VME64
0x17	CSR data access width		VME64
0x1B	CR/CSR space specification ID		VME64
0x1F	0x43	ACSII “C”	VME64
0x23	0x52	ASCII “R”	VME64
0x27, 0x2B. 0x2F	Manufacturer’s ID	IEEE OUI	VME64
0x33, 0x37, 0x3B, 0x3F	Board ID		VME64
0x53, 0x57, 0x5B	Pointer		VME64
0x5F to 0x7B	Reserved		VME64
0x7F	Program ID code		VME64
0x83, 0x87, 0x8B, 0x8F	Serial number	4 bytes assigned by manufacturer	Rec. Practices
0x93, 0x97, 0x9B, 0x9F	Capabilities	4 bytes	Rec. Practices

Table 5.2 CR capabilities - bit assignments

Address 0x93

Bit	Name	Read
7	RSVD	0
6	RSVD	0
5	RSVD	0
4	RSVD	0
3	MCST	1 MCST capable 0 Not MCST capable
2	REREAD	1 CBLT PURGED bit may be cleared 0 CBLT may not be cleared
1	CBLT	1 CBLT capable 0 Not CBLT capable
0	STST	1 Self test capable 0 Not self-test capable

Addresses 0x97, 0x9B, 0x9F

Bit	Name	Read
7	RSVD	0
6	RSVD	0
5	RSVD	0
4	RSVD	0
3	RSVD	0
2	RSVD	0
1	RSVD	0
0	RSVD	0

5.2.2 Control and Status Registers

Table 5.3 Summary of CSR registers

Address	Content	Meaning
0x7FF7F	Self-test register	See Table 5.4
0x7FF7B	Self-test result register	0 - self-test completed successfully 1-255 - application dependent
0x7FF77	CBLT/MCST CSR1	See Table 5.5
0x7FF73	CSR2	See Table 5.6
0x7FF63 - 0x7FF6F	CBLT counter (4 bytes)	Actual transfer count in bytes
0x7FF5F	CBLT result register	0 - transfer completed successfully 1 - ENDED 2 - 255 - application dependent
0x7FF5B	CBLT ADRS	Most significant 8 bits of CBLT address register
0x7FF57	MCST ADRS	Most significant 8 bits of MCST address register
0x7FF53	CBLT geographic register	Least significant 5 bits (only if the geographical address is not available)

5.2.3 Self-Test Register

Table 5.4 Self-Test Register - bit assignments

Address 0x7FF7F

Bit	Name	Write	Read
7	RSVD	Reserved	0
6	RSVD	Reserved	0
5	RSVD	Reserved	0
4	RSVD	Reserved	0
3	RSVD	Reserved	0
2	RSVD	Reserved	0
1	RSVD	Reserved	0
0	STSTEXE	1 Execute self-test 0 No effect	1 Self test executing 0 Self-test not executing

RECOMMENDATION 5.1
Limit the time taken by self-test procedures to 2s maximum.

RULE 5.1
If the self-test fails the error number in the status register SHALL be set.

OBSERVATION 5.1
The “board has failed” indication specified in VITA 1 VME64 may be set whether the board has a software triggerable self-test or not. However self-test may or may not set the “board has failed” indication depending on the severity of the fault(s) detected.

5.2.4 CBLT/MCST Registers - CSR1

Table 5.5 CBLT/MCST CSR1 - bit assignment

Address 0x7FF77

Bit	Name	Write	Read
7	MCSTENB	1 Enable MCST 0 No effect	0
6	MCSTDIS	1 Disable MCST 0 No effect	1 MCST enabled 0 MCST disabled
5	FIRSTENB	1 Enable first module in a CBLT chain 0 No effect	0
4	FIRSTDIS	1 Disable first module in a CBLT chain 0 No effect	1 First module in a CBLT chain 0 Not first module in a CBLT chain
3	LASTENB	1 Enable last module in an CBLT chain 0 No effect	0
2	LASTDIS	1 Disable last module in an CBLT chain 0 No effect	1 Last module in a CBLT chain 0 Not last module in a CBLT chain
1	CBLTENB	1 Enable CBLT 0 No effect	0
0	CBLTDIS	1 Disable CBLT 0 No effect	1 CBLT enabled 0 CBLT disabled

Table 5.6 CBLT CSR2 - bit assignments

Address 0x7FF73

Bit No	CSR bit	Value	R/W	Meaning
7	RSVD	0		Reserved
6	RSVD	0		Reserved
5	RSVD	0		Reserved
4	RSVD	0		Reserved
3	RSVD	0		Reserved
2	ENDED	1	READ ONLY	The module is the last in a CBLT chain and has asserted BERR* to terminate the transfer
		0		The module is not the last in a CBLT chain, or the module is the last in a CBLT chain and has not asserted BERR* to terminated the transfer
1	EMPTY	1	READ ONLY	The module has no data for the event
		0		The module has data following the acquisition of an event
0	PURGED	1	R/W*	The module has received an event
		0	R/W*	All the modules data has been read out

* If the REREAD capability is supported writing "1" to the PURGED bit will clear purged whilst writing "0" will have no effect.

Chapter 6: Chassis, power supplies and cooling <<UNDER DEVELOPMENT>>

6.1 Introduction

Whilst there are many applications in physics for catalogue-standard chassis, power supplies and cooling systems (known collectively as “crates”) - typically in laboratory and office environments, in common with other similar applications in research and industry, there are many applications for rugged, high-reliability, modular systems.

Crates used in control and data acquisition applications are often placed in short-term inaccessible locations. This, and the frequent need for a large number of input/output cables, requires that the backplane and its housing (“card-cage” or “bin”) be able to be left undisturbed by repair or routine maintenance activity on the electrical and electro-mechanical parts of the crate (i.e. power supply and cooling).

6.2 Backplanes

- Automatic daisy-chaining.
- Monolithic construction

OBSERVATION 6.1
Modules equipped with the VME64 Extensions 160 pin connector, require that crates are equipped with compatible backplanes. Modules with 96 pin connectors may be used in crates equipped with either 96 pin or 160 pin connectors.

6.2.1 Termination

6.2.2 Power connection

6.2.3 Signal connectors

6.3 VSB

6.3.1 Daisy chain

6.3.2 Termination

6.3.3 Signal connectors

6.3.4 J3

6.4 Card-cage

6.4.1 Card guides

The VME64 specification with respect to card guide dimensions is followed (refer also to 6.7.1).

6.5 Power supply

6.6 Air cooling system

6.7 9U module mechanical considerations

6.7.1 Module thickness & stiffening

Based on FASTBUS experience, 9U x 400 mm modules need stiffening if unacceptable warpage is not to result even with careful manufacture. This stiffening is provided two ways: increased board thickness and mechanical stiffening.

6.7.1.1 Increased board thickness

IEEE1101.1 [4] specifies boards 1.6 mm thick whilst FASTBUS calls for a thickness of 2.36 mm. However for compatibility with VMEbus 3U and 6U boards, standard card guides, foreseen for 1.6 mm thick boards, are specified for (9U). Provision is made for reducing the thickness of (9U) boards at their edges.

> ***RULE 6.1***
> (9U) modules SHALL have a thickness of 2.4mm except for a distance of 2.5mm from the top and bottom edges (card-guide edges) where the thickness SHALL be reduced to 1.6 mm (see Figure 6.1).

6.7.1.2 Mechanical stiffening

Mechanical stiffeners are recommended to be used and may normally be placed in three places: near the VMEbus connectors and along each of the card-guide edges. These latter stiffeners should be manufactured in a manner so as not to impede the flow of cooling air and should respect the maximum component height specified in IEEE1101.1 [4]. See the VSO 9U specification.

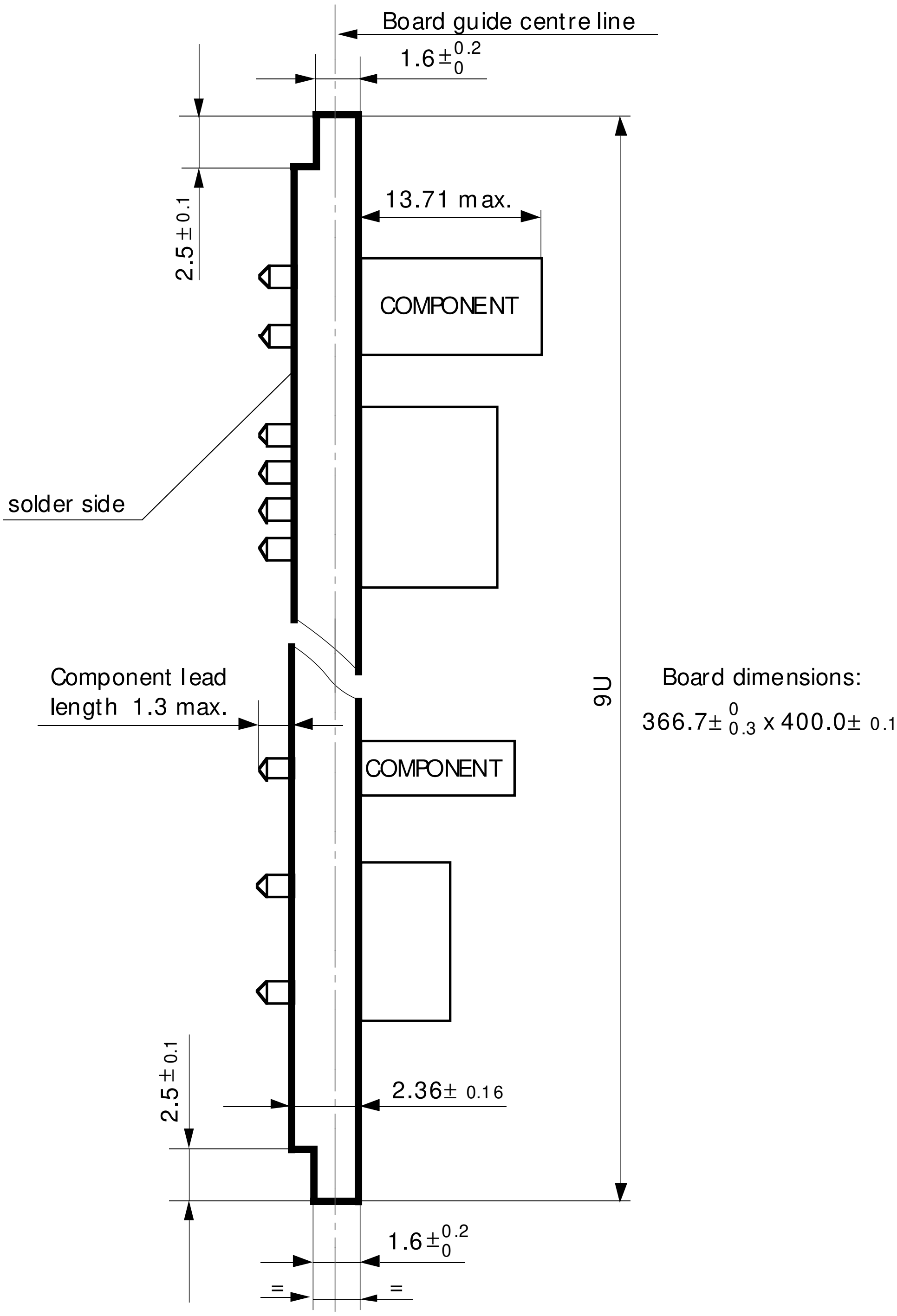


Figure 6.1 Cross-section of a (9U) module

Chapter 7: Front panel connectivity

7.1 Introduction

This chapter discusses the commonly used signal standards for front-panel interconnects and their application in physics.

Two different interconnection methods for digital signals are commonly used in physics instrumentation modules: NIM (Nuclear Instrument Module - a current switching standard) and ECL (Emitter Coupled Logic). These signalling standards are used in the vast majority of the front panel control and status signals of NIM, CAMAC and FASTBUS modules. To optimise connectivity it is recommended that modules retain this consistency. TTL (Transistor-Transistor Logic) interconnects are also discussed.

Differential ECL is the preferred method for digital signal interconnect, and requires less physical front panel space than NIM signals.

The one drawback to ECL is not the logic itself, but the commonly used cabling. The 110 ohm twisted pairs have a greater attenuation at high frequencies than co-axial cables. Although it is possible to interconnect single-ended ECL with coaxial cables, it is not recommended, since such cables are more commonly used for ground referenced signals such as NIM and analogue.

> ***RECOMMENDATION 7.1***
> Whenever possible, use differential ECL. For single-ended signals, NIM is an acceptable alternative.

7.2 ECL

7.2.1 Signalling and termination

ECL is a standard logic family with a variety of standard devices available for both single-ended and differential interconnection. ECL offers both a high degree of flexibility in interconnection methods as well as a very high fan-out capability. ECL outputs are open emitters which require resistive pull-downs for correct bias. Normally the driver requires a pull-down resistor of about 390 ohms to be connected to -5.2V, to properly bias the output transistor, making it into a low impedance voltage source, and also to sink the current necessary to develop 800 mV across the termination resistor. Note that 100 ohm pull-downs to -2V at the outputs of front panel ECL drivers will not be adequate to meet this requirement. ECL inputs are transistor bases and require only a few µA of bias in either the low or high states. They appear as a very high impedance with respect to the 100 ohm line impedance used for interconnections.

7.2.1.1 Differential signalling

Differential signalling is the preferred method for ECL interconnections since it provides a high degree of rejection of temperature and voltage variations, ensuring a good noise margin. The received signal is extracted based on the crossing of two signals from the same source and even if the amplitudes vary, or the noise between modules varies, the crossing of the differential signals maintains the correct threshold.

Differential ECL signalling should be used in all cases where timing is critical, such as for gating, triggering and fast clearing signals. In contrast, a single-ended ECL signal has the driver and receiver circuits in entirely different modules, each with separate thresholds. The single-ended interconnect may be acceptable for short digital interconnections within the same crate where exact timing or timing stability is not critical.

7.2.1.2 Signal termination

Some differential ECL line receivers (such as the 10114 and 10125 receivers/level translators) go to a defined state if their inputs are left unconnected. Differential ECL inputs will normally be provided with an input termination network compatible with twisted pair cables having a nominal 100 ohm characteristic impedance. This is most often achieved by connecting two 56 ohm resistors in series. The common point of the termination is decoupled to ground with a capacitor (0.01μF to 0.1μF) in order to provide a partial common mode termination to prevent high frequency ringing of the input signals.

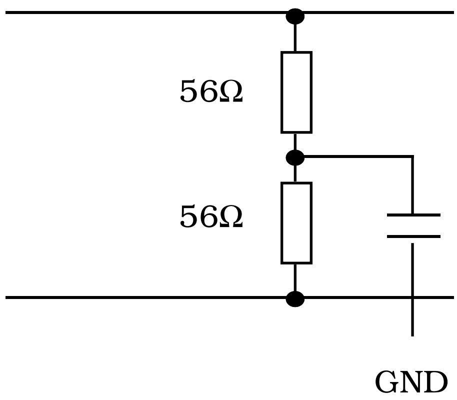


Figure 7.1 Differential ECL termination

RULE 7.1
Terminate differential ECL signals as shown in Figure 7.1.

RECOMMENDATION 7.2
In order to accommodate the bussing of a common gate or timing signal across several adjacent modules, make the ECL terminator removable.

OBSERVATION 7.1
The bussing of a common differential ECL signal across several modules is only possible if the transmission line stubs extending into the module are relatively short before they encounter their termination networks and line receivers.

OBSERVATION 7.2
For differential twisted pair signals entering a printed circuit board, the individual traces for each signal should run with an impedance of one half of the differential line impedance. In the nominal case, the 110 ohm cable should transition into 55 ohm transmission lines on the printed circuit and be terminated in 56 ohm to a voltage half way between Vhigh and Vlow, as achieved by the specified termination network. It is also customary to have the nominal 390 ohm output pull-down resistors removable for certain applications.

Front panel connectivity

7.2.1.3 OR'd signals

It is possible to use differential drivers in combination with single-ended receivers to provide a data bus across modules. Modules would normally stay off the bus by keeping their outputs in the logic "false" state. When a module's turn to drive the bus comes, it drives a logic "true" onto the bus. Since ECL has open emitter outputs, a logical "ORing"[5] of all logic "trues" is performed. Only the "+" outputs are looked at by a single-ended receiver.

In this example, only the driving module at the end of the line provides the pull-down resistors to -5.2V. All of the other driving modules have their removable pull-downs removed. The receiving module should be at end and terminate the line by tying the "-" input to ground and the "+" input via a 100 ohm resistor to -2V and will go to a single-ended input with a logic threshold equal to Vbb, nominally -1.3V.

7.2.2 Connectors

Insulation Displacement Connectors (IDC) mounted on the cables allow for either point to point or bussed interconnections since IDC connectors can be placed at points along the cable. Individual pairs are easily routed with 2 pin connectors which use only the 2.54 mm allowed for each pair on a dual row 2.54 x 2.54 mm header.

> ***RECOMMENDATION 7.3***
> Use dual row 2.54 x 2.54 mm headers and IDC connectors for differential ECL connections.

> ***RECOMMENDATION 7.4***
> Use 34 pin connections for 16 pairs of differential signals as shown in Table 7.1.

7.2.2.1 Suitable connectors

Printed circuit headers

Examples of printed circuit mount right angle headers that work well are:

4 pin	(2 pair)	DUPONT (BERG) 75789-101-04
6 pin	(3 pair)	DUPONT (BERG) 75789-101-06
20 pin	(10 pair)	DUPONT (BERG) 75789-101-20
34 pin	(17 pair)	DUPONT (BERG) 75789-101-34

These connectors are particularly suitable since the pins are higher above the board (approx. 3.8 mm) than conventional right-angle headers. This allows the mating connector in turn to be slightly higher above the board and prevents the exposure of the printed circuit board through the front panel cut-out.

5 See Annex ? for a description of the Wired-OR "Glitch".

Cable connectors

Examples of cable connectors that work well are:

2 pin	(1 pair)	BERG 65039-035 housing (requires BERG 47745 contacts)
34 pin	(17 pair)	3M 3414-6034

Cables

Examples of multi-conductor twisted pair cables that work well are:

Spectra-Strip 843-132-2801-nnn, where nnn is the number of conductors from 5 to 25 pairs. These cables are 28 AWG on 1.27 mm centres. Specifically:

10 conductor	(5 pair)	Spectra-Strip 843-132-2801-010
34 conductor	(17 pair)	Spectra-Strip 843-132-2801-034

7.2.2.2 Polarity and connector orientation

Headers should be assigned such that the signal which is logic “true” is at the nominal -0.8V state and is designated the “+” side of the pair. The “-” side of the pair will be a nominal -1.6V state when the signal is “true”.

RULE 7.2
Differential ECL logic “true” SHALL be designated by the “+” signal being at nominal -0.8V and the “-” signal being at nominal -1.6V.

RULE 7.3
Differential ECL front panel connectors SHALL be mounted such that the “+” side of the header is on the left when viewed from the front.

OBSERVATION 7.3
For single pair cables, it is easy to invert the signal by reversing the connector orientation upon insertion into the header.

RECOMMENDATION 7.5
In a front panel implementation, label the pairs as to their “+” and “-” orientation.

OBSERVATION 7.4
The header manufacturers convention for pin numbering places pin 1 at the bottom of a connector mounted on the right hand (component) side of a VMEbus board, as seen from the front, (the opposite to NIM, CAMAC and FASTBUS). The cable connector will then plug into the VMEbus module front panel header rotated by 180 degrees such that pin 1 of the connector will mate with pin 34 of a cable-mounted 34 pin connector.

RECOMMENDATION 7.6
For the reasons given in OBSERVATION 7.4 do not use shrouded and polarised headers on the module front panel.

RECOMMENDATION 7.7
When a 34 conductor (17 pair) cable is used for 16 differential signals, connect the unused pair to ground at the printed circuit header and mark the pair as “ground” on the front panel.

Front panel connectivity

OBSERVATION 7.5
The application of RECOMMENDATION 7.7 avoids ground loops.

Table 7.1 Differential ECL front panel connector

Signal +	Signal -
00	00
01	01
02	02
03	03
04	04
05	05
06	06
07	07
08	08
09	09
10	10
11	11
12	12
13	13
14	14
15	15
16	16
-	-

(view on front panel)

7.3 NIM

NIM signals originated in the NIM standard and are still popular. This digital signalling convention can be ideal for fast trigger generation and distribution as well as clock distribution. It should be considered when there are long signal runs, when sub-nanosecond timing is important, where signals source are widely separated and not conducive to cabling with ribbon style cables and when a single-ended signal is preferred. In addition, for many temporary laboratory set-ups, NIM signals can be more quickly interconnected with readily available coaxial cable assemblies.

NIM offers many advantages over single-ended ECL data transmission. NIM's strengths lie in the use of coaxial cable and the fact that its drivers are current sources. The coaxial cable brings good immunity to crosstalk and lower high frequency attenuation over long distances as compared to twisted pairs. This helps to maintain fast edge rates on signals and minimises ringing. Although either sub-miniature LEMO connectors or BNC connectors can be used the former are much preferred for density reasons.

7.3.1 Connectors

Suggested LEMO style connectors:

LEMO EPL.00.250.NTN or WW Fischer DLP101-A004-10

NIM-CAMAC series right angle receptacle for printed circuit

LEMO EPN.00.250.NTN or WW Fischer DP101 A-004-10

NIM-CAMAC series printed circuit board end launch receptacle

LEMO EPY.00.250.NTN

NIM-CAMAC series right angle dual receptacle for printed circuit - two connectors in one body

7.3.2 Polarity and signalling levels

The current source driver, resistive termination strategy of NIM is an excellent solution for single ended signal distribution. The NIM driver in the logic “false” state is “off” (0 mA) except for leakage (±1 mA max.). Therefore, the logic “false” level is determined by the ground at the termination resistor’s location, which should normally be at the input to the receiver. The receiver then has control over both the “false” state level and the switching threshold. The driver’s responsibility is to ensure a proper signal swing from the logic “false” to the logic “true” state. This method provides a considerably better noise margin then the single-ended ECL case where the receiver generates only a switching threshold and the driver can do whatever its local ground dictates!

When a logic “true” is to be generated. the NIM driver sinks 16 mA ±2 mA, which develops a voltage at the termination resistor. In a nominal 50 ohm system the logic levels for NIM are: “false” = 0V and “true” = -0.8V. Note that this is inherently “negative” logic such that the leading edge of a timing pulse is “falling” when viewed on an oscilloscope. This is the opposite of the ECL convention which is “positive” logic (important when conversion from NIM to ECL is to be made).

7.3.3 Implementation considerations

7.3.3.2 Double NIM

A “Double NIM” output can sink twice the normal 16 mA “true” state current. This is intended to be terminated with a 50 ohm resistor in two places, such as both ends of a line. these outputs typically have two coaxial connectors connected in parallel on the front panel of the modules. If only a single coaxial line is to be driven, then the other line must be terminated with 50 ohms.

7.3.3.3 Bussed NIM

Bussed NIM signals may be achieved with bridged inputs. In this, two coaxial connectors are mounted on the front panel with a removable termination resistor which takes up considerable front panel space. Another method is to use coaxial “T” connectors, but again at the expense of front panel space, and with the accompanying risk of reflections on the cable and a loss of fidelity of the distributed signal.

Front panel connectivity

7.4 TTL

TTL is not recommend for front-panel interconnects. It can be used on an “as needed” basis, such as the implementation of a “proprietary” bus between two sister modules.

> ***RECOMMENDATION 7.8***
> Mark all TTL front-panel input and outputs as such.

7.5 Low voltage differential signals (LVDS).

Advances in technologies (BICMOS, FPGAs, etc.) makes it increasingly possible to avoid power-hungry ECL for high-speed applications and thus also avoid the need for negative power supplies. In such case, a signalling standard with comparable performance and similar advantages as differential ECL, but compatible to BiCMOS technology becomes very attractive.

The proposed TIA/IEC SP-3357 standard (originating from the IEEE P1596.3 SCI LVDS standard) defines LVDS with following main characteristics.

7.5.1 Main characteristics

LVDS, like differential ECL, exhibits:

- near constant total drive current (decreasing noise on the supplies)
- excellent immunity to ground potential differences (between driver and receiver) and induced noise.
- low EMI (low, equal and opposite currents create small and cancelling electromagnetic fields)

7.5.1.1 Voltage levels:

At driver side (100 ohm load across opposite polarity outputs)

- (Voh) max: 1.6 V
- (Vol) min 0.9 V
- (Vod) differential output swing: 250 mV min, 350 mV typical, 400 mV max.
- loop current high state: +3.5 mA typical.
- loop current low state: -3.5 mA typical

At receiver side

- common mode input range: 0 to 2.4 V (referred to receiver ground)
- differential input threshold “high”: +100 mV max.
- differential input threshold “low”: -100 mV max.

7.5.1.2 Differential noise margins;

- High” and '“low”: min 150 mV, typical 250 mV.

7.5.1.3 Switching

- Rise/fall time: typical 300 ps.

Chapter 8: Analogue implementations
<<UNDER DEVELOPMENT>>>

8.1 Introduction

VMEbus is not an ideal platform for sensitive analogue implementations, but nevertheless is often used in such applications. This chapter gives a number of guidelines and recommendations which together describe a suitable VMEbus environment.

Annex B contains a narrative description on the subject.

8.1.1 Relation to VXIbus

The VMEbus Extensions for Instrumentation (VXIbus) specification describes extensions to the VMEbus specification which provide all the features necessary for the implementation of modular instrumentation. VXIbus includes many of the features specified in this document: ECL and analogue power, screening, large module format (9U x 340 mm and 6U x 340 mm).

8.2 Power for analogue circuits

The requirements for supply rails for analogue sub systems result from three factors:

1. The digital 0V reference is inherently noisy in a VME system,
2. The ±12V often gives insufficient voltage headroom for I/O requirements
3. The implementation of DC to DC converters on the module its self results in generation of additional noise and heat close to susceptible electronics often causing a reduction in their possible performance. Apart from being noisy DC to DC converters are only 70 to 90% efficient and are also a major cost component of any board. Provision of suitable supply rails will largely eliminate the DC to DC requirement.

8.2.1 Digital 0V

On a VME64 system, as any address/data word switches over any major code boundary, for example EFFFFFFF to F000000, the sudden surge in current pulled from the supply can cause the ground line to “bounce” resulting in the noise spikes appearing on the 0V rail. Although the problem of “ground Bounce” is addressed in the VME64 Extensions specification, supply surges will still occur, albeit to a possible lower level. ADC and DAC sub-systems are increasing in their conversion speed, (e.g. 30 MPs for a 12 bit ADC), and are easily capable of digitising the noise which appears on the digital 0V rail. The noise causes a significant reduction in the systems potential dynamic range if appropriate design precautions are not implemented, such as isolation and suitable component selection and layout. All of these engineering demands add considerable cost and complexity to any design. In short, the noise on the 0V digital rail can degrade the potential performance of the analogue sub-system.

To get round this problem most designs have either implemented isolated DC to DC converters or used an external supply approach. In the first instance DC to DC converters are expensive and have limited current drive and also generate heat and noise in the second the additional wiring harnesses and cables introduce a higher level of system integration complexity.

8.2.2 Using the ±12 V supply for analogue circuits

These supplies are often extremely noisy since most communication ports make use of them and, owing to their usual high switching rates, introduce noise not only on the ground but also on to the supply rails. Furthermore, most power devices, output drivers and in some instances input devices with a “High Dynamic Range” require more than 2V above the maximum input signal level on the supply lines to operate within their specification, in order to achieve the ±10V range, then greater than ±12V is required, thus renders the use of the ±12V rail unsuitable. Again to resolve this manufactures have resorted to using DC to DC technology or by using external supplies, and as described above this is often not the most cost effective or best solution.

8.2.3 On-board power conversion

The use of DC to DC converters can provide solutions to some system requirements such as board to board isolation or by the selection of a low noise, low capacitivly coupled DC to DC converters a higher accuracy sub-systems may be realised. In the main the DC to DC converters are used to provide the necessary ±15V rail required to attain the ±10V I/O capability. Although they have improved in efficiency over the last few years DC to DC converters still have a power loss and when running at or near to their maximum rating can dissipate considerable heat. This is a design factor most VME systems could well do without. Apart from the real estate they require, the heat dissipated, DC to DC converters also radiate considerable noise, again a factor any designer and system integrator would prefer not to have to contend with.

8.2.4 Jaux/Paux for analogue supplies

The Jaux/Paux provides ±15V primarily to supply analogue circuits. In addition, and analogue return, or reference, is also provided.

To allow fail-safe design a minimum of two pins should be allocated per rail, resulting in a total of six pins.

The ±15V rail should be kept to a tight specification thus allowing the integration of medium to high performance analogue sub-systems. The ripple should be of the order 20 mV peak to peak maximum, this should be expressed as an absolute value and not as an RMS value to ensure no high level spikes are tolerated within system designs. Any use of this supply must ensure that is no contamination of the rail. Appropriate design techniques include implementing suitable ferrite chokes and decoupling at the supply input on their board.

A further issue should be considered regarding the implementation of the bus. This can be either a user configurable Jaux per connector or by a bussed architecture. The bus architecture provides the simplest system integration, however this may result in the rail being unsuitable for high end applications such as true 14 Bit accuracy or 74 dB dynamic range @ 20 Mega samples/s. The user configurable back plane would be the only approach suitable for these types of design requirements. It may be possible to offer two different types or crate, one for high end applications which has a "point to point" wiring arrangement (user configurable) and a second of a reduced performance capability for general and less demanding applications.

8.2.5 Analogue reference

Having suggested making use of the Jaux as an analogue power bus it would be advisable to provide a clean Earth or reference Rail. This would be made use of as a true reference point for all analogue sub-subsystems. As this is a reference point it would provide no current sink or source capability and all users would buffer their electronics by way of a high impedance buffer amp (>100M Ohms). In this way it would be free from noise being caused by current flow as may be found in the ±15V return rail.

Chapter 9: Mezzanine Standards

9.1 Introduction

In recent years, a trend toward increased modularity of electronic equipment has become popular. The concept ("mezzanine concept") is to use general-purpose base boards that carry application specific mezzanine boards. This gives users an easy way to customise their system with off-the shelf or in-house designed components.

Base boards, or carrier, or mother boards, provide common infrastructure features (e.g., backplane-bus interfacing, compute resources, networking capabilities, etc.) for the mezzanines connected to them. Mezzanines are also known as daughter boards or piggy-backs. Both carriers and mezzanines follow a “mezzanine-bus” specification which defines the mechanics, the electrical, and logical layers.

Carriers exist as “intelligent” (with an onboard processor) or “dumb” (slave-only capability) boards. One finds standalone or bus-based (e.g., VMEbus, etc.) carriers. The mezzanines perform application-specific functions, such as analogue-to-digital conversion (ADC), digital input/output, graphics, communications, etc.. Carriers and mezzanines exist in different sizes (form factors). Examples are 3U- or 6U-sized VMEbus carriers, and single- or double-width mezzanines, with or without front panel option. Typically, carriers can accommodate 1–4 mezzanines.

With the growing popularity of mezzanines, one could observe a proliferation of products and specifications. For instance, VITA’s (VMEbus International Trade Association) “1995 VMEbus Product Directory” lists 30 vendors of company-specific mezzanine solutions. Four other mezzanine specifications are undergoing standardisation, with three standards being prepared under VSO (VITA Standards Organisation) and one under IEEE (Institute of Electrical and Electronics Engineers). They are:

- VITA 4-1995 - IP Modules
- VITA 12-199x - M-Modules
- VITA 14-199x - CXC / ModPack
- IEEE P1386.1 - PMC

Looking at possible application areas in physics, one can find a whole spectrum, ranging from simple industrial I/O to very-high bandwidth applications. It appears, that, at least for the time being, no single mezzanine standard covers the spectrum.

RULE 9.1
Mezzanines in physics SHALL be of the PMC [6] or the IP-Module [7] type.

OBSERVATION 9.1
An application-area overlap between IP-Module and PMC exists. Factors, like the existing environment (e.g., predominantly industrial I/O or predominantly high bandwidth) will determine whether to choose one or the other, or both mezzanine families in the specific case.

OBSERVATION 9.2
PMC (PCI Mezzanine Card), the combination of the PCI (Peripheral Component Interconnect) Local Bus specification [8] with the Common Mezzanine Card (CMC) [9] specification, has become an industry standard. Its peak data transfer rates of 132 Mbytes/s (for 32-bit wide

implementations) or 264 Mbytes/s (for 64-bit wide implementations) and the momentum which it has gained in industry make it the preferred candidate for high-bandwidth applications (e.g., data links, graphics, etc.).

OBSERVATION 9.3
IP-Modules, with their smaller size and simpler protocol, are intended to cover application areas with less-stringent bandwidth requirements. Peak data transfer rates for IP Modules are 64 Mbytes/s (for the 32 MHz clock version and 32-bit wide implementation).

OBSERVATION 9.4
Mezzanines provide a convenient base for in-house developments. Carrier boards provide infrastructure features, like networking capability, backplane-bus interface, compute resources, graphics, etc.. If engineers base in-house developments on mezzanines, they can take advantage of these existing features, without having to (re)design them.

RULE 9.2
PMC hosts that provide I/O through the backplane SHALL comply with the I/O mapping schemes as defined in the CMC Standard (IEEE1386.0).

Annex A: Summary

A.1 Introduction

Table A.1 summarises the features of the profiles and summarises the endorsement given by this document to each of the possible combinations of connector layout and board format.

Table A.1 Summary of features

	Connectors							Addtl. Power				
Format	96p J1	96p J2	160p J1	160p J2	30p Jaux	42/70p J0	Adr/Data	3.3	±15	-5.2/-2	Geo adrs	Specification
3U	X	-	-	-	-	-	A24:D16	-	-	-	-	VME64
3U	-	-	X	-	-	-	A24:D16	X	-	-	X	VME64 Extns
6U	X	-	-	-	-	-	A24:D16	-	-	-	-	VME64
6U	X	X	-	-	-	-	A32:D32	-	-	-	-	VME64
6U	X	-	-	-	-	X	A24:D16	-	-	-	-	VME64 Extns
6U	X	-	-	-	X	-	A24:D16	-	X	X	X	Rec. Practices
6U	X	X	-	-	-	X	A32:D32	-	-	-	-	VME64 Extns
6U	X	X	-	-	X	-	A32:D32	-	X	X	X	Rec. Practices
6U	-	-	X	-	-	-	A24:D16	X	-	-	X	VME64 Extns
6U	-	-	X	X	-	-	A32:D32	X	-	-	X	VME64 Extns
6U	-	-	X	-	-	X	A24:D16	X	-	-	X	VME64 Extns
6U	-	-	X	-	X	-	A24:D16	X	X	X	X	Rec. Practices
6U	-	-	X	X	-	X	A32:D32	X	-	-	X	VME64 Extns
6U	-	-	X	X	X	-	A32:D32	X	X	X	X	Rec. Practices
9U	X	-	-	-	-	-	A24:D16	-	-	-	-	Rec. Practices
9U	X	X	-	-	-	-	A32:D32	-	-	-	-	Rec. Practices
9U	X	-	-	-	-	X	A24:D16	-	-	-	-	Rec. Practices
9U	X	-	-	-	X	-	A24:D16	-	X	X	X	Rec. Practices
9U	X	X	-	-	-	X	A32:D32	-	-	-	-	Rec. Practices
9U	X	X	-	-	X	-	A32:D32	-	X	X	X	Rec. Practices
9U	-	-	X	-	-	-	A24:D16	X	-	-	X	Rec. Practices
9U	-	-	X	X	-	-	A32:D32	X	-	-	X	Rec. Practices
9U	-	-	X	-	-	X	A24:D16	X	-	-	X	Rec. Practices
9U	-	-	X	-	X	-	A24:D16	X	X	X	X	Rec. Practices
9U	-	-	X	X	-	X	A32:D32	X	-	-	X	Rec. Practices
9U	-	-	X	X	X	-	A32:D32	X	X	X	X	Rec. Practices

Annex B: Sensitive analogue implementations

B.1 Introduction

This annex contains a number of explanations of the problems encountered when implementing sensitive analogue circuits in the inherently electrically noisy environment which is VMEbus.

B.1.1 What is the problem?

The basic problem is that analogue and digital circuits do not mix well. This is a known problem for analogue designers but is less well known by the digital fraternity. Bussed systems are all bad, but VMEbus is probably among the worst, since it would appear that very little, or no consideration has been given to the problems of placing sensitive analogue electronics on VMEbus cards. The VXIbus approach, while much better in this respect, can only go so far in reducing the problems created by high speed digital circuits operating on the same powering system as their analogue front ends.

The major problem which digital circuits create is a high level of common-mode noise, i.e.. the entire crate “floats” above ground on a noise generator. Analogue circuits have to be connected in some way to the real world of signals exterior to this crate and therefore the above noise generator appears in series with each analogue signal. To a lesser extent, direct electromagnetic radiation from digital circuits can cause a number of problems for analogue electronics in the same crate. These types of problem are usually associated with false triggering or non-linearities.

B.1.2 What is the magnitude of the problem?

The common-mode noise source in a well designed crate can typically be reduced to a few hundred millivolts, but having spectral components ranging from a few kHz to several 100’s of MHz. A bad system may produce several volts by comparison. Therefore, if the analogue electronics has say an ADC with a 10 volt input range some suppression of the common-mode noise is needed to even exceed the 10 bit level for the best crate. Clearly, achieving higher resolutions, or using crate systems having higher levels of common-mode noise, needs even more suppression and this is where the difficulties start.

As far as radiated noise is concerned, the careful use of analogue ground planes and continuous metal shielding enclosures can normally reduce problems to acceptable levels, i.e. less than 1/2 an LSB.

The major difficulty is that solutions acceptable for say 12 bits are clearly inadequate for 14 or 16 bit performance or beyond. It is therefore essential to fix levels for the crate generated noise at a certain level which is adequate for most normal applications. Should the same crate then be called on to house, say an 18 bit converter, it becomes obvious that something else has to be done (see below). As you can see, it is a mixed problem of technical possibilities, general costs and dedicated design objectives. Your dilemma is therefore to fix the bar not too high, otherwise VMEbus will become a very expensive solution.

B.2 Solutions

B.2.1 Suppressing common-mode noise

The important word here is suppressing not eliminating. How well can you reduce the effects of this unwanted noise ? Very obviously, by suppressing it at the source if at all possible. One major noise source which can be identified and tackled easily is caused by the use of switch-mode power supplies in many VMEbus crates. Surprisingly perhaps, it is also mainly the design of the VMEbus power supplies which determines the electronics capacitance to ground and therefore the amplitude of the common-mode noise. The individual digital cards and the backplanes create some noise which can also be minimised by careful design. In this case digital ground planes and careful local decoupling can help for the individual cards but the backplanes still represent a large signal flow to ground via the above mentioned capacitance.

Provided the precautions outlined above are taken, the noise level should not be larger than the few hundred millivolts mentioned earlier. This noise level must then be suppressed by other means if analogue performance would be degraded by such a noise level. The usual means of reducing common-mode noise is via the use of differential or instrumentation amplifiers at the input to the sensitive analogue electronics. However, such amplifiers can provide adequate suppression only up to a limited bandwidth and are rarely of any use above 100kHz. Therefore, balanced filters must often be employed to suppress high frequency common-mode and radiated noise components which cannot be reduced by the instrumentation amplifier. The use of absorbing ferrites, continuous metallic shielding as well as the correct connection of cable screens plays a vital role in this area, particularly where the input impedances are high.

B.2.2 Alternative methods

The above assumes that the analogue electronics is powered directly from the standard VMEbus supply lines. It is not possible to quote an exact point at which no more improvement can be obtained, but it is probably between 12 to 14 bit accuracy. To go beyond this limit requires other approaches and/or some combination of all of them. This may sound confusing, but it is frequently necessary to combine some, but not necessarily all, of the methods of noise suppression to obtain a satisfactory result. Since the major source of common-mode noise appears between the zero-volt bus of the VMEbus and ground, a natural idea would be to isolate the analogue electronics by powering it independently. Use of a separate, but standard type of power supply to power the analogue part can be quite effective, but will suffer to some extent from the same problem as the normal VMEbus supplies. This is because the coupling capacitance to ground is still too high. The connections to the digital part of the VMEbus card must also be isolated otherwise noise enters via this path. Use of photo isolators or transformers can be considered, but the key design objective is to reduce the overall coupling capacitance to as low a value as possible. Therefore, it is not sufficient to consider one, but all the coupling paths, hence the power supply again becomes the weak point. Ideally, the total coupling capacitance should be reduced to the pico-farad level, but this is rarely possible. Photo-couplers, or better still fibre-optics, can be considered almost ideal, (provided there are not too many in parallel), however, the power supply needs special techniques to reduce the coupling capacitance to the 10's of pico-farad level.

The best approach would be to provide a separate, low coupling capacitance, analogue supply for each VMEbus card having sensitive analogue electronics on board, and to therefore have no common bus connections effectively tying everything together. The zero-volt connection of each sensitive electronics must then be referenced to the ground of the signal source to which it is connected. Provided that the precautions mentioned earlier, with respect to photo-isolators, instrumentation amplifiers, filters, shielding and screened cable connections are observed, an excellent analogue performance should be obtained to beyond the 16 bit level. It is therefore vital to tackle the most important point first and this is the power supply. It is possible to obtain supplies which are on-board DC-DC converters which are optimised for this type of application. They will probably employ a resonant high frequency technique with very low levels of radiated noise. Such supplies can provide adequate power for most modern analogue circuits and could be powered either from the ± 12V VMEbus supplies or from the 48V line. A separate zero volt pin for each VMEbus card (clean ground/guard/ground return or whatever you want to call it) is absolutely vital for this scheme to work and it must be connected to ground somewhere exterior to the VMEbus crate, which itself must be connected to ground too. If, as so often happens, the analogue electronics is left floating, it is not able to work correctly.

B.2.3 Connectors and Busses

As mentioned earlier, VMEbus is not really a good platform for sensitive analogue applications, particularly from the connector point of view. Mixing of any analogue signal lines with digital or supply lines is to be avoided, since the inevitable coupling capacitance between pins or adjacent lines is a disaster. Use of screened cable is not practical either. Therefore, while it is certainly very practical to have inputs on the rear of a module they should, if possible, be well separated i.e. on a special connector or the P2 if unused for digital signals. For very sensitive signals, a special, isolated and fully screened front panel connector would actually be the best arrangement. Such a connector should have signal high, signal low, ground return/guard and isolated screen.

Annex C: Wired-OR glitch

Consider a transmission line where a number of drivers are sinking current in a wired-OR manner. The terminators will supply current more or less equally to each of the drivers, and if one driver switches off, the current it had been sinking will be shared between the other drivers.

If an instantaneous view is taken of the switching off of the driver, and the line is considered as a real transmission line with a finite signal propagation time, then, although the final stable state is the sharing of the current, the short term events are not as simple. In Figure D.1, the loss of the current sinking capability of a driver by its being switched off, may be considered as equivalent to the injection of a current *i* at that driver. A voltage step will therefore be produced across the characteristic impedance of the line as seen at the driver, which will travel towards the terminators at the propagation speed of the line.

The practical situation may be exacerbated by differences in the characteristics of the drivers, through manufacturing tolerances, temperature differentials, etc. These differences will mean that the current sinking capabilities of the drivers will not be the same.

Consider a system with two drivers, one sinking all the current, the other, none. If the former driver now switches off, the line will be momentarily released to the high state, and a voltage step equal to the logic high level *v* will propagate towards the terminators. When the other driver receives this step, it will begin to sink the current, and will return an equal step of the opposite polarity, effectively returning the line to the zero state. However, any receiver connected to the line between the two will sense a pulse greater than its logic threshold, and will switch. If the two drivers in question are at opposite ends of the bus, the resulting pulse will be equal in length to twice the propagation time of the line (T_{CP}), and a receiver connected to the line near to the driver which switches off will see a pulse of that duration.

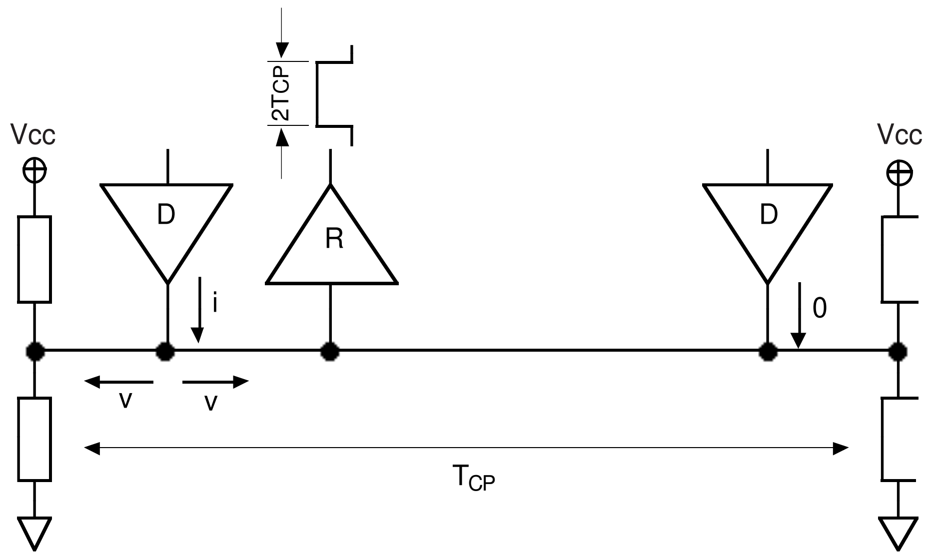


Figure C.1 Wired-OR glitch