

Status Report on the RD-12 Project

**Timing, Trigger and Control Systems
for LHC Detectors**

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Timing, Trigger and Control Systems for LHC Detectors

1 Introduction

At the LHC experiments timing, trigger and control (TTC) signals must be distributed from a small number of sources to numerous electronic systems located in the ALICE, ATLAS, CMS and LHC-B detector caverns and underground electronics rooms. The LHC timing reference must be delivered with low jitter and programmable phase. First-level trigger decisions must be broadcast from the central trigger processor to all the front-end pipeline controllers and delivered synchronously with the appropriate bunch and event identification, compensated for particle flight times and detector, electronics and propagation delays. In addition, fast synchronous commands must be broadcast to control the running of the experiment and the execution of tests of the detectors and read-out systems, and individually addressed controls and parameters such as channel masks and calibration data have to be distributed.

In view of the fact that the TTC system provides a basic resource which must interface with the LHC machine timing, CERN management has expressed an interest in identifying and supporting a uniform solution which would be acceptable to all parties. A global solution would benefit from important economies of scale and lead to a simplification of the development, operational and maintenance efforts compared with the use of a plethora of different distribution systems using incompatible architectures, coding schemes, data rates, timing ASICs or optical transmitters, receivers and wavelengths for each subdetector.

Within the framework of LEB Project RD12 a general solution to the problem of TTC distribution is being developed [1] which is applicable to the backbones of all the subdetectors of the LHC experiments. The Project collaboration now comprises representatives from ALICE, ATLAS, CMS and LHC-B, CERN Microelectronics and Electronics Groups, six external institutes and two European industrial companies. The system has been adopted for the ATLAS [2] and CMS [3] TTC backbones and is currently being considered for ALICE and LHC-B.

2 LHC timing

The bunch structure foreseen for normal proton-proton operation of the LHC is shown in Fig. 1 and the basic timing parameters are listed in Table 1. With an RF frequency of 400.8 MHz there will be 35640 RF buckets in each LHC ring of circumference 26.66 km. For “25 ns” (24.95 ns) bunch spacing, 1 bucket in 10 within the bunch trains will be occupied by a bunch of 4σ length about 31 cm.

The basic structure comprises 12 “SPS batches” each composed of 3 “PS trains” of 81 bunches separated by gaps imposed by the rise times of the extraction and injection kickers required to transfer the beam from the PS via the SPS to the LHC [4]. Because of the 12-fold symmetry, bunch trains will be correctly phased for collisions

at 24 points around the LHC and 8 of these can be positioned in the straight sections by adjustment of the injection timing. While the gaps reduce the machine filling factor to about 80%, they may prove useful for the management of the detector synchronisation by crosscorrelation of event hit data with the bunch structure [5].

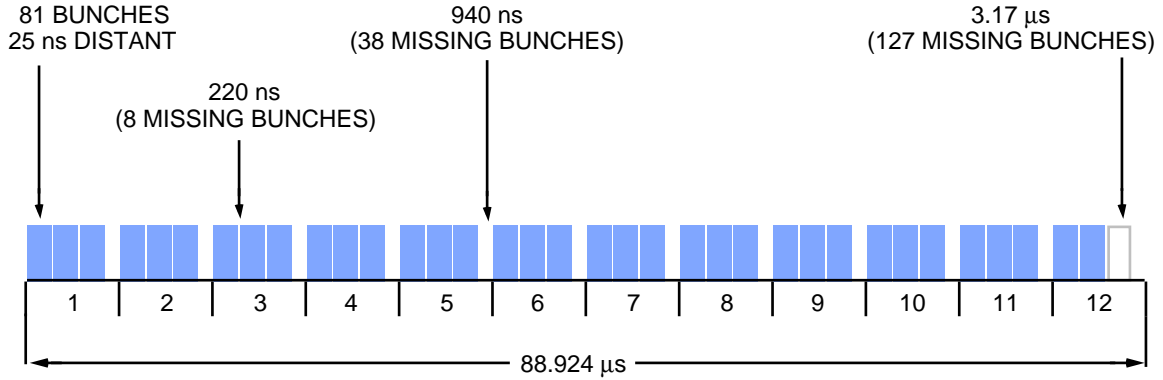


Fig. 1 LHC bunch structure

The third PS train of the twelfth SPS batch will be suppressed to create one long gap of 3.17 μs in each beam to allow time for the rise of the extraction kickers of the beam dumping system. The extractor gaps of the two beams will coincide at only two diametrically opposite points. At the other intersection regions only 2754 instead of 2835 bunches will collide, resulting in a 3% reduction in luminosity.

Revolution time	88.924 μs
Revolution frequency	11.246 kHz
RF frequency	400.8 MHz (2 x SPS)
Bunch crossing rate	40.08 MHz
No. of bunches/beam	2835
Filling factor	0.795
Bunch train length	81
SPS injection kicker gap	220 ns
LHC injection kicker gap	940 ns
LHC extraction kicker gap	3.17 μs
Full bunch length (4σ)	0.31 m
RMS collision length	0.053 m
Interbunch spacing	7.5m, 25 ns

Table 1 LHC timing (pp)

The synchronisation procedure must be able to adapt to the fact that the injection phase may be altered to favour one pair of intersection points or another at different times. The bunch structure indicated will also be subject to change, at least during

the initial period of machine development [6]. The TTC system will therefore assign consecutive numbers in the range 0 to 3563 to all “potential” bunch crossings per orbit. One of its tasks is to make this number available along with the corresponding trigger decision at the electronics controllers; correctly compensated for time-of-flight, detector and electronics delays and for the propagation delays over the different optical fibre paths of the distribution network itself.

CERN has already developed techniques for the transmission of stabilised radio-frequency phase references over long optical fibre links [7] and the technology has been transferred to industry. We do not anticipate that major new developments will be required to transmit the required LHC machine timing reference signals to the central nodes of the TTC systems in the underground electronics rooms. In addition to the 40.08 MHz bunch-crossing clock, these will include a square wave once-per-revolution signal called the Orbit signal.

Because both signals are periodic, their transmission is not subject to systematic data-dependent jitter and a high degree of suppression of random jitter can be achieved by the use of a very stable VCXO in a primary PLL with narrow loop bandwidth. Since the Orbit signal is qualified by the LHC clock a phase-compensated link is required only for the latter signal.

For synchronisation purposes, it would be possible to use either local beam monitors or control room signals for the bunch structure information under different operational conditions. The instrumentation [8] required for this is not expected to present any major challenge compared with that already in place for LEP.

Due to the very high average beam current and the combination of a high RF frequency and long revolution period, transient beam loading will be very significant in the LHC and phase modulation of the circulating beams will be a concern for timing [9]. For reasons of symmetry the position of the collision centroid in the even intersections will not move, but at the odd intersections at which ATLAS and CMS will be installed the maximum displacement at full intensity will be about 1 cm (33 ps). The RMS collision length for proton bunches in the LHC will be 0.053 m, corresponding to an initial spread of about 180 ps relative to the equilibrium bunch phase.

3 Architecture

To minimise the level-1 trigger latency, the trigger processors and central trigger logic will be located in the underground control areas as close as possible to the special direct trigger cable ducts communicating with the detector caverns. A small number of relatively high-power laser sources will be installed at these locations to distribute the TTC signals to their destinations through entirely passive all-glass networks composed of a hierarchy of optical tree couplers (see Fig. 2). At each destination, a special timing receiver ASIC (TTCrx) delivers all the signals required by the electronics controllers.

The tree architecture of this distribution network is well matched to the physical configuration of the underground areas, the co-located signal sources and the dispersed destinations. It requires considerably less optical fibre than a star configuration of point-to-point links from a central fanout and permits the flexibility

of extensive intermediate connectorization, since only the final destination connectors contribute significantly to the cost. The optical couplers have small size, low mass and unlimited bandwidth. They require no operating power and are potentially highly reliable [10].

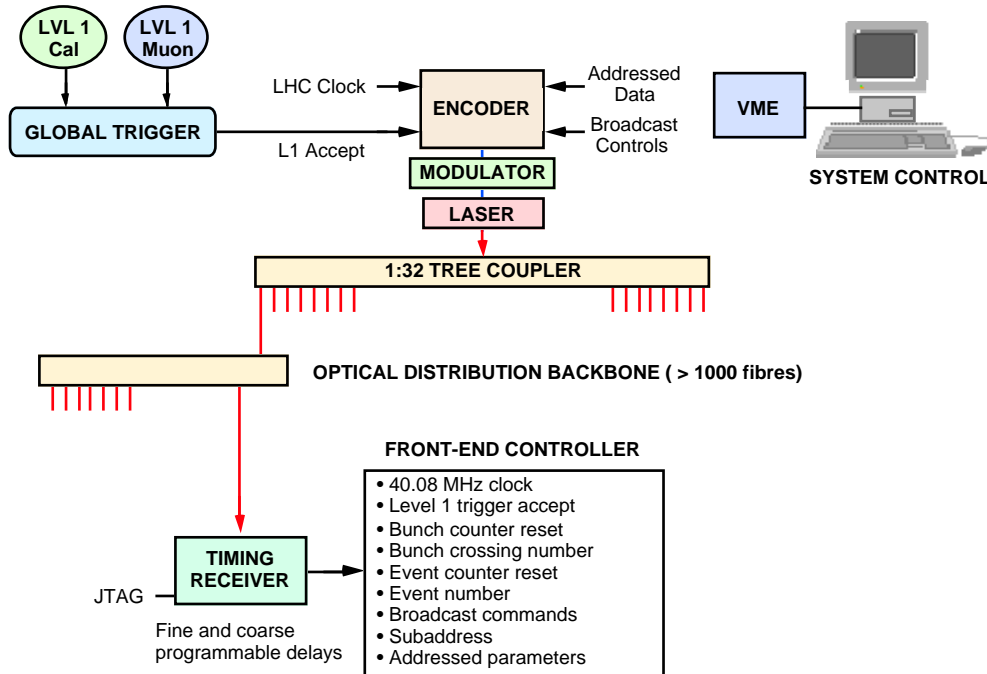


Fig. 2 TTC distribution components

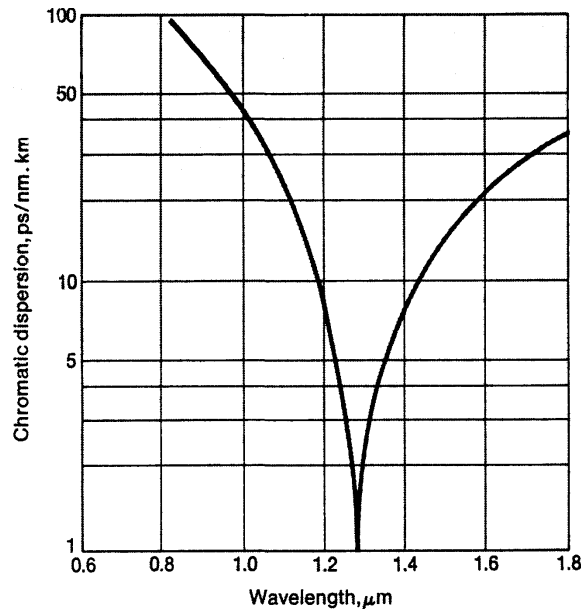
Each laser transmitter serves a TTC distribution zone which is typically associated with a major component of a subdetector, such as an entire end-cap or barrel section. Owing to the small number of laser sources employed for the complete system, it is economically feasible to optimise performance and reliability by equipping all of them with full three-term feedback controllers providing precision temperature regulation and incorporating comprehensive low-noise stabilisation and protection circuitry.

Furthermore, continued improvements in the efficiency, reliability, intensity noise, spectral and modulation characteristics of laser diodes are to be expected during the years preceding start-up of the LHC. As new devices become available, the architecture adopted allows the TTC system to be upgraded much more readily than if thousands of individual LED sources had been employed.

4 Laser transmitter

Several considerations have led to the selection of 1310 nm as the operating wavelength for the TTC systems. At this wavelength the chromatic dispersion of normal optical fibre is negligible (see Fig. 3), so that Fabry-Perot laser diodes operating in multiple longitudinal modes can be used and the effect of the chirping

caused by direct modulation is minimised. The overall length of fibre in each distribution path being only about 100 m, fibre attenuation is negligible. Hence in a short-range timing distribution system the minimum-dispersion wavelength of 1310 nm is more appropriate than the minimum-attenuation wavelength of 1550 nm.



(Ref: HP 5952-9554)

Fig. 3 Chromatic dispersion of optical fibre

Multimode Fabry-Perot lasers are less expensive and available with higher output powers than distributed-feedback types. They are considerably less sensitive to optical feedback noise [11] and as a result have been found to perform satisfactorily without the use of isolators in spite of the Fresnel reflection from multiple inexpensive (non angle-polish) connector interfaces in the distribution path.

At 1310 nm, even inexpensive LED sources having a relatively broad output spectrum can be used successfully for low-power test systems, whereas at 830 nm the fibre dispersion of 80 ps/nm.km (1 ns for a 125 nm wide source and 100 m length of fibre) excludes them from applications requiring precise timing. While somewhat higher laser powers [12] are currently available from the most expensive short-wavelength AlGaAs lasers than from long-wavelength InGaAsP diodes, this gap is narrowing and the projected lifetime of the latter devices is more than an order of magnitude longer.

Step index multimode fibre is unsuitable for this application because of its large multimode dispersion, while the use of monomode fibre would incur high optical tree coupler and connector costs and limit the coupling efficiency from high power laser sources, which have divergent output beams. On the other hand, 50/125 μm graded index fibre can provide adequate bandwidth over the short path length (several GHz for 100 m) and is available in boron-fluorine doped form with good radiation tolerance characteristics.

Graded index fibre multimode dispersion varies with optical wavelength. Fibre that has low dispersion at 1310 nm is substantially cheaper than fibre that has the same

dispersion at 830 nm or which has a compromise performance at both windows. Finally, both the appropriate photodetectors and the optical fibre itself are more radiation resistant at 1310 nm [13].

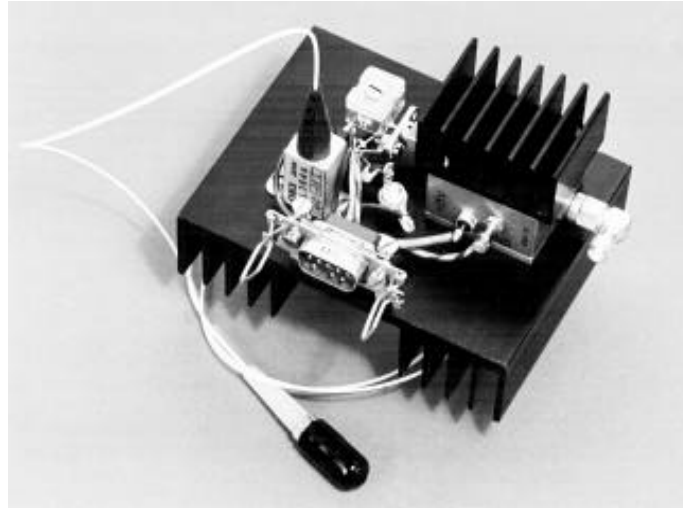


Fig. 4 Laser transmitter head module

External modulators are normally polarisation-dependent and have significant insertion loss. With direct modulation of currently available laser diodes it is quite feasible to broadcast reliably to groups of 1024 channels per transmitter through 100 m of 50/125 μm graded index fibre and two levels of 1:32 passive optical tree coupler.

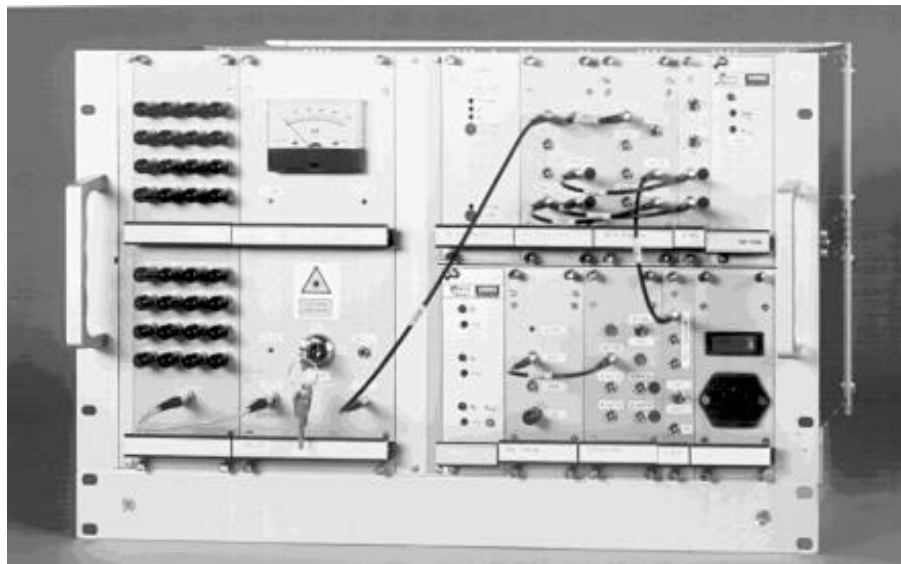


Fig. 5 TTC transmitter crate

Fig. 4 shows the laser head module of the transmitter. It incorporates a 0.4 W RF amplifier with a bandwidth of 10 MHz - 1 GHz, an inexpensive bias tee fabricated

with ferrite beads and an adjustable matching network for the very low impedance input of the laser diode. The laser has an integral Peltier cooler element and monitor thermistor, which permits a compact assembly. A complete transmitter subsystem crate is shown in Fig. 5.

This transmitter is capable of distributing the TTC signals through three levels of 1:32 tree coupler (1:32768 fanout). In practice more modest fanouts will be employed to allow adequate margins for component tolerances and radiation-induced receiver degradation. Users should be aware that such lasers generate invisible infrared energy and that ocular exposure to the output should be avoided. The transmitter module is equipped with a key-operated master control in accordance with CERN TIS/RP rules [14] for the safe use of lasers, which are based on IRPA guidelines.

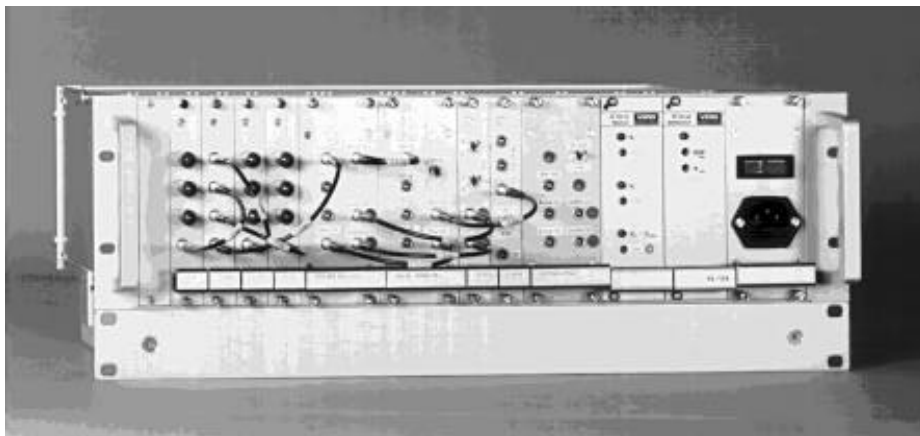


Fig. 6 Mini-crate transmitter subsystem for electronics developers

For electronics development at CERN and associated institutes it is not always necessary to have the high-power laser capable of transmitting to several thousand receivers. To meet this need a mini-crate system (see Fig. 6) has been developed which does not support a large optical fanout but which supplies a few channels of compatible signals for development work and costs less than half as much.

The mini-crate can be expanded by the addition of extra transmitter modules which supply groups of three channels each, but if more than a few such modules are required it is recommended to procure the full size crate with its higher power source. If a mini-crate is subsequently upgraded to a high-power transmitter a number of the modules and power supplies can be recuperated. Both high-power transmitters and mini-crates are available now and several have been delivered to the first developers.

5 Encoding

As indicated in Fig. 7, the laser modulator is driven by an encoder which is phase-locked to the LHC clock and linked to an associated trigger select and serializer TTC-VMEbus interface (TTCvi) module [15].

The TTC system must deliver broadcast and individually-addressed signals to several thousand destinations. An important reduction in receiver cost, power consumption, size and mass is achieved by encoding these signals in such a way that they can be received by a single optoelectronic detector per destination. The encoding should also allow the signals to be transmitted at a relatively low rate compatible with the photodetector/preamplifier devices that are being manufactured in the highest volumes and at the most competitive prices for the LAN market.

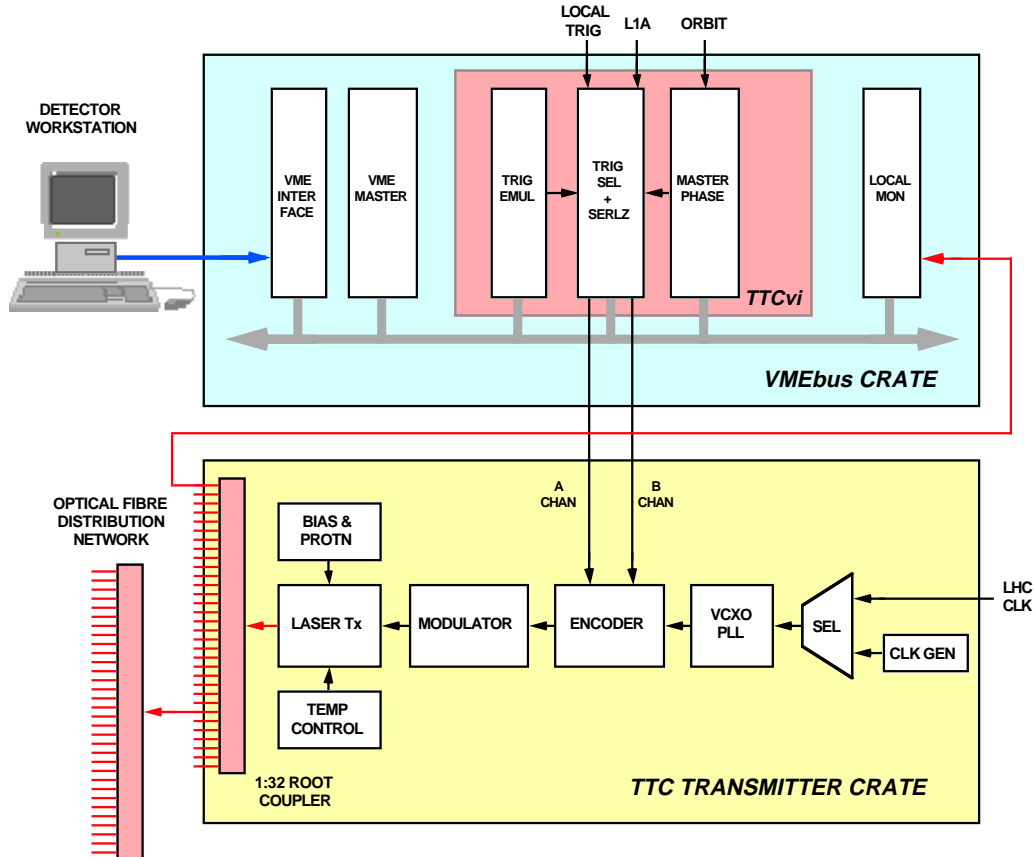


Fig. 7 TTC transmitter elements

The code employed must be balanced (DC-free) so that the phase of the extracted timing reference is quite independent of the level-1 trigger data being transmitted. The signals must be reliably decoded by receivers that may be subject to radiation-induced sensitivity changes and offset shifts, so that the use of pulse amplitude modulation and non-binary transmission requiring multiple detection thresholds is excluded.

Evaluation of a number of signalling alternatives offering different tradeoffs between channel efficiency and synchronisation precision led to the selection of a scheme whereby two data channels are time-division multiplexed (TDM) and encoded biphasic mark at 160.32 MBaud (four times the LHC bunch-crossing rate). This is sufficiently close to the standard Sonet OC-3 (CCITT SDH STM-1) rate of

155.52 MBaud that an expanding range of photodetector/preamplifier components produced in increasingly high volume is appropriate.

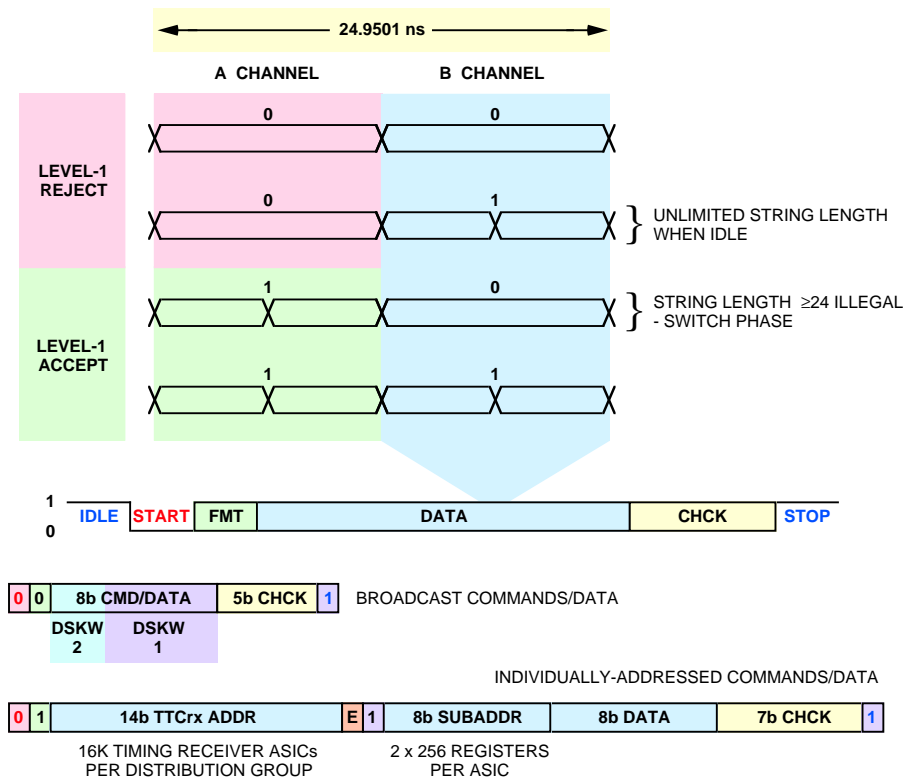


Fig. 8 TTC signal encoding

The four symbols which can be transmitted in each bunch-crossing interval are shown in Fig. 8. The DC offset is well bounded and timing reference signal transitions are generated at the start and finish of every such interval.

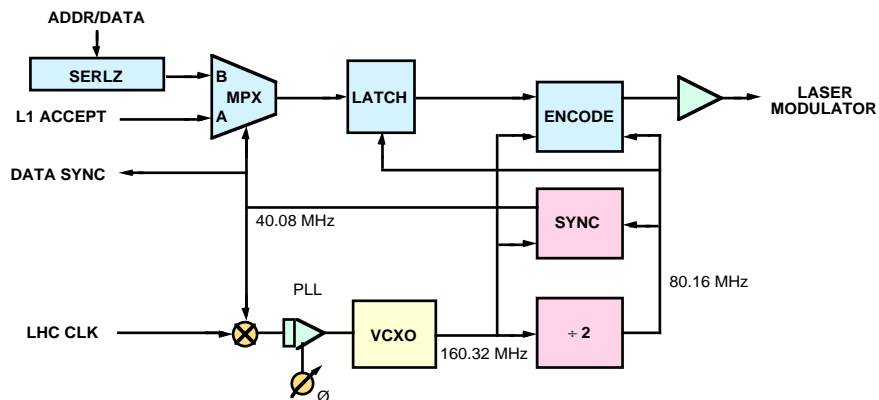


Fig. 9 TDM biphasse mark encoder

This is not the case for many alternative line codes such as non-return-to-zero (NRZ) inverted, scrambled-NRZ, enhanced (run-limited) NRZ, coded mark inversion, biphasse level (Manchester), Miller (delay modulation, modified frequency

modulation), Miller-squared or mB/nB group codes. A block diagram of the encoder is shown in Fig. 9. The encoder 160.32 MHz VCXO is phase-locked to the LHC clock, or a local clock generator, by a PLL employing a high gain active loop filter with low offset drift.

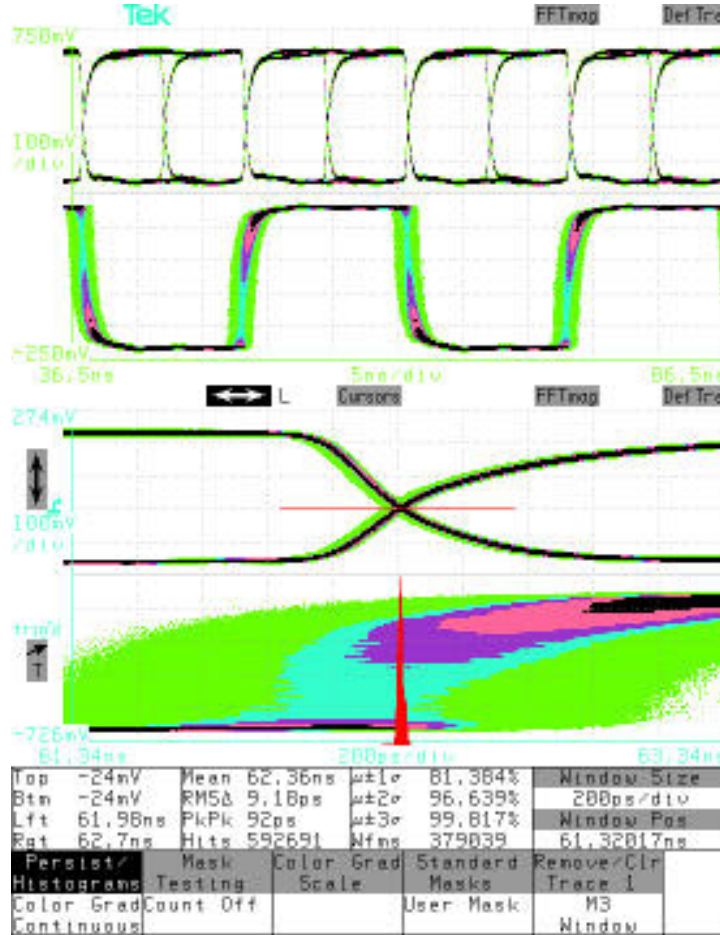


Fig. 10 *Upper trace:* encoder output (PRBS data)
Second trace: noisy reference clock input
Third trace and histogram: encoder jitter
Lower trace : reference clock input jitter

By means of an oscillator having low internal noise and a narrow loop bandwidth, a 160.32 MHz output jitter of less than 10 ps RMS can be maintained for a 40.08 MHz reference clock input jitter of several hundred ps, as shown in Fig. 10. In this test the jitter of the reference clock was increased by sending it to the TTC transmitter crate over an optical fibre link with artificially increased attenuation.

The “prompt” TDM A Channel, which is designed for minimum latency, is dedicated to the broadcasting of the first-level trigger-accept signal, delivering a one-bit decision for every bunch crossing. The B Channel transmits broadcast and individually-addressed commands or data using the frame format shown in Fig. 8.

During a short programmable interval at the end of the 3.17 μ s LHC extraction kicker gap in one of the beams, other transmissions are held off so that the bunch counter reset signal can always be broadcast with exactly the required phase.

Although this signal arrives at the receivers at different times because of the different lengths of the optical fibre paths, it experiences the same propagation delay to any receiver as the trigger-accept signals and so does not require separate delay compensation.

High priority is assigned to other synchronous broadcasts, while in the background the timing calibration controller can continuously scan all the timing receivers transmitting fine deskew adjustments to compensate for phase wander due to changes of temperature, fibre tension, optical wavelength, signal amplitudes, voltage drifts and component ageing.

The addressing scheme provides for up to 256 external and internal subaddresses associated with each of up to 16K timing receivers in each timing distribution group. With standard two-channel biphase mark encoding, there is a fundamental ambiguity in the phase of the recovered clock. This is resolved automatically in the receivers by monitoring constraints on the data structure imposed by the B Channel data format. Hamming checkbits permit the forward error correction of all single-bit and the detection of all double-bit errors, as well as many others.

6 TTCvi VMEbus interface

The TTC-VMEbus interface (TTCvi) module interfaces the TTC system to the Central Trigger Processor (Global Trigger) and to the control processors or development workstations which generate commands and data to be transmitted to the electronics controllers. The module delivers the A Channel and B Channel signals to the TTC transmitter crate for multiplexing, encoding, optical conversion and distribution to the timing receiver ASICs at the destinations

To minimise the possibility of configuration errors, the characteristics of the module and the signal routing which it controls are fully programmable from the VMEbus.

The TTCvi incorporates a programmable L1A source selector (for four external sources) and an internal trigger emulator (a random signal generator with a period of $2.15 \cdot 10^9$ and a programmable average rate from 1 Hz to 160 kHz) for test purposes.

The B Channel signals can be in either of two formats:

- Short-format synchronous or asynchronous broadcast command/data cycles. If synchronous, the timing of these cycles relative to the LHC orbit is controlled precisely. They are used for the broadcasting of the bunch counter reset signals which control the phases of the TTCrx bunch counters, and for the transmission of other fast synchronous broadcast controls and test commands or data. The timing of the synchronous cycles is fully programmable with respect to the external Orbit signal (or to an internally generated one for test purpose).

These commands are deskewed in the TTCrx ASICs to compensate for individual differences in fibre propagation delay, electronics and detector delays and particle times-of-flight.

- Long-format asynchronous individually-addressed or broadcast command/data cycles. The timing of these cycles with respect to the LHC orbit is indeterminate and they are not individually deskewed in TTCrx ASICs. They are used for the

transmission of parameters, test data, calibration data and non time-critical commands, such as channel masks, to the front-end electronics.

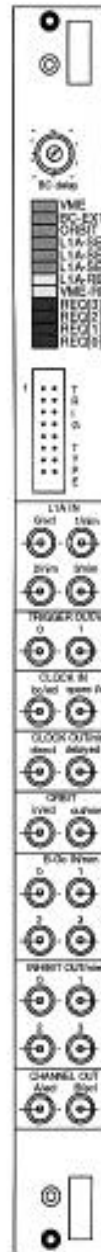


Fig. 11 TTCvi front panel

Synchronous and asynchronous short- and long-format B Channel command/data cycles can be generated in a number of different ways:

- Short- and long-format asynchronous cycles.

Asynchronous cycles may be initiated by writing the required data (a single byte for short-format or two 16-bit words for long-format) to specified TTCvi VME addresses. Normally short-format cycles are used for broadcast commands or data

while long-format cycles are used for individually-addressed commands or data. However, a broadcast of 16 bits of data can be made with long-format cycles if TTCrx address 0 is chosen. The timing of these cycles is not synchronised with the LHC orbit.

- Pre-loaded synchronous or asynchronous cycles.

Four VME-addressable FIFOs are provided which may be pre-loaded with commands and data to be transmitted by B Channel cycles. For each of the four channels, the actual transmission of the pre-loaded information is initiated by a signal called B-Go<3..0> which can be generated either by a VME write to a key address or by an external signal applied to one of four front panel inputs. It is also possible to start the cycle transmission as soon as the FIFO is not empty. This last mode will facilitate the use of several TTCvi's in a single crate by reducing the VME access time: one can fill the FIFO in DMA mode and start the transmission as soon as the FIFO is not empty. Sequences of B Channel cycles can be generated by loading the FIFOs with several parameters.

A VME-addressable register associated with each of the channels allows the selection of synchronous or asynchronous mode, and VME or front panel generation of B-Go.

If synchronous mode is selected, the B-channel cycle is generated at a programmable time within the LHC orbit. The cycle can be programmed to be either single or repetitive. In the latter mode the cycle is generated for each LHC orbit. The bunch counter reset command, for example, is sent with this repetitive mode.

If asynchronous mode is selected, the B Channel cycle is generated when the B-Go<i> signal occurs. There will be one cycle and one cycle only for each occurrence of the signal.

- Event number and trigger type cycle.

After each L1A is transmitted, the contents of the 24-bit event counter in the TTCvi can optionally be broadcast together with an 8-bit trigger type parameter which is received from the Central Trigger Processor via a front panel connection. This broadcast, which is intended for check purposes, is made asynchronously and takes about 4.4 μ s if the B Channel is free.

The front panel of the TTCvi module is shown in Fig. 11. The module contains about 300 components including 10 Altera FPGAs and 20 synchronous FIFOs. The TTCvi design has been completed and fully simulated. The PCB layout is in progress and despite space problems on the board, which are being solved, it is expected that prototype modules will be available during 2Q97.

7 Optoelectronic receiver

Although it is foreseen that LHC detectors will have many optical links for data readout and monitoring purposes, the TTC network may be one of the few systems requiring hundreds of optoelectronic receivers located on and within certain subdetectors. The photodetectors used should have high optical signal responsivity, low sensitivity to ionising and neutron irradiation and fast rise times at a low reverse bias voltage, preferably less than 3.5v.

InGaAs PIN diodes are superior to normal Si photodiodes in most technical characteristics including radiation hardness. The current packaging configuration approach for TTC optoelectronic receivers is a subminiature connectorized InGaAs PIN + Si bipolar preamplifier device with differential outputs connected directly to a separately packaged low-power timing receiver ASIC containing the postamplifier/AGC circuit followed by all the necessary analogue and digital functions. The PIN + preamplifier (Fig. 12) has a bandwidth of 160 MHz and incorporates a second amplifier for power supply noise cancellation. It has shown little performance degradation after 20 MRad ^{60}Co irradiation [16] and further tests are in progress.

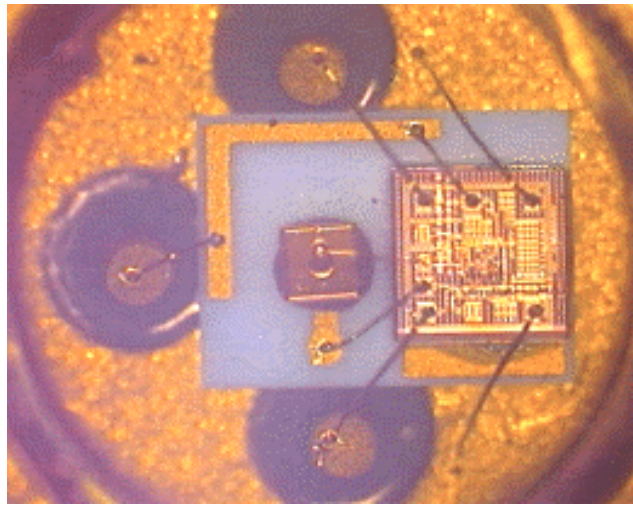


Fig. 12 PIN + Preamplifier

Several manufacturers are currently introducing monolithic InGaAs/InP receivers in which PIN or MSM photodiodes are combined with a transimpedance amplifier using HBTs or MODFETs. Although clear performance advantages relative to hybrid designs have yet to be achieved, these OEICs could eventually open the way to the high volume fabrication of very cheap components, including “smart connectors” integrating all the standard optoelectronic receiver functions.

8 Optical connector

While conventional optical single-fibre connectors, such as the popular ST/PC type, are quite appropriate for use in small numbers at the TTC transmitters, they are too massive for use at receivers in a particle physics detector and often contain high-permeability carbon steel springs and circlips. They are inconveniently large even for mounting on some high-density modules in external electronics readout crates.

In collaboration with our industrial partners, a new subminiature “RD12 Connector” family has been developed for this application. The connector, which is non-magnetic and manufactured only from proven radiation-hard materials, mates with an active device mount designed to accommodate the PIN + preamp with an absolute minimum of additional mass and volume (see Fig. 13). A prototype series

has been manufactured and pre-production testing has been carried out including vibration tests specified by an aircraft manufacturer which is one of the potential users of the devices.

The RD12 connector family also includes a subminiature coupler for connector-connector interfacing at bulkheads. The coupler, which has a mass of less than 0.7 g, is compared in size with its conventional ST counterpart in Fig. 14.

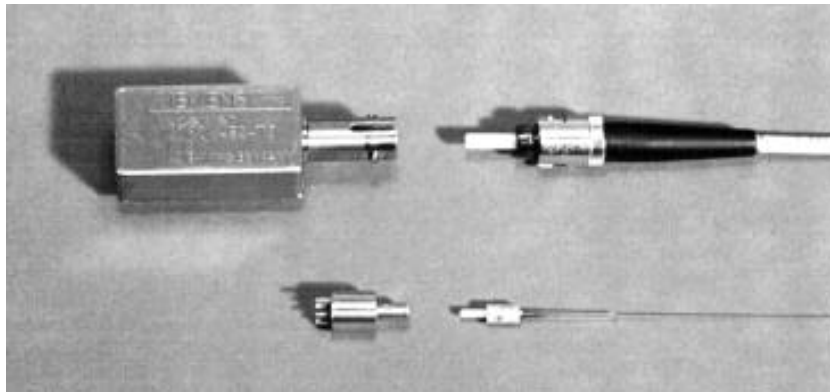


Fig. 13 Conventional ST and subminiature RD12 connectors

The RD12 Connector incorporates a zirconia ceramic ferrule to ensure high reliability, but its diameter is reduced to only 1.25 mm. ARCAP alloy is used for the device housing and polyether etherketone (PEEK), a glass-fibre enhanced thermoplastic material, for the connector shell. The PIN + preamp manufacturer actively aligns the TO-46 devices within the device mounts to ensure maximum responsivity, an operation that can be automated on a production line basis.

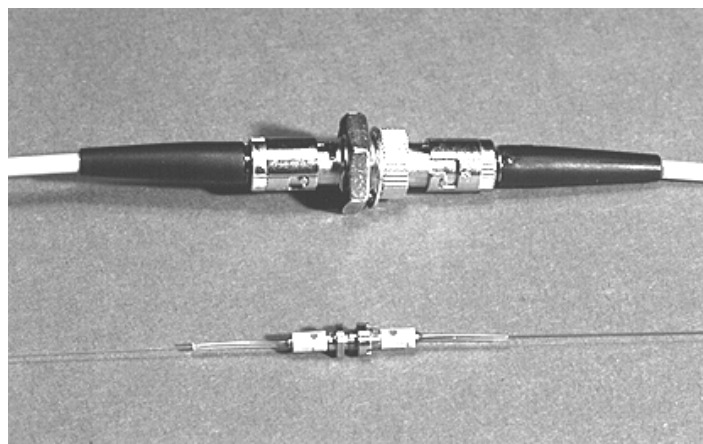


Fig. 14 Conventional ST and subminiature RD12 couplers

No really tiny affordable connector/device mount for single optical fibres has so far been brought to the market. The RD12 Connector may meet this need in a number of future applications in other areas where very small size and low mass are important. The series is now being introduced commercially and preliminary data are given in Figs. 15 - 17.

PRELIMINARY
VERSION



RD-12 Sub-Miniature Fibre Optic Connector

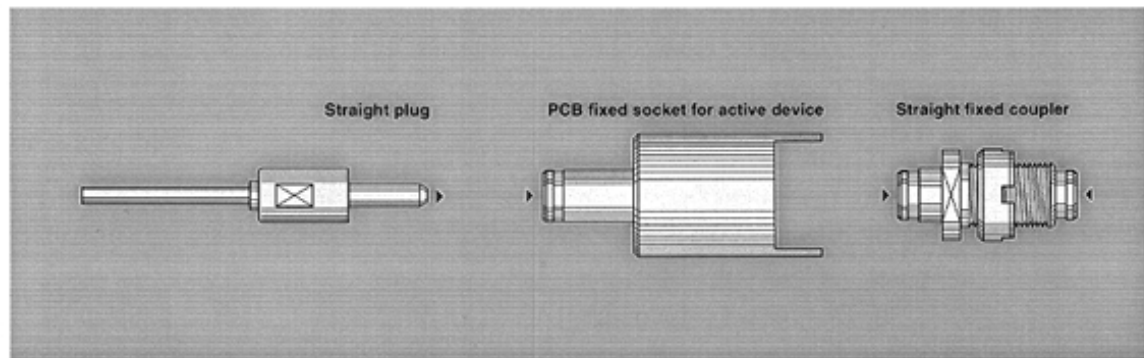
Introduction

The LEMO RD-12 is an extremely small fibre optic connector which is ideal for use in very confined areas. It uses materials which are compatible with radioactive environments and its low mass makes it an ideal choice in the fields of avionics and particle physics.

Features

- Sub-miniature size
- Low mass
- Push-Pull snap-on latching
- Compatible with TO18 transmitter/emitter components
- Very low insertion loss for both multimode and single-mode
- Fully floating ferrule
- Simple termination

Interconnections



Part section showing internal component

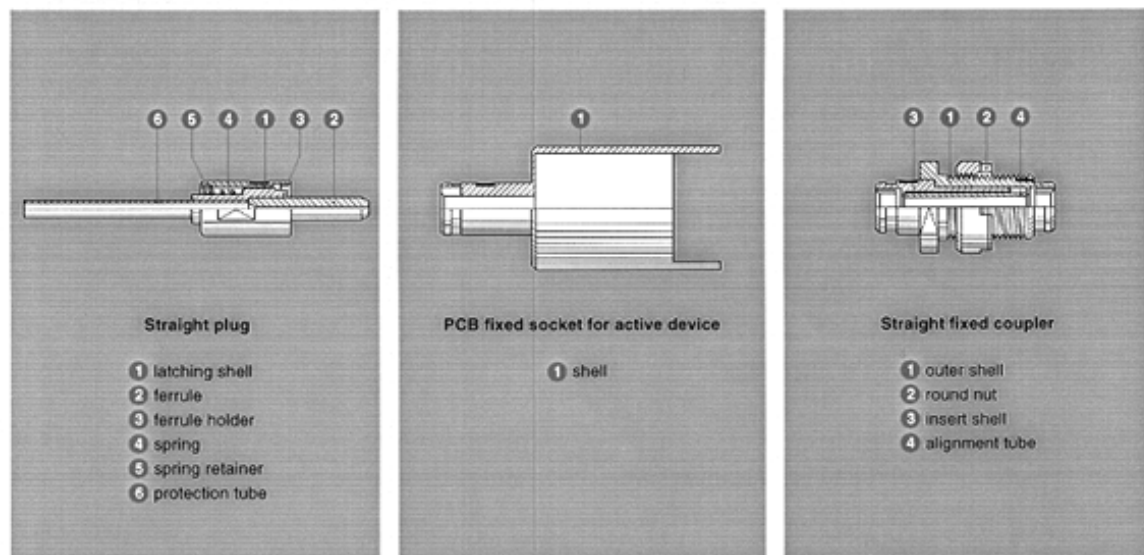
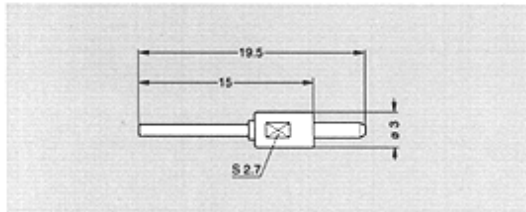


Fig. 15 RD12 Connector family and sectional drawings



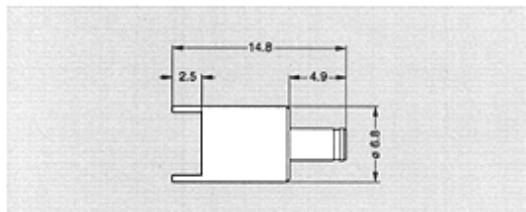
Models

Δ The reference given below are preliminary and are subject to change



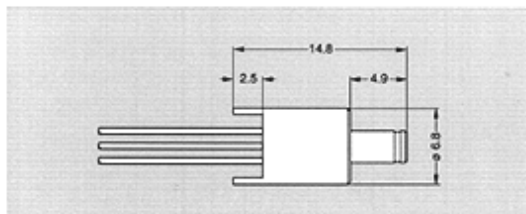
Straight plug

Part Number	Fibre type	Weight (g)
FGG.RD.UKE.143.002	9/125 singlemode	< 0.2
FGG.RD.UKE.143.003	50/125 multimode	< 0.2
FGG.RD.UKE.143.004	62.5/125 multimode	< 0.2
FGG.RD.UKE.143.005	100/140 multimode	< 0.2
FGG.RD.UKE.143.006	200/280 multimode	< 0.2



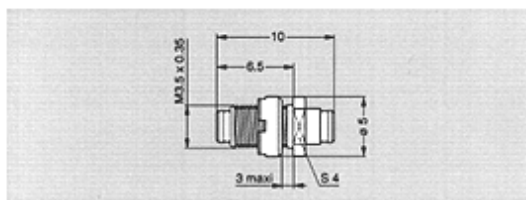
PCB Fixed socket for active device

Part Number	Weight (g)
UKE.143.A12.001	*



PCB Fixed socket fitted with Honeywell DT 200-42F active device

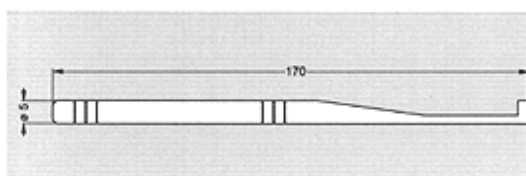
Part Number	Weight (g)
EZG.RD.UKE.143.002	*



Straight fixed coupler

Part Number	Weight (g)
RAD.RD.UKE.143.001	< 0.7

Accessory



Insertion/extraction tool

Part Number	Weight (g)
UKE.143.A15.001	22.5

Note:
This tool also serves as a spanner for the round nut on the coupler.

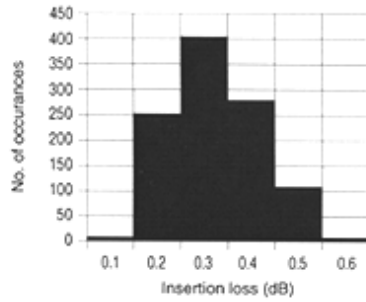
Fig. 16 RD12 Connector family models and dimensions



Technical Characteristics

Optical Performance

Multimode insertion loss



Std Deviation = 0.09 dB
Mean = 0.27 dB
Fibre = 50/125 µm

Materials and Treatment

Component	Material (Standard)	Surface treatment	
		Cu	Ni
Plug latching shell	PEEK	without treatment	
Coupler outer shell	St. steel (AISI 303)	without treatment	
Socket shell	ARCAP	without treatment	
Ferrule and sleeve	Ceramic	without treatment	
Ferrule holder	St. steel (AISI 303)	without treatment	
Round nut	St. steel (AISI 303)	without treatment	
Spring	Stainless steel	without treatment	

Mechanical Performance

Characteristic	Value	Change in insertion loss	Notes
Endurance	< 30 cycles	< 0.15 dB	
Shock	100 g, 10-50 ms	< 0.30 dB	
Vibration	According to document No. DO 160C figure 8-4, Curve "V" Standard sinusoidal vibration test curves for equipment installed in helicopters.	< 0.15 dB	
Vibration	According to Boeing Specification D200Z001 "Gaussian random vibration test" 5 hours per axis category C.	< 0.15 dB	

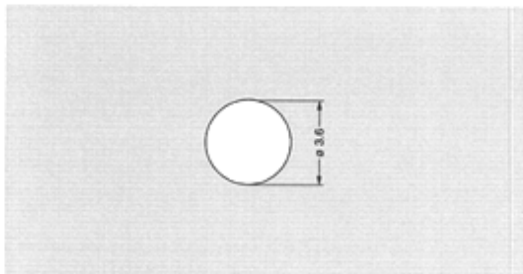
Environmental Performance

Characteristic	Value	Change in insertion loss ¹⁾	Notes
Life test	100 hrs @ -55°C	< 0.20 dB	
Life test	1000 hrs @ 125 °C	< 0.15 dB	
Temperature cycling	-55 to +90°C	< 0.20 dB	25 cycles
Humidity	Up to 95% at 60°C	< 0.20 dB	

Note: ¹⁾ the insertion loss variations were measured during the entire environmental and mechanical tests respectively.

Panel Cut-Out

Coupler Panel Cut-out



PCB Drilling pattern

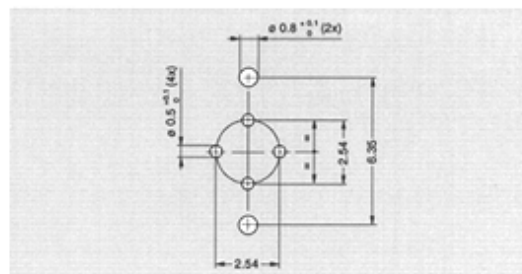


Fig. 17 RD12 Connector family performance and materials

9 Front-end electronics functional model

The detailed implementations of the proposed front-end electronics systems for LHC experiments are dictated by the requirements of the different subdetectors. They comprise specially optimised preamplifiers, unique signal-processing elements, local or remote ADCs of widely differing characteristics, analogue or digital real or virtual pipelines, and individually-tailored channel multiplexing and readout schemes implemented with a range of electronics and photonics technologies.

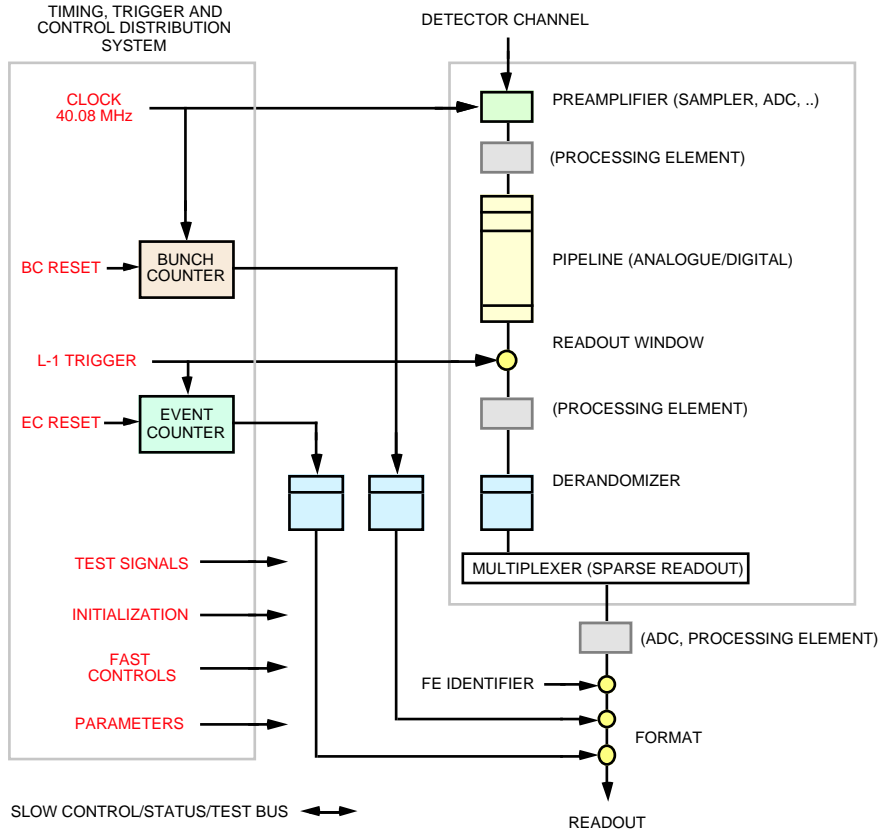


Fig. 18 Basic front-end electronics functional model

However, much of the basic functionality relevant to the TTC and DAQ systems is common to the front-end architectures. All the readouts incorporate several stages of pipelining, derandomizing, zero-suppression and signal processing, and require the 40.08 MHz LHC clock, level-1 trigger accept, initialisation, test and fast control signals, and the bunch-crossing and event numbers delivered by the TTC system. Fig. 18 illustrates a model of this basic logical functionality which can be mapped to different front-end implementations.

This common functionality makes it possible to implement a TTC system which can serve the requirements of the front-end controllers of all the different subdetectors of several LHC experiments. Only the final fanouts to the front-end electronics channels need be detector-specific. Within CMS, there is even a growing realisation

that substantial benefits would result from the use of a common front-end driver (FED) design for all subdetectors.

Since all the electronics controllers require essentially the same TTC signals, it is cost effective to develop an integrated timing receiver ASIC which can deliver them.

10 TTCrx timing receiver ASIC

As indicated in Fig. 19, the TTCrx ASIC [17], [18] accepts a single input from the TTC photodetector/preamplifier and generates a full range of decoded and deskewed signals for the electronics controllers. The ASIC comprises an analogue part (including the postamplifier, automatic gain control circuits and clock recovery/fine deskew PLL) and a digital part (including the decoding, demultiplexing, coarse deskew, bunch counter, event counter and command processing sections). Any functions not required for a particular application can be disabled to minimise the TTCrx power consumption.

With suitable logic, the receiver clock recovery function can be performed by a charge pump PLL with voltage-controlled delay elements. With this technology the fine deskew of the periodic clock output can be implemented merely by the addition of a multiplexer since the loop inherently provides a full range of output phases over the bunch-crossing interval. The technology is appropriate for monolithic integration without the use of any external components. A non-deskewed clock output is also provided for use by processors which cannot accept the minor duty factor distortion which occurs at the moment when the phase of the deskewed output is being changed by the selection of a new tap by the multiplexer.

The TTCrx ASIC incorporates such a multiphase clock generator and also virtual programmable-length shift registers for fine and coarse signal deskewing respectively. The fine deskew provides for phase adjustment over the 25 ns bunch-crossing interval in steps of 104 ps. The coarse delay compensation range of 16 bunch-crossing intervals (total 399 ns) allows a substantial margin beyond the possible maximum variation due to differences in time-of-flight and optical fibre path length. These functions, as well as broadcast command generation and bunch and event counter resets, are controlled by the data transmitted over the B Channel.

It is assumed that the optical fibre path lengths in the TTC distribution system will be dictated by installation convenience alone and that their propagation delays will not be known precisely. Glass optical fibre is a rather elastic medium so that, even if the fibre lengths were initially cut with precision, significant changes could occur during installation and when opening and closing the detectors. However, records may be kept so that a data base of approximate delays is available for the initial setting of the deskews before beam is available to allow more precise tuning.

The bunch counter reset signal is also provided for external use but a 12-bit counter, which delivers a unique bunch crossing number synchronously with the corresponding first-level trigger decision, is integrated on-chip. During the 2 clock cycles following a trigger accept, for which the central trigger logic (global trigger) inhibits the generation of new triggers, the corresponding 24-bit event number is delivered on the same 12 output lines as the bunch number. Unlike the bunch counter, the event counter need not be reset periodically but rolls over after every

16M events (about every 3 minutes at the expected level-1 trigger rate of 100 kHz). All the TTCrx event counters are initialised by a broadcast command and may be reset by such a command during any gap in the LHC bunch structure.

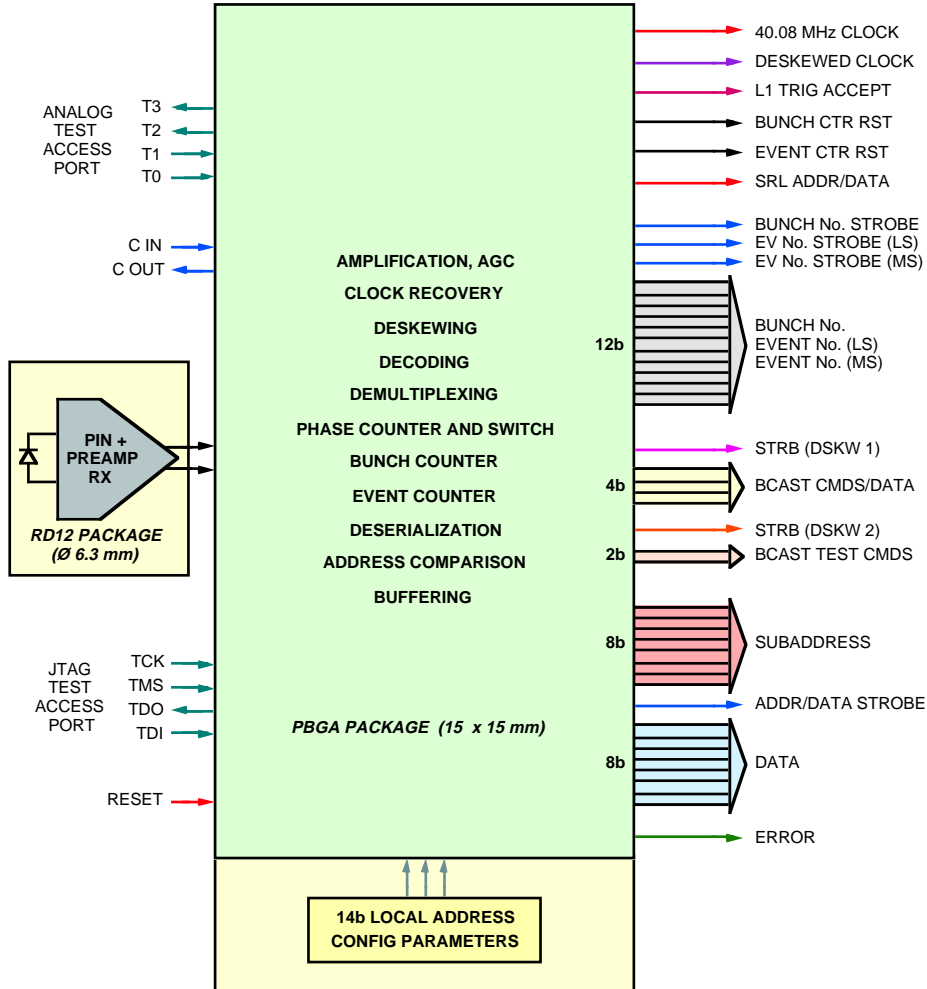


Fig. 19 TTCrx timing receiver ASIC

The 12-bit bunch number generated by the TTCrx is required by the synchronisation algorithms and permits the study of correlations between event data and the LHC orbit. The 24-bit event number suffices to detect possible problems of event ordering or loss in the data readout and event building. Additional information, rendering the event identification unique, will of course be added to the data at later stages of the DAQ chain.

The bunch counter reset, and non-periodic signals such as the trigger decision and broadcast commands, are deskewed by the timing receiver over a maximum 12-bit range; 4 bits for the number of bunch-crossing intervals and up to 8 bits for the phase within an interval. The broadcast command outputs have two independent coarse skew registers for the number of bunch-crossing intervals. This is to allow some of them to be used for the generation of test and calibration signals having different delay compensations (excluding time-of-flight but including test signal

latency, for example) without having to reload the deskew parameters used for normal running.

During 1996 a second version of the TTCrx was developed in which the L1A latency was reduced from 160 ns to 100 ns and a functional subset of the JTAG/IEEE 1149.1 standard was implemented to allow boundary-scan testing of the on-chip logic and board-level connectivity tests. This strategy may be extended to the subsystem level.

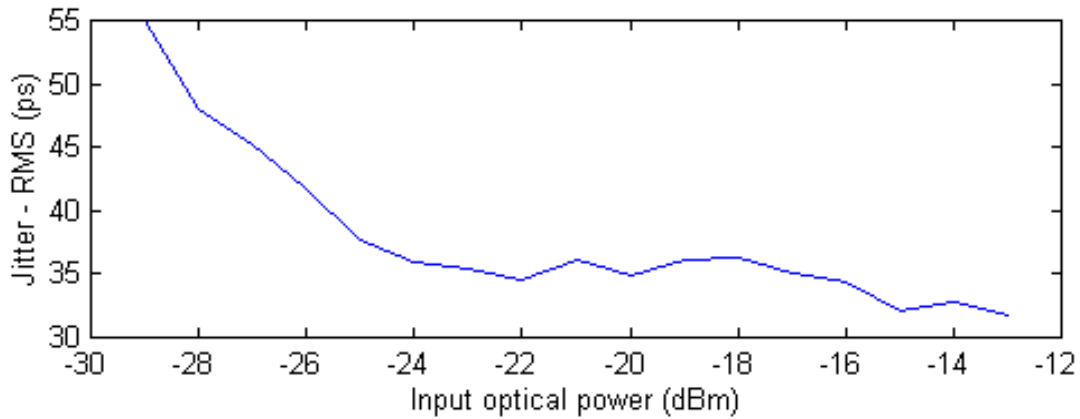


Fig. 20 Recovered clock jitter: zero clock deskew

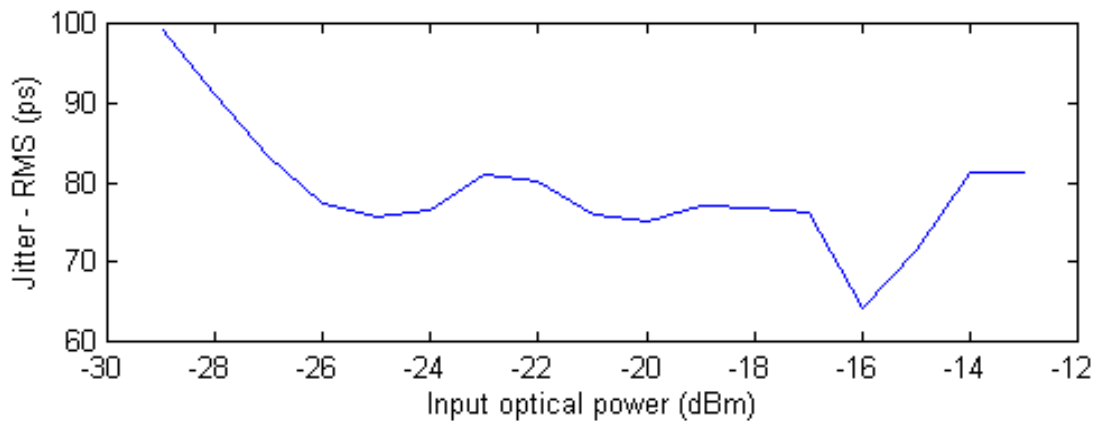


Fig. 21 Recovered clock jitter: maximum clock deskew

A number of special test functions were also provided which allow timing receiver internal parameters and the local addresses to be read back via the data acquisition system for verification. It is expected that further reductions in the L1A latency will be achieved in later versions of the ASIC.

The present chips are temporarily packaged in a large Pin Grid Array (PGA) package which has an adverse effect on the both the recovered clock jitter and the linearity of the fine deskewing. The performance obtained is indicated in Figs. 20 - 23, which show a recovered clock jitter of less than 80 ps RMS and an error of time resolution of 111 ps RMS.

By means of tests in which a chip was bonded directly to a special PCB it was verified that substantially improved performance should be achieved with smaller and lower-inductance packaging.

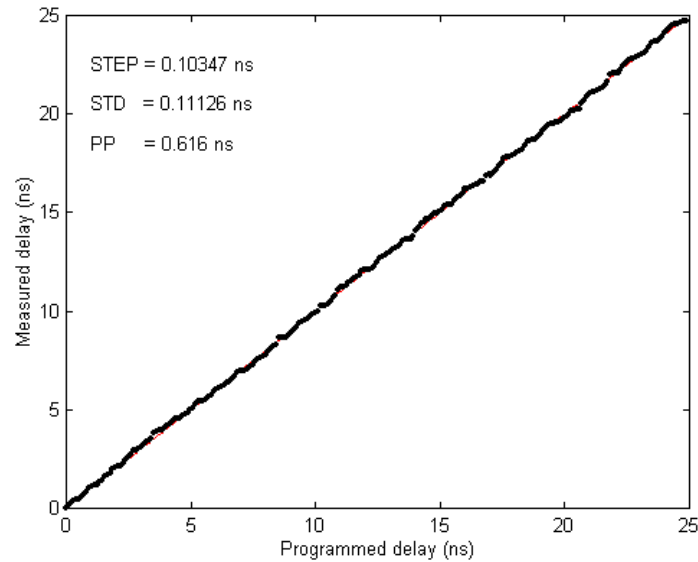


Fig. 22 TTCrx deskewing function linearity

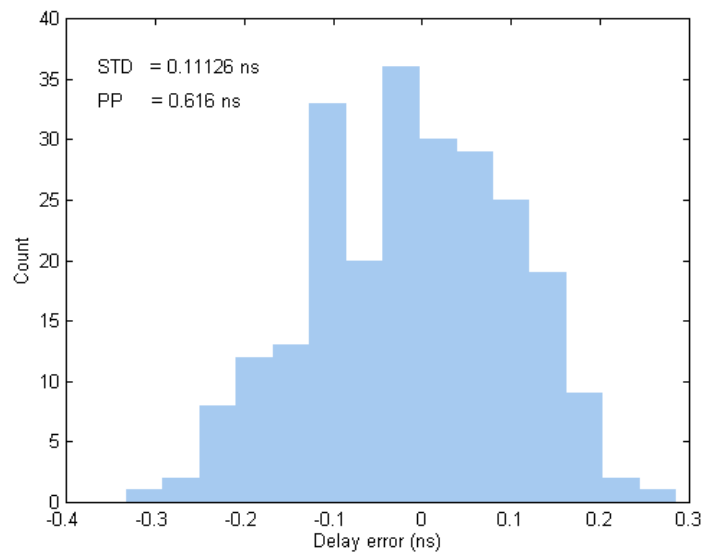


Fig. 23 Delay error histogram

A development contract was placed with a European facility of IBM to develop a 15 x 15 mm Ball Grid Array (BGA) package for the TTCrx and the first chips in the new package will be delivered 2Q97. Meanwhile a small number of ASICs in the PGA package have been supplied to the first developers who have reported applying them successfully.

At present the porting of the TTCrx design to DMILL radiation-hard technology is being studied and in order to have an early evaluation it is planned to submit some of the critical blocks of the ASIC for fabrication in a DMILL MPW run during 1997. However, a complete radiation-hard version of the TTCrx is only expected by the end of 1998. A preliminary TTCrx Reference Manual [19] is available.

11 TTCsr PMC module

In most cases TTCrx ASICs will finally be embedded directly in the electronic systems requiring the TTC signals and services. But for the convenience of users carrying out development work before such integration a TTC simple receiver (TTCsr) board is being developed as a PCI Mezzanine Card (PMC) [20]. Such a module is also required for ATLAS Level-3/DAQ prototype development and may have other applications in crate-mounted systems.

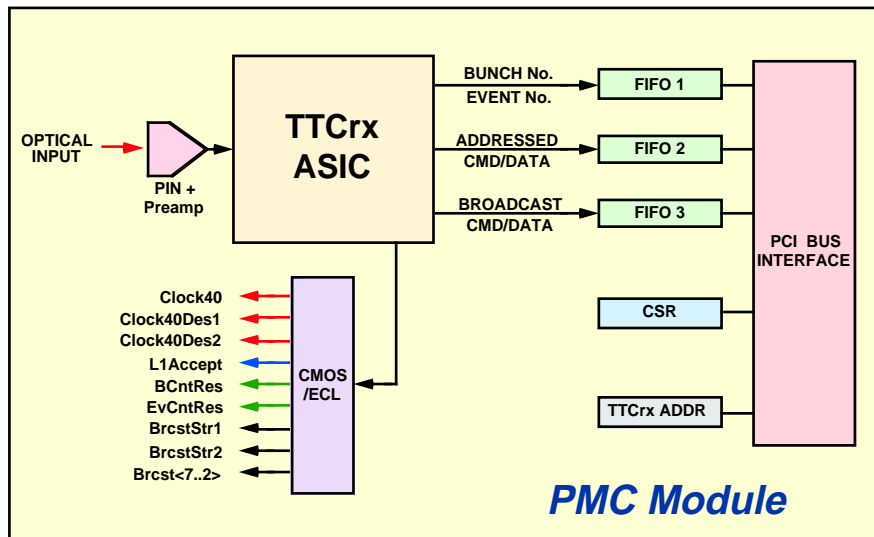


Fig. 24 TTCsr general functionality

The TTCsr provides some of the principal TTCrx signals as ECL front-panel outputs, and includes FIFOs to buffer TTCrx data to the PCI port of the module. The general functionality of the TTCsr module is indicated in Fig. 24.

The front panel signals are divided into two groups, the broadcast data and strobes being single-ended ECL and available at a 10-pin connector, while the other signals are IEC 912 differential ECL signals which are provided at a separate 12-pin connector. The different FIFOs store the data associated with each level-1 trigger, the subaddress and data of individually-addressed commands and the broadcast commands and TTCrx responses. The FIFO counters are mapped into PCI I/O space and a 32-bit control and status register provides the status of the module and allows TTCrx, FIFO and front panel functions to be controlled from the PCI bus.

The TTCsr design is based on that of the PCI-SCI [21] PMC module, a previous development with similar characteristics, in which the SCI part has been replaced by

the TTC functions. The PCI functions of the previous design, including a PCI slave and DPM controller, have been retained. A block diagram of the TTCsr module is shown in Fig. 25.

IDT7025 DPMs are used to implement the FIFOs and some of the registers, which allows faster data reading by PCI burst cycles. 4 chips are used, each providing a capacity of 16 Kbytes. The DPMs can be written 16-bit wide at 40 MHz on the TTC side and can be read 32-bit wide at 33 MHz on the PCI side.

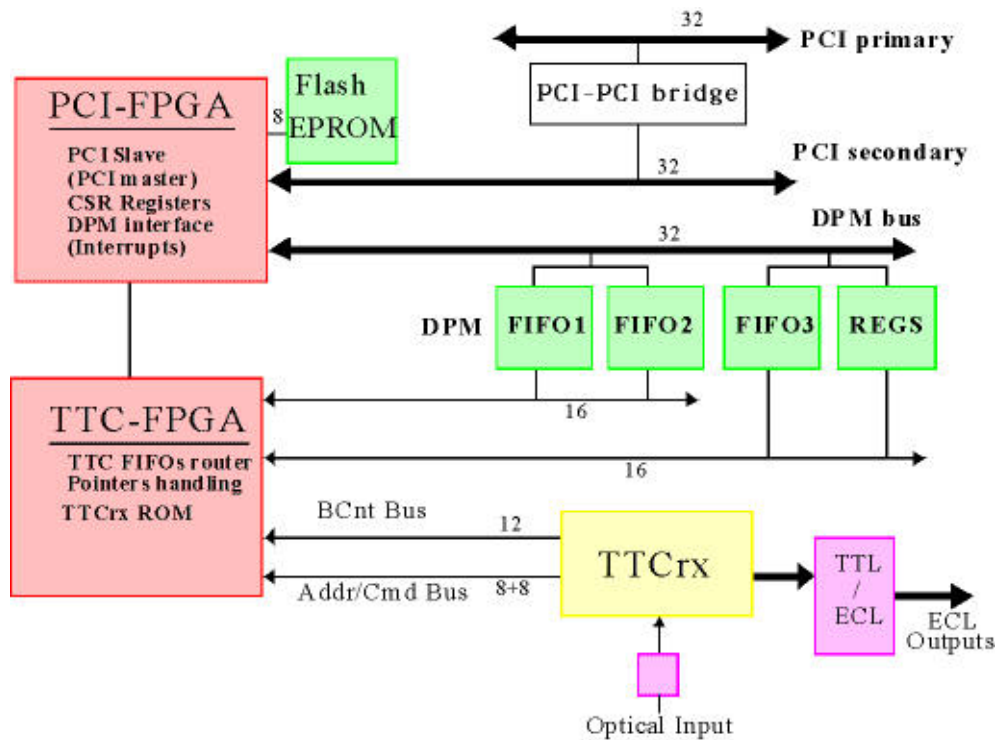


Fig. 25 TTCsr block diagram

The module incorporates two FPGAs (ORCA 2C15, 2C26). The PCI-FPGA is used for the PCI protocol and includes full PCI slave functionality, the CSR registers and the DPM control. The TTC-FPGA includes the control of the FIFOs and the routing from the 2 output buses of the TTCrx to 3 different FIFOs. During the idle cycles when the TTCrx is not dumping data it also writes the counters of the FIFOs to part of a DPM.

This operation is done using a semaphore protection mechanism that prevents the PCI side from changing the counter before the operation is finished. The functionality of the TTCrx configuration PROM is also included in the TTC-FPGA so that its contents can be changed from the PCI bus.

The TTCsr module schematic and PCB layout have been completed, the board is currently being manufactured and an initial production of 10 modules is foreseen. The programming of the PCI-FPGA has been finished and the TTC-FPGA VHDL code is in progress. The software for controlling and testing the modules will be similar to that already developed for the PCI-SCI card.

12 TTC Workshop

A one-day TTC Workshop was held at CERN on 30 October 1996 which was attended by representatives of the 4 LHC experiment collaborations, CERN management and the TTC development groups. Organisational issues were discussed, the status of the TTC technologies being developed in RD12 was reviewed, and the overall requirements and implementation plans for the TTC systems of all the experiments were presented.

It was concluded that a common approach to TTC system design is of benefit to the LHC experiments and support teams and that the RD12 Project should continue for a period to provide a framework for the required collaboration. A TTC Workshop Record [22] is available.

13 TTC integration

TTC integration work in the LHC experiments is at present only at an early stage, although a number of high power and mini-crate systems have been ordered and built for future development work. Most groups plan to accelerate this activity during 1997, when also TTCrx ASICs should be available in the final BGA package.

ALICE has particularly stringent requirements on TTC clock jitter for the Pestov counters and until the BGA-packaged TTCrx is available it is not known whether these can be met. It is planned to have an independent TTC system for each subdetector [23] and it may be possible to exploit the precise timing of the TTC clock signal to retune the early 'level-0' triggers which in this experiment must be sent by copper cables to minimise the propagation delay. It is planned to build a prototype TTC system with about 100 destinations for the setup in NA49 where a Pestov array will be installed next year.

For the different subdetectors of ATLAS it appears that the jitter performance of the current system should be acceptable. The LAr group took delivery of a mini-crate system and PGA TTCrx ASICs at an early stage and have reported successful results in exploiting them. The first application in CMS is the distribution of TTC signals to the FED boards. In this case a TTC daughter board is being designed which will support the optoelectronic receiver and TTCrx and distribute the signals to the other ASICs on the board. For this application the serialised output from the TTCrx will be used to reduce the number of bus lines required on the FED. At a later stage the FED may be implemented as a large specialised PCI carrier with all the different subfunctions such as TTC implemented as PMC modules on it.

In FERMI [24] the TTCrx will be interfaced to the clock manager ASIC which delivers all the required timing signals to the other ASICs of the microsystem. A method for the synchronisation of the trigger data is being studied [25]. For the inner tracker an extension of the TTC system is being designed to transmit the signals to a reduced-functionality receiver at the front-end electronics, where low mass and power consumption are particularly critical. A special coded serial output has been provided in the TTCrx to drive this.

LHC-B will have four levels of triggering, of which two will be implemented in hardware [26]. In addition to the clock, it is proposed to use the TTC system to distribute the level-0 decision on the A Channel at a rate of up to 1 MHz [27]. Protocol options and the trigger processing time distribution are being studied to evaluate whether the level-1 data could be broadcast on the B Channel.

14 Conclusion

The development of TTC systems for the next generation of collider experiments presents a number of challenges in the areas of high-power laser transmitters, encoders and modulators, interface design, passive optical couplers, low-cost sub-miniature optoelectronic receivers and VLSI microelectronics. These challenges are being tackled in the RD12 Project by a collaboration of CERN groups, associated research institutes and industrial partners.

It has been shown that it is possible to multiplex and encode the first-level trigger decisions, broadcast commands and individually addressed controls and data for optical transmission to over one thousand electronics destinations per laser source. The bunch-crossing timing reference can be recovered from the received data stream with a time jitter smaller than the spread in event origin time due to the LHC bunch collision length and expected longitudinal phase modulation of the circulating beams. System synchronisation can be adjusted by transmitting deskew parameters to the timing receivers over the distribution network itself.

For LHC detectors these facilities can be implemented with the relatively low transmission rate of 160.32 MBaud, permitting the use of photodetectors manufactured in increasingly large volume for the expanding LAN market. Prototype high power laser transmitter subsystems have been developed as well as compatible lower-cost mini-systems for use by electronics designers in their laboratory development work.

A VMEbus interface for the system is being developed which provides facilities for trigger source selection and emulation and generates the synchronous command sequences with the appropriate phase relative to the LHC orbit.

A new subminiature optical fibre connector family has been developed and is being introduced commercially. The family includes an active device mount incorporating a photodetector and preamplifier which have survived irradiation tests to 20 MRad. Prototype timing receiver ASICs have been fabricated and a special BGA package is being developed for them which should result in performance improvements as well as smaller size. A PMC module is being designed to assist timing receiver integration work.

Preliminary specifications and user manuals for the different components of the TTC system have been produced. Together with further regularly-updated information these are available on the Web at <http://www.cern.ch/TTC/intro.html>.

There is general agreement by the LHC experiment collaborations that a global solution to TTC system design is of benefit to all parties and the first steps towards integration of the RD12 system in the different experiments have already been taken. However, it is probably useful to maintain the project structure for a further year to provide a framework for the common development work and to ensure that the

present fruitful collaboration continues. On the assumption that equipment delivered by the Project to the experiment teams will be paid for by the latter, a budget allocation of CHF 150K will be sufficient to fund the RD12 Project developments during this period.

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