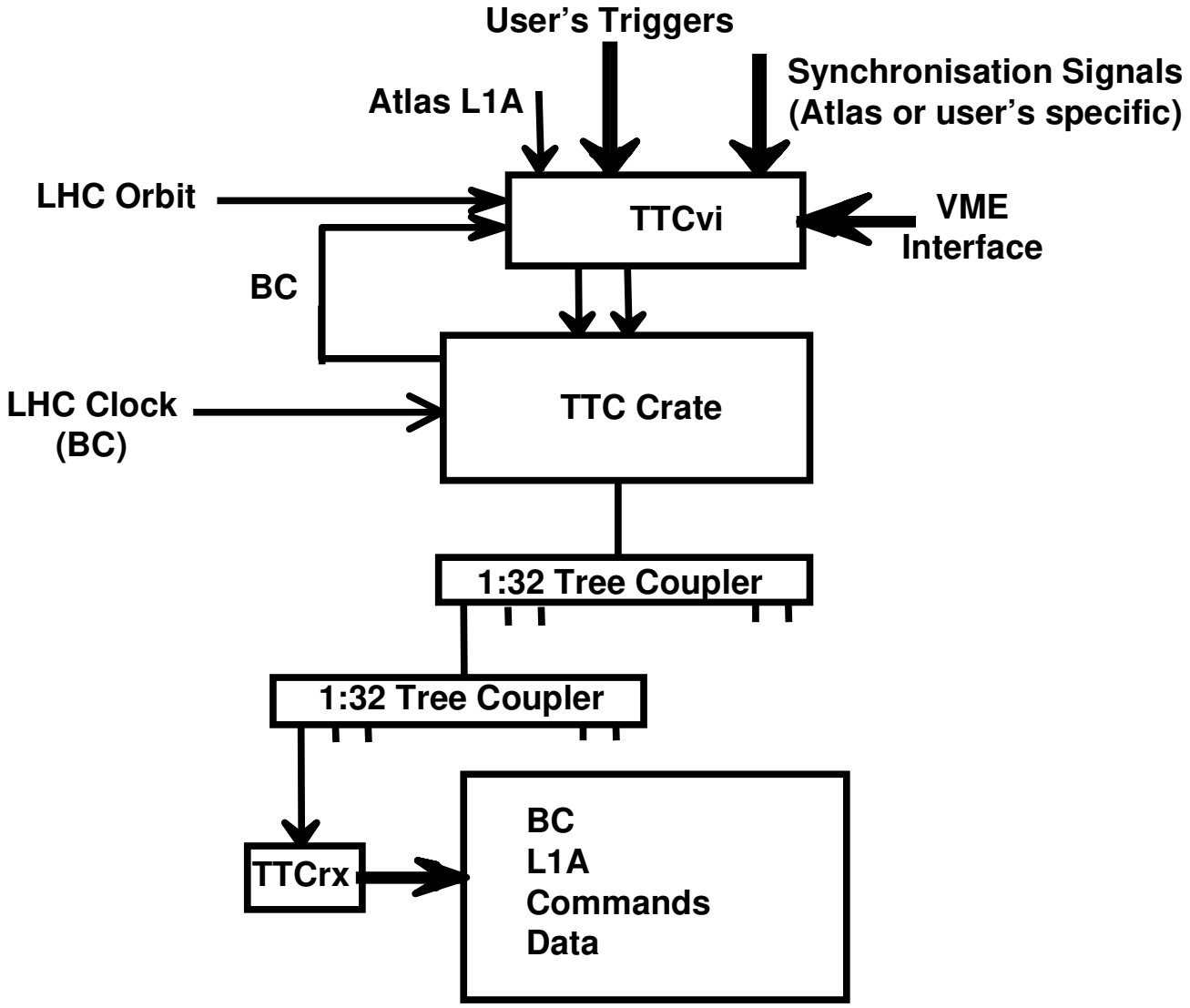
Timing, Trigger & Control

- Role of the TTC
- Partitions
- Backbone components
- Timing adjustment
- Latency
- Conclusions and requests

Role of the TTC

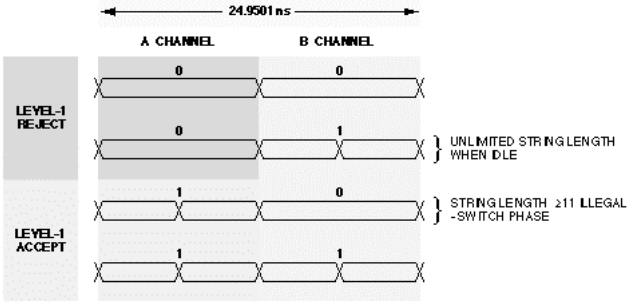
- During physics runs
  - Distribute the BC clock and the L1A signal to the read-out electronics
  - Make available BCID, EVID and Trigger_type to the read-out electronics
  - Make available any test or calibration signals
- During calibration or test runs
  - Distribute test or calibration triggers
  - Independent partitions
- Timing adjustment and synchronisation tools
  - Fine adjustment
  - Delay within the LHC cycles

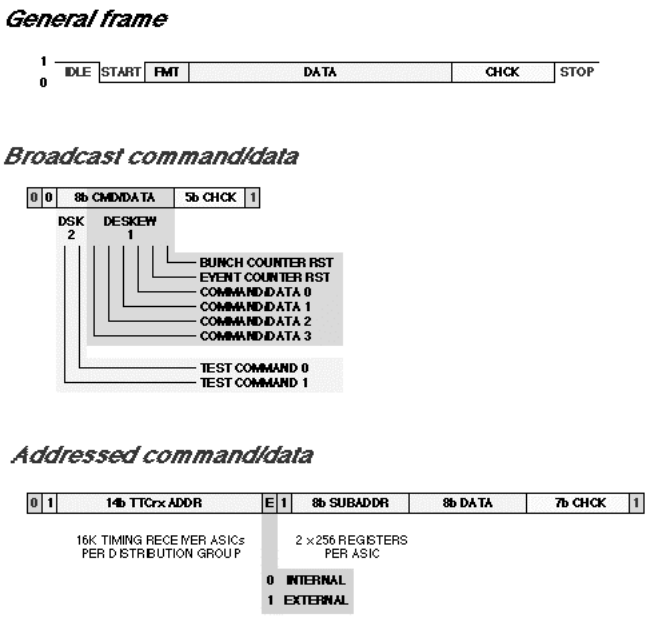
RD12 TTC Backbone



- 1 to N (< 1024) distribution
- Optical tree fan-out
- L1A and commands/data transmission

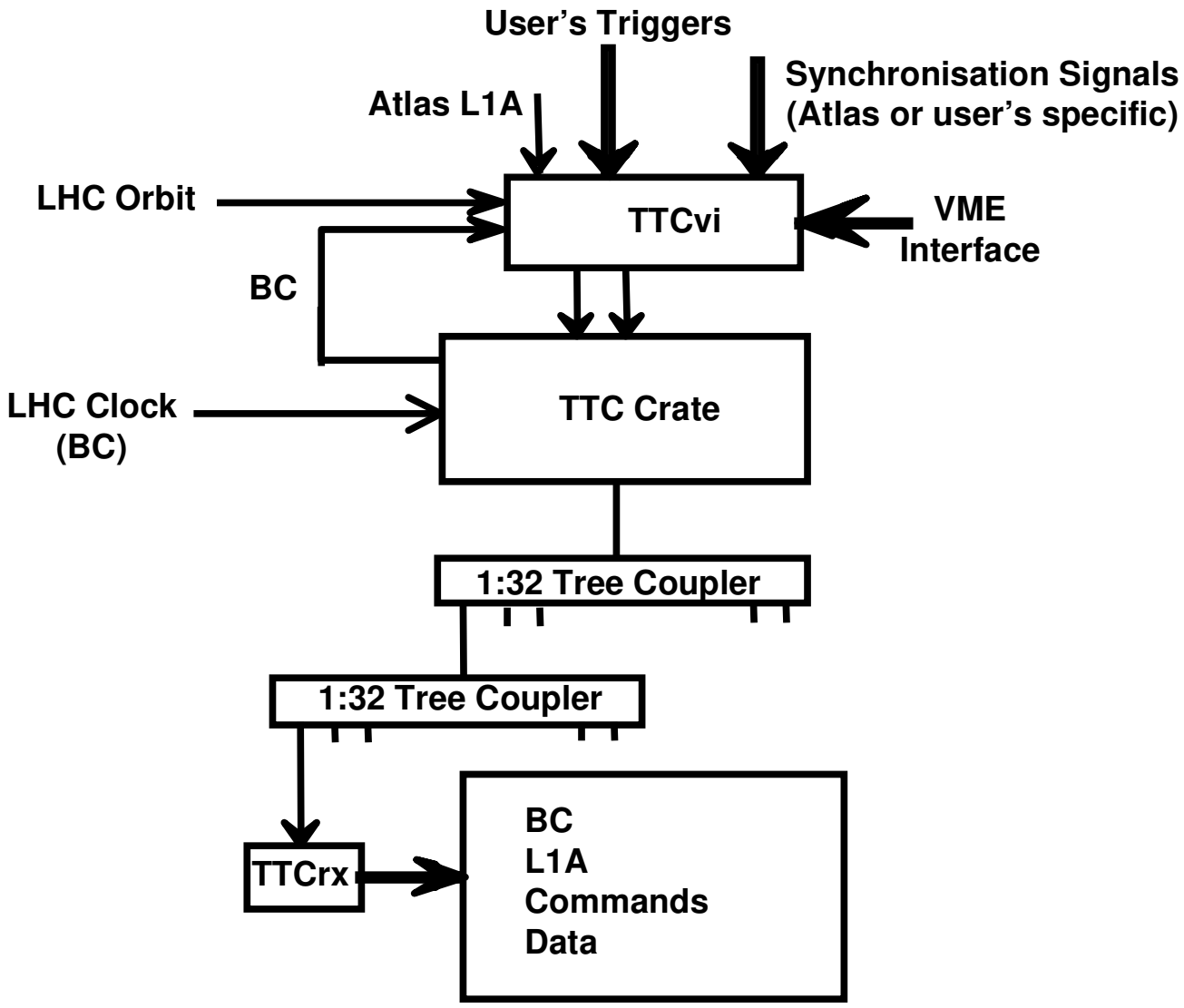
RD12 TTC Backbone



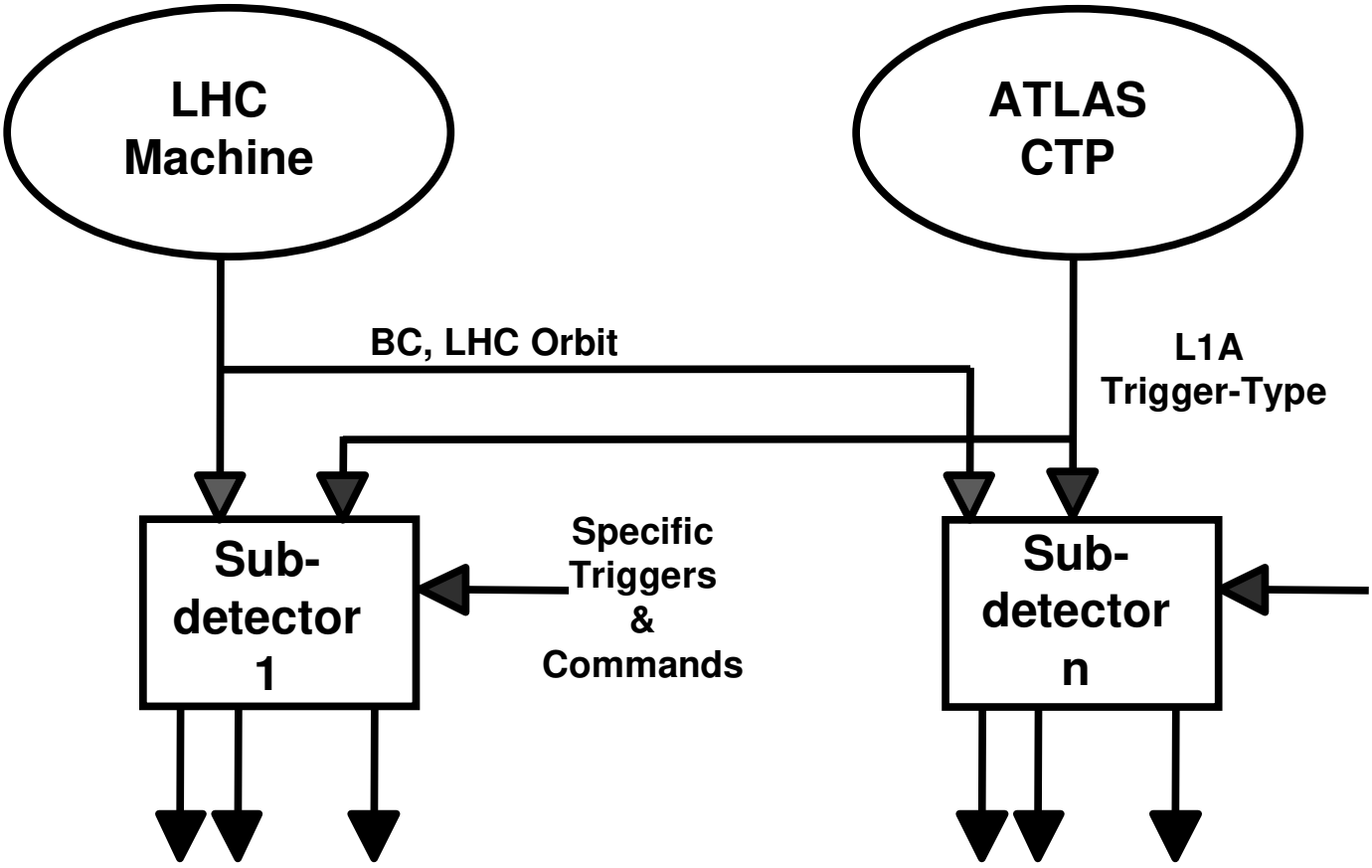


- Simultaneous L1A and Commands/data transmission
- Data cycles
  - Trigger-type
- Commands
  - Bunch Counter Reset
  - Test signal

Partition

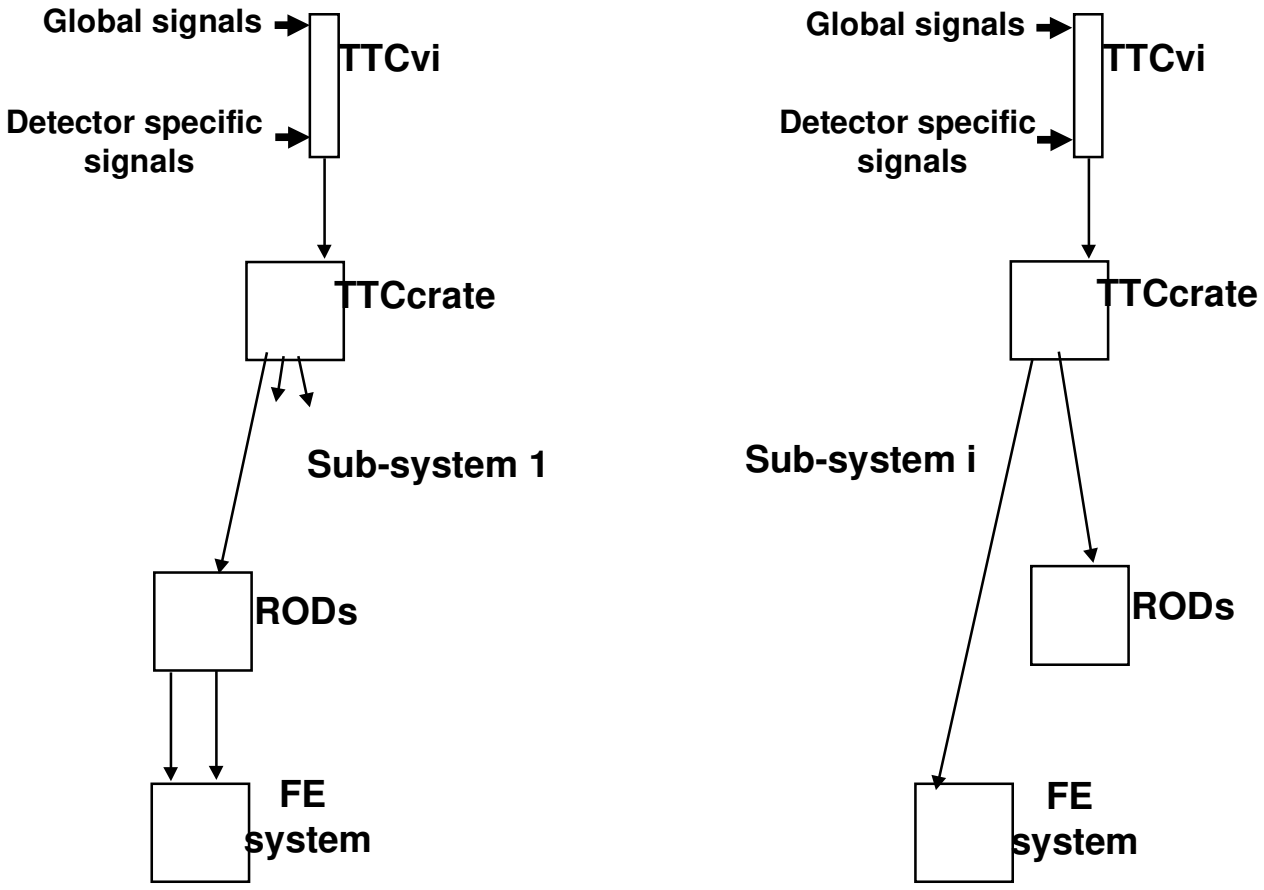

User's Triggers
Atlas L1A
Synchronisation Signals
(Atlas or user's specific)
LHC Orbit
TTCvi
VME
Interface
BC
LHC Clock
(BC)
TTC Crate
1:32 Tree Coupler
1:32 Tree Coupler
TTCrx
BC
L1A
Commands
Data

Partitions (1)



- Sub-systems need to work independently
- Each sub-system requires sub-partitions

Partitions (2)



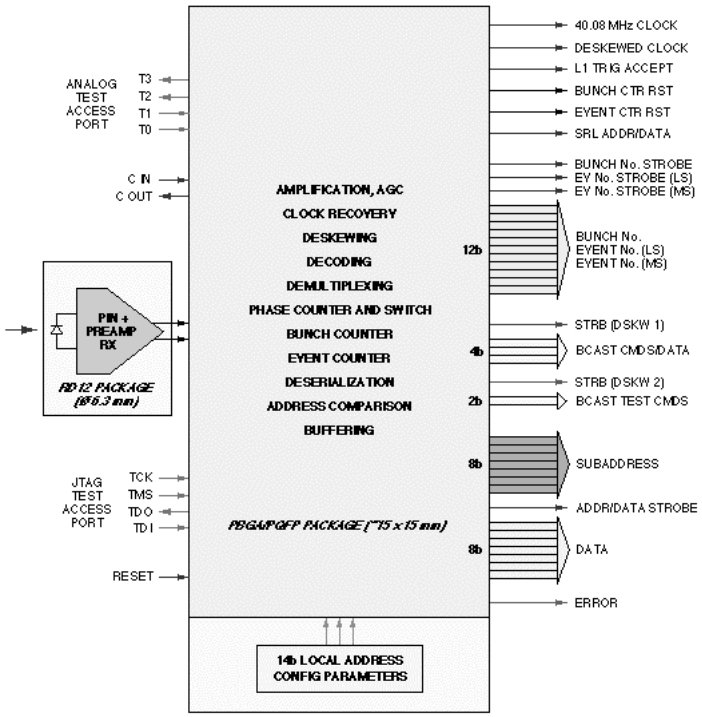
- TTC partition can be stopped at different places

Partitions (3)

System	*Number of partitions*	*Remarks*
Pixel	**2(?)**	**To be defined**
SCT	**4(?)**	**To be defined**
TRT	**4**	**End-cap & Barrel / Left & Right**
EM Larg	**4(?)**	**To be defined**
HEC	**2**	**End-cap Left & Right**
Tile calorimeter	**4(?)**	**To be defined**
Forward calorimeter	**2**	**End-cap Left & Right**
TGC	**2**	**End-cap Left & Right**
RPC	**2**	**Barrel Left & Right**
MDT	**4**	**End-cap & Barrel / Left & Right**
CSC	**2**	**End-cap Left & Right**
Level-1 calorimeter	**1 (?)**	**To be defined**
Level-1 muon	**1 (?)**	**To be defined**
DAQ/Level2	**(?)**	**To be defined**

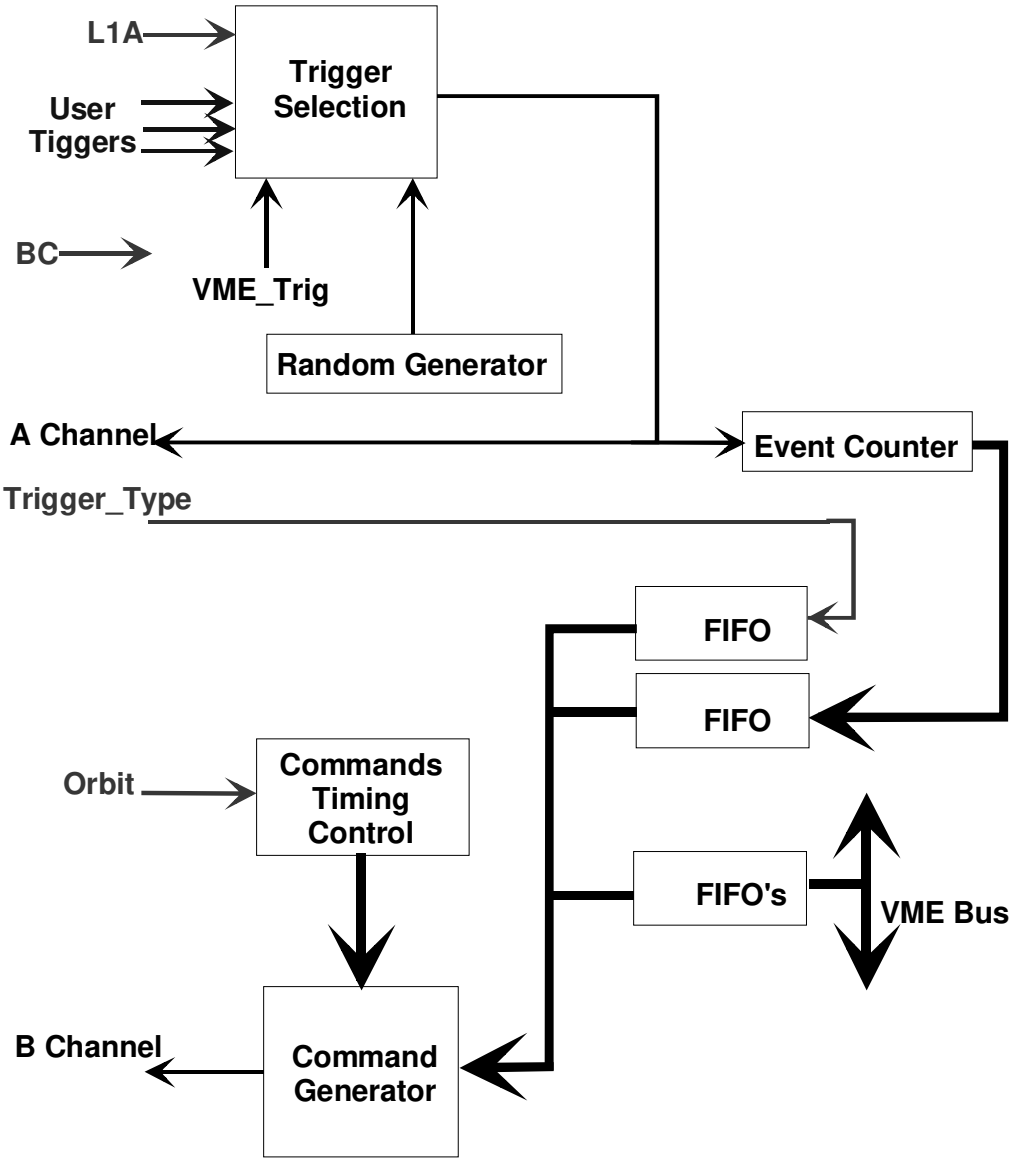
- Costing model
- Feed-back needed

Backbone Components: TTCrx



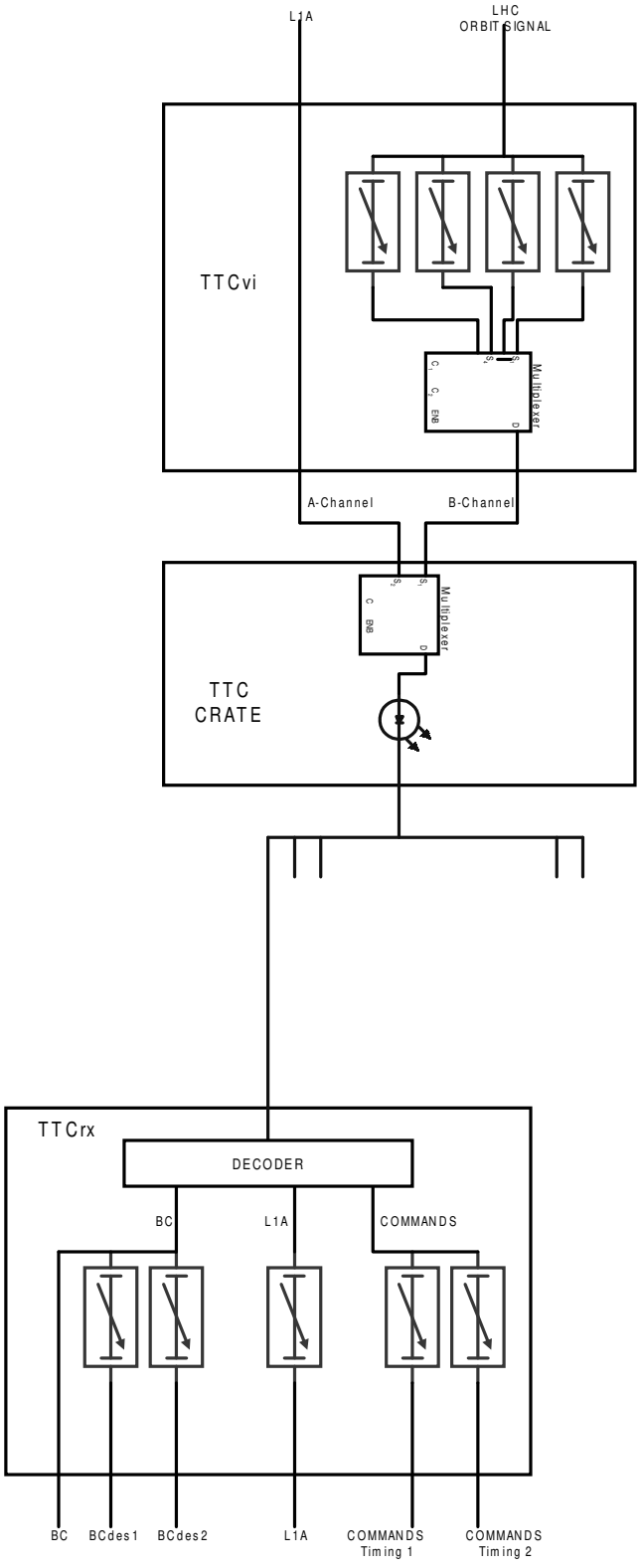
- Rad-hard ASIC
- BC extraction (timing adjust.)
- L1A extraction (timing adjust.)
- BCID and EVID
- Commands (timing adjust.)
  - e.g. Bunch Counter Reset
- Address/data
  - e.g. Trigger-Type
- I2C interface

Backbone Components: TTCvi



- Trigger selection
- Command/data generation
- Synchronisation within the LHC cycle

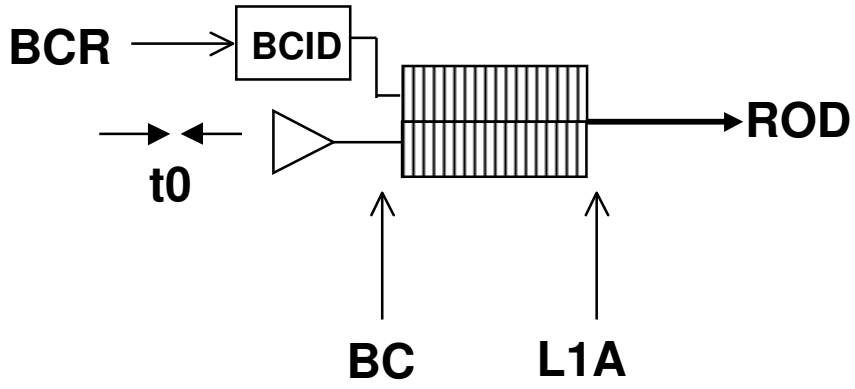
Timing Adjustments (1)



- 4 delays elements allowing to define the timing of the TTC commands with respect to the LHC cycle

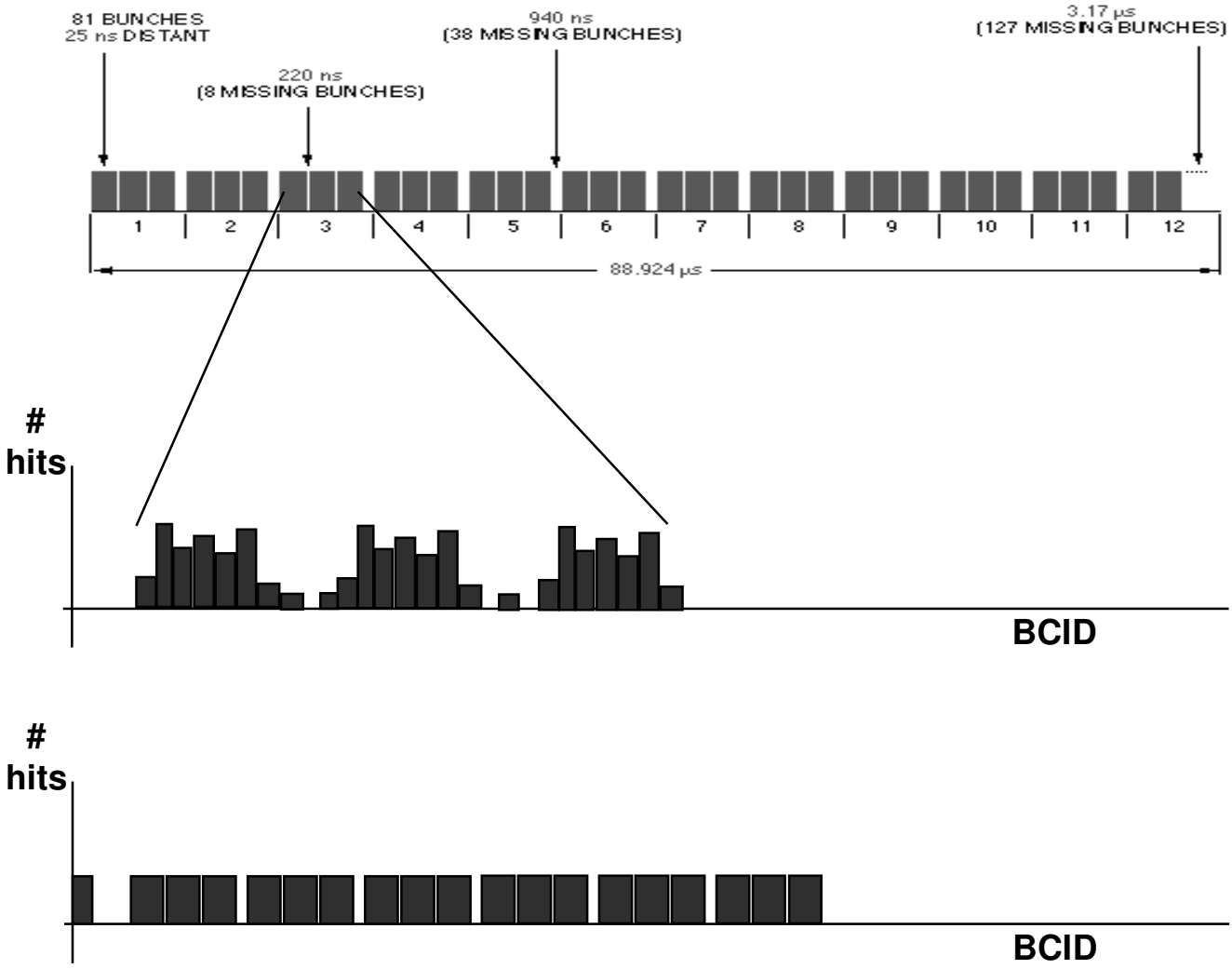
- 2 fine delay elements on BC (0-25 ns with 100 ps steps)
  - Allow fine adjustment of the local BC phase
- 1 delay element on L1A (0 to 16 BC)
  - Allows to adjust the L1A latency with respect to the front-end pipeline length
- 2 delay elements on commands (0 to 16 BC)
  - Allow to adjust the local command phase within the LHC cycle (to be done for instance for the BCR)

Timing Adjustments (2)

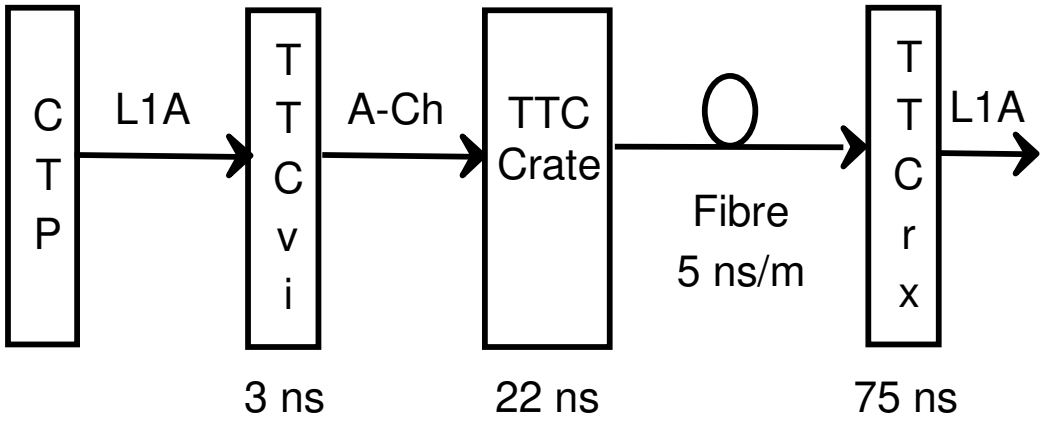


- Fine BC adjustment
  - Random Trigger
    - Peak position or Histogram of signal timing or ...
    - Adjust BC
- BCR adjustment
  - Random Trigger
    - # of hits versus BCID (--> picture)
    - Correlate with the LHC structure
    - Adjust BCR to have structure coincidence
- L1A adjustment
  - Trigger at a given BC
    - Read-out BCID
    - Adjust L1A delay to get the correct BCID

Timing Adjustments (3)



Latency



Element	*Delay*	*Remark*
CTP-TTCvi	50 ns	Cable and fan-out
TTCvi	3 ns	3 ECL stages
TTCvi to TTC crate	3 ns	Cable
TTC crate	22 ns	Modulator etc…
Fibre	400 ns	80 m
TTCrx	75 ns	Receiver
Total delay excluding cables and fibres	**100ns**	**TTCvi + TTC crate + TTCrx**
Total Latency	**553 ns**	**About 21 BC**

- Total latency depends on the location of the different elements

Conclusions and Requests

- It is expected to have all the necessary tools to distribute timing and trigger
- This review should give valuable feed-back
  - Partitioning
  - Functionality
- Sub-systems to provide a timing set-up strategy:
  - BC adjustment,
  - Bunch counter reset adjustment to make sure that the bunch crossing identifier has the proper value
  - L1A timing to accommodate the level-1 pipeline depth