ATLAS-DAQ-NO-xxx
18 Feb. 98

# Trigger, Timing & Control System (TTC) (User) Requirements Document

## (DRAFT version 0.2)

**Abstract**

To be written.

## DOCUMENT HISTORY

| Version | Date | Editor | Comments |
|---|---|---|---|
| Draft 0.1 | 29/1/98 | Ph. Farthouat | First draft version. |
| Draft 0.2 | 18/2/98 | Ph. Farthouat | First Nick's comments implemented. |

## NOTES OF THINGS TO BE ADDED

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# INTRODUCTION

## Purpose of the Document

This document gives a functional specification of the Trigger, Timing and Control system (TTC). It serves as a checklist to make sure that issues get discussed before decisions are made and will make it easier to document the decision-making process.

## Scope of the Document

The document specifies the required functionality of the TTC system, without going into details of the implementation. Note that the interface between Front-End electronic systems and the DAQ is already specified [1].

## Definitions and Acronyms

| | |
|---|---|
| BC | The 40 MHz clock, linked to the LHC machine, used to synchronise the pipelined processing system. |
| CTP | Central Trigger Processor — electronic system that accepts inputs from the muon and calorimeter level-1 trigger processors and forms the global (yes/no) level-1 trigger decision for each bunch crossing. |
| DAQ | Data acquisition. |
| L1MT | Level-1 muon trigger (system). |
| LVL1 | Level-1 or level-1 trigger. |
| LVL2 | Level-2 or level-2 trigger. |
| L1A | Level-1 accept signal [1]. |
| ROB | Read-Out Buffer [1]. |
| ROD | Read-Out Driver [1]. |
| ROD_BCID | Number provided by TTC system, used to tag event fragments; corresponds to bunch number in the LHC machine. |
| ROD_L1ID | Number provided by TTC system, used to tag event fragments; event number defined by counting LVL1 trigger signals. |
| TTC | Trigger, Timing and Control. |
| URD | User Requirements Document. |
| URL | Universal Resource Locator (address used by WWW). |
| WWW | World-Wide Web. |

## References

[1] FE interface requirements document, ATLAS-DAQ-NO-049 (see WWW for latest revisions, URL= http://atlasinfo.cern.ch/Atlas/GROUPS/DAQTRIG/FRONTEND/fe.html).

## Document Overview

This document is organised as follows. The present section (Introduction) gives a very brief account of the purpose and scope of the document, defines terms and acronyms, lists cited documents and explains the structure of the document. The following section (General Description) gives a “plain-English” description of the functional requirements of the TTC system. The final two sections set out in more formal way requirements on the TTC system.

# General Description

## System Description

To be written.

## User Characteristics

One can identify several classes of user:

1) The electronics experts, who will design, build and commission the system, and make upgrades if necessary.

2) The hardware experts who will maintain the system *in situ* during the life of the experiment.

3) The software experts who will develop and maintain the code necessary to operate the equipment in the experiment; software includes diagnostic and test programs, and calibration, control, readout and monitoring programs, as well as off-line programs.

4) The shift operator who will interact with the system via the run-control system.

## Specific Requirements

General Requirements

TTC_GE_ The TTC system shall distribute to the read-out systems (front-end electronics, RODs crates, ROBs crates) the BC signal.

TTC_GE_ The TTC system shall distribute to the read-out systems (front-end electronics, RODs crates, ROBs crates) the L1A signal.

TTC_GE_ The TTC system shall distribute to the read-out systems (front-end electronics, RODs crates, ROBs crates) all other signals or commands necessary.

Note 1: for instance calibration signals.

Note 2: the maximum number of signals and commands must be specified.

TTC_GE_ The TTC system shall allow the broadcast of synchronous signals or commands with respect to the LHC cycle (figure 1).

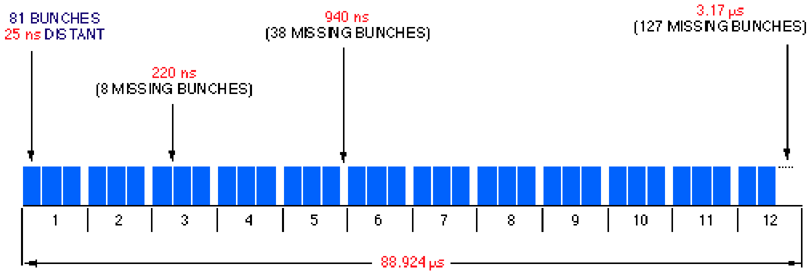


Figure 1 LHC cycle

Note: A synchronous command or signal is a command or a signal which occurs at a known BC within the LHC cycle.

TTC_GE_ The TTC system shall allow the transmission of asynchronous data either in an individual address mode or in broadcast mode.

Note: An asynchronous data transmission is a data transmission for which no timing requirements with respect to the LHC cycle are set.

TTC_GE_ The timing of any signal shall be adjustable with respect to BC and with respect to the LHC cycle in order to be able to adjust the timing at each distribution point.

TTC_GE_ The TTC system shall allow concurrent running of different sub-systems without interference outside normal running conditions.

Note: For instance during commissioning, debug or calibration runs.

TTC_GE_ The TTC system shall allow concurrent running of different sub-systems with different timing (BC) or trigger (L1A) signals outside normal running conditions.

Note: As above.

TTC_GE_ The TTC system shall allow the synchronisation of the data taking by providing a unique BC identifier (BCID) and a unique event identifier (EVID) with each L1A.

TTC_GE_ The TTC system shall allow synchronisation of the BCID's and EVID's across the whole read-out system by providing synchronous reset signals BCR and ECR.

TTC_GE_ The TTC system shall allow the transmission of an 8-bit "trigger_type" with each L1A signal.

Partitioning Requirements

TTC_PA_ A TTC partition shall consist of one source and several destinations.

TTC_PA_ The maximum number of destinations per partition is 1024.

Note: maximum number to be confirmed.

TTC_PA_ There shall be at least one partition per sub-system. The sub-systems are: Pixel, SCT, TRT, EM Larg Calorimeter, HEC, Tile calorimeter, Forward Calorimeter, TGC, RPC, MDT, CSC, Level-1 calorimeter, Level-1 muon, DAQ.

TTC_PA_ Each sub-system partition shall be further partitionable. The number of sub-partition shall be:
Pixel:
SCT:
TRT: 4
EM Larg:
HEC: 2
Tile calorimeter:
Forward calorimeter:
TGC: 2
RPC: 2
MDT: 4
CSC: 2
Level-1 calorimeter:
Level-1 muon:
DAQ:

Note: the exact number to be quoted by each sub-system.

TTC_PA_

Source Requirements

TTC_SO_ A TTC source shall allow the selection of the clock used. There shall be at least 2 clock sources out of which one is the LHC clock.

TTC_SO_ A TTC source shall allow the selection of the L1A signal used. There shall be at least 4 L1A sources out of which one is the ATLAS L1A signal coming from the CTP.

TTC_SO_ A TTC source shall allow the generation of a L1A under computer control.

Note: For instance with a write access at a key location.

TTC_SO_ The clock and L1A source selection shall be done without cabling or de-cabling operations and without any other manual interventions.

Note 1: It is envisaged to put the TTC source at high voltage to avoid any stupid guy to change the cabling.

Note 2: note 1 to be confirmed.

TTC_SO_ A TTC source shall allow the transmission of synchronous broadcast commands. These commands are encoded in an 8-bit word.

TTC_SO_ The phase of the synchronous commands with respect to the LHC cycle shall be programmable.

TTC_SO_ The synchronous commands shall be sent in response to either a computer action (e.g. write operation at a key location) or an external signal.

TTC_SO_ The following commands are mandatory: Bunch Counter Reset (BCR), Event Counter Reset (ECR) and Reset.

TTC_SO_ The TTC source shall allow the generation of periodic commands, i.e., which are repeated at each LHC cycle.

Note: for instance BCR.

TTC_SO_ The TTC source shall allow the generation of command sequences.

Note: for instance test-pulse followed by a trigger.

TTC_SO_ A TTC source shall allow the transmission of asynchronous data cycles individually addressed to a given destination. There shall be 15-bit address and 16-bit data.

TTC_SO_ A TTC source shall allow the transmission of asynchronous data cycles broadcasted to all destinations. The 15-bit address shall be 0.

TTC_SO_ A TTC source shall allow the transmission of an Event Number with each L1A.

Note 1: This is in addition to the Event Number generated at the receiving end.

Note 2: May be used for additional checking.

Note 3: To be confirmed.

TTC_SO_ The Event Number shall be a 24-bit identifier.

Note 1: to be used as check tool in the RODs.

Note 2: to be confirmed.

TTC_SO_ The Event Number shall be available in the destination at most 10 microseconds after the L1A has been transmitted when the previous L1A was issued at least 10 microsecond before.

Note 1: to make sure that this information is available in the ROD's when the front-end data of a given L1A arrive.

Note 2: the 10 microseconds need to be confirmed. It is the maximum time allowed to readout the data from the front-end at 100 kHz L1A rate.

TTC_SO_ The TTC source shall accept an 8-bit trigger-type word from the CTP with the L1A and transmit it to the destinations.

Note 1: sub-detector to tell what they want to do with the event-type.

Note 2: trigger-type size to be confirmed.

TTC_SO_ The trigger-type shall be available in the destination at most 10 microseconds after the L1A has been transmitted when the previous L1A was issued at least 10 microsecond before.

Note: same as for Event Number.

TTC_SO_ The latency introduced on the ATLAS L1A shall not exceed 2 BC. This time is taken from the L1A input of the TTC source to the L1A output of the distribution media (cable or fibre).

Note: to be confirmed.

TTC_SO_ The latency introduced to any synchronous commands and the L1A shall be fixed.

TTC_SO_ The TTC source shall not introduce any dead-time.

Note: it means that the encoding scheme used to transmit the L1A and the commands and data has to be done properly.

TTC_SO_ There shall be at least four clock cycles without L1A after a L1A has been received.

Note 1: the L1A source should make sure that these 4 empty BC are introduced.

Note 2: this may simplify some part of the coding scheme and the way it is done.

Note 3: if these 4 empty BC are mandatory to have the TTC properly working, then the TTC source shall include a protection circuitry.

TTC_SO_ The TTC source settings shall be programmable through a VME interface.

Note: bus selection to be confirmed.

Destination Requirements

TTC_DE_ The TTC destination shall make available the clock signal (BC).

TTC_DE_ The TTC destination shall make available the L1A signal.

TTC_DE_ The TTC destination shall make available the BCR signal.

TTC_DE_ The TTC destination shall make available the ECR signal.

TTC_DE_ The TTC destination shall make available the synchronous 8-bit encoded commands.

TTC_DE_ The TTC destination shall make available the asynchronous data when it is addressed individually or in broadcast mode.

TTC_DE_ One shall be able to assign a unique address to each destination of a given partition.

TTC_DE_ On reception of the Reset command, the destination shall be re-initialised.

Note 1: reset all internal counters, reload address and configuration data (if any).

TTC_DE_ With each L1A, the TTC destination shall provide a 12-bit BCID and a 24-bit L1ID, internally generated.

TTC_DE_ The L1ID and BCID must be provided within 5 BC maximum after reception of L1A.

Note 1: may need to be included in the event at the front-end level and thus should be delivered during the fixed dead-time introduced after each L1A (4 BC dead after a L1A).

Note 2: making this time available may simplify the receiving circuitry for instance in allowing the implementation of a shorter width data bus to make these quantities available.

TTC_DE_ BCID should be reset on reception of the Reset command and on reception of BCR.

TTC_DE_ L1ID should be reset on reception of the Reset command and on reception of ECR.

TTC_DE_ At least 2 clock signals (BCdes1 and BCdes2) with different programmable delays with respect to BC shall be made available.

TTC_DE_ The jitter introduced on the clock signal (BC) shall not exceed 50 ps rms.

Note 1: the value of the jitter may be revisited.

TTC_DE_ The delivered clocks (BCdes1 and BCdes2) phases shall be stable within a range ±1 ns in a period of 24 hours.

Note 1: must be stable during a full physics run.

Note 2: number to be confirmed.

TTC_DE_ The delivered clocks (BCdes1 and BCdes2) phases shall be adjustable at every destination node, within a range 0-25 ns, with steps of 500 ps.

TTC_DE_ The delivered L1A signal duration shall be 25 ns.

TTC_DE_ The delivered L1A signal shall be centred on a rising edge of the delivered BCdes1 signal.

TTC_DE_ It shall be possible to delay the delivered L1A signal from 0 to 16 BC cycles at each destination node.

Note: maximum number of BC cycles to be confirmed.

TTC_DE_ The delivered ECR signal duration shall be 25 ns.

TTC_DE_ The delivered ECR signal shall be centred on a rising edge of the delivered BCdes1 signal.

TTC_DE_ It shall be possible to delay the delivered ECR signal from 0 to 16 BC cycles at each destination node.

Note 1: to be able to compensate delays and be sure the event number is reset at the same physical BC at every destinations.

Note 2: maximum number of BC cycles to be confirmed.

TTC_DE_ The delivered BCR signal duration shall be 25 ns.

TTC_DE_ The delivered BCR signal shall be centred on a rising edge of the delivered BCdes1 signal.

TTC_DE_ It shall be possible to delay the delivered BCR signal from 0 to 16 BC cycles at each destination node.

Note 1: to be able to compensate delays and be sure the bunch number is reset at the same physical BC at every destinations.

Note 2: maximum number of BC cycles to be confirmed.

TTC_DE_ The delivered synchronous encoded command bits duration shall be 25 ns.

TTC_DE_ The delivered synchronous encoded command bits shall be centred on a rising edge of the delivered BCdes1 signal or around a rising edge of the delivered BCdes2 signal in a programmable way.

Note 1: to allow for instance time scan tests.

Note 2: the way the selection is done has to be defined.

TTC_DE_ It shall be possible to delay the delivered synchronous encoded command bits from 0 to 16 BC cycles at each destination node.

Note: maximum number of BC cycles to be confirmed.

TTC_DE_ The TTC destination shall not introduce any dead-time.

Note: the L1A decoding shall not introduce dead-time.

TTC_DE_ The TTC destination shall not introduce more than 3 BC of latency between the input signal to the delivered L1A signal.

Note: this latency has to be as small as possible. The value has to be confirmed.

TTC_DE_ The latency introduced to any synchronous commands and the L1A shall be fixed.

TTC_DE_ The TTC destination shall be able to work in a radiation environment. The maximum radiation levels are 100 kRad and 10^13 N.cm^-2.

Note: These numbers correspond to the level of radiation in the Larg gap for 10 years of LHC at full luminosity. They need to be confirmed.

TTC_DE_ The TTC destination settings (delays, etc…) shall be programmable through the TTC network itself (asynchronous data cycles) and through a local access.

Note 1: this allow to program the TTC destination when it is in the on-detector electronics systems and when it is in boards accessible through a local bus (e.g. in the ROD’s).

Note 2: the local access may be JTAG, I2C or any convenient interface.

TTC_DE_ The TTC destination settings should be readable through the local access.

Control Requirements

TTC_CO_ There shall be a way of detecting transmission errors between a source and destinations.

TTC_CO_ Each destination shall implement an error counter, which is incremented, each time an error is detected.

TTC_CO_ The error counters shall be reset upon reception of the Reset command.

TTC_CO_ The error counters shall be readable.

TTC_CO_ Any programmable setting in both TTC source and destination shall be readable.

TTC_CO_ The maximum allowed BER is 10^-14.

Note 1: assuming 1 bit transmission for the L1A and 8-bit transmission for the BCR (which are the most critical parts), 1000 destinations, a L1A rate of 100 kHz and a run duration of 4000 s, this BER would mean 4 10^-3 error on L1A transmission and 3.6 10^-3 error on BCR transmission per run.

Note 2: to be confirmed.

Physical Requirements

TTC_PH_ The power consumption of the TTC destination has to be kept as low as possible. It should not exceed 500 mW per destination.

Note: to be confirmed.

TTC_PH_ The size of the TTC destination has to be kept as small as possible. It shall not exceed 4 x 4 x 1 cm^3.

Note: to be confirmed.

Requirements on external systems

TTC_EX_ The LHC clock (BC) shall be made available by the LHC machine.

TTC_EX_ A synchronisation signal arriving at a known time during the LHC cycle shall be made available by the LHC machine.

TTC_EX_ This synchronisation signal must be stable with respect to the LHC cycle within ±5 ns.

TTC_EX_ The CTP shall provide the L1A.

TTC_EX_ The L1A signal duration shall be 25 ns.

TTC_EX_ After a L1A signal there shall be 4 BC without L1A.

TTC_EX_ It is the responsibility of sub-detector community to develop a strategy for setting up the timing of their partition(s).

Note: the TTC system shall provide all the necessary tools for this operation but cannot do more.

Test Requirements

TTC_TE_ It shall be possible to test all programmable memories (registers, etc.) for data and addressing errors; for all such memories (including control registers) it shall be possible to read (non-destructively) the memory contents.

Note 1: This requirement to be discussed.

TTC_TE_ It shall be possible to complete test procedures within the following time limits: Standard test sequence in under 10 minutes; comprehensive test sequence in under 2 hours; switch from test mode back to normal mode in under 5 minutes; diagnosis of single point of failure in under 10 minutes.

Note 1: Timings need to be confirmed.

TTC_TE_ The use of JTAG (boundary scan) shall be considered for all boards and ASICs in the system.

Note 1 It may be decided to omit JTAG for reasons of cost or simplicity of the logic, but the reasons for doing so should be documented.

TTC_TE_ It shall be possible to test and to diagnose faults in the TTC system *in situ*, without having to touch the hardware.

TTC_TE_ It shall be possible to generate test signals at the input to any TTC partition to test and debug a TTC partition in isolation from the others.

Maintenance Requirements

TTC_MA_ It shall be possible to replace a faulty module in the system by a spare one, and to make a comprehensive test of the system after the repair has been made, in under two hours.

Note 1: The time allowed for making repairs is to be confirmed.

TTC_MA_ It shall be possible to replace a faulty power supply in the system by a spare one, and to make a comprehensive test of the system after the repair has been made, in under two hours.

Note 1: The time allowed for making repairs is to be confirmed.

TTC_MA_ It shall be possible to replace a faulty cable (electrical or optical) in the system by a spare one, and to make a comprehensive test of the system after the repair has been made, in under two hours.

Note 1: The time allowed for making repairs is to be confirmed.

TTC_MA_ It shall be possible to replace a cooling unit in the system by a spare one, and to make a comprehensive test of the system after the repair has been made, in under two hours.

Note 1: The time allowed for making repairs is to be confirmed.

TTC_MA_ Supplies of fully-tested spare modules, power supplies, cables, fans shall be provided at CERN for all parts of the TTC.

TTC_MA_ Test stations shall be provided at CERN to allow full and independent diagnosis, repair and testing of all TTC components.

TTC_MA_ During running, experts capable of maintaining the system shall be available at CERN.