Use of the TTC system in ATLAS

Draft

History

Version 0.	16 Mar. 98
Version 0.1	18 Mar. 98

1. Introduction

This note describes the way it is intended to use the TTC system system in ATLAS for:

- Initialisation
- Timing adjustment of the distributed clock and trigger
- Timing adjustment of the TTC commands
- Test and calibration signals transmission
- Trigger-type transmission.

In addition an example of timing set-up strategy is given.

The figure 1, shows the different delay adjustments and their location in the TTC system.

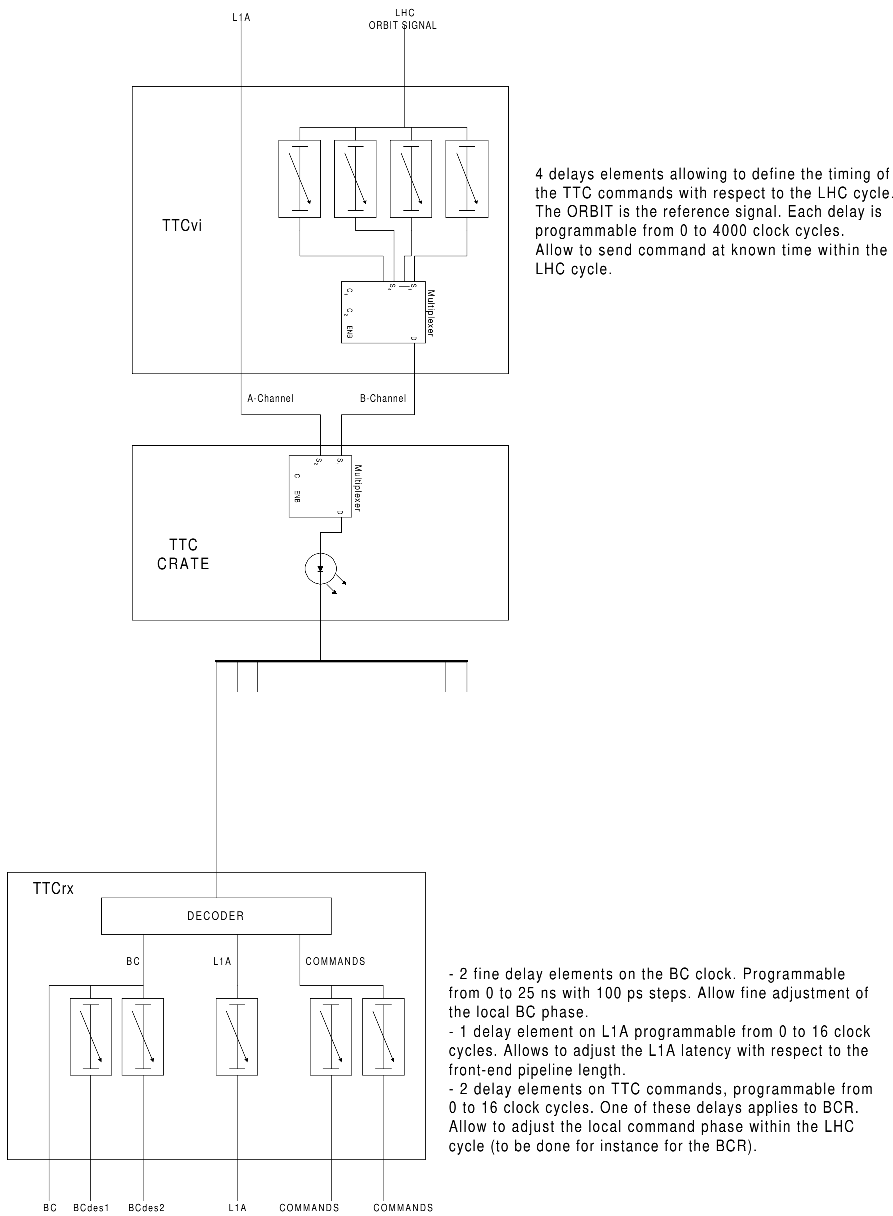

Figure 1. Delay elements in the TTC system

2. Initialisation

At the start of a run or a test or calibration period, one has to:

- Select the signals to be used (Clock, Trigger source,….) and configure other parameters in the TTCvi driving the TTC partition;
- Set all the programmable delays in the TTCrx chips.

The first operation is done through the VME interface of the TTCvi and the second can be done either through the TTC network or through the I2C interface of the TTCrx chips. This last way is probably much more convenient when the TTCrx chips are located at the RODs level: the TTCrx registers are loaded in the same way as the other registers of the read-out chain (and can be read back and checked).

3. Synchronisation

One has to consider:

- Synchronisation with respect to the LHC cycle
- Maintaining the BCID consistent across the complete experiment
- Maintaining the EVID consistent across the complete experiment.

3.1 Synchronisation within the LHC cycle

The LHC cycle is shown in figure 2. The LHC machine provides a synchronisation signal (ORBIT) which exhibits a transition edge at known time in the cycle. This signal is used by the TTCvi to build up to four internal synchronisation signals (Inhibit<3..0>). These signals allow the generation of commands (including BCR) at known times within the LHC cycle.

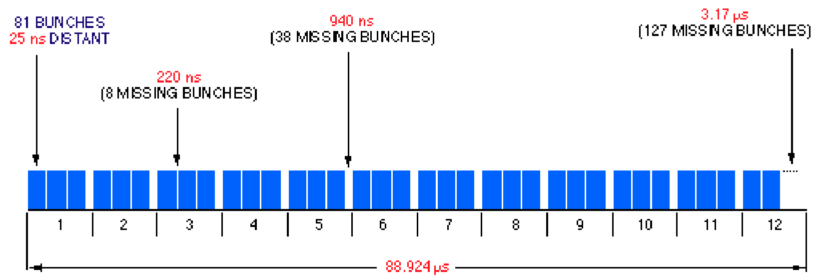

Figure 2 LHC cycle

3.2 BCID synchronisation

All the necessary tools to maintain a coherent BCID across the experiment are available.
In the TTCvi, one of the Inhibit<0> signal is devoted to the BCR command. The phase of this command with respect to the LHC cycle is properly programmed in the TTCvi. At the receiving end (TTCrx) one can locally adjust the phase of the BCR signal in the range 0-400 ns. This allows a misalignment of up to ±200 ns between the TTCrx of a given partition; this is deemed to be enough to cover differences in cable or fibre lengths or differences in time of flight in the detector.
BCR will be issued at the end of each LHC cycle in order to reset the Bunch Crossing counters in the TTCrx. BCID 0 will be allocated to the last BC of the 3.17µs gap at the end of the LHC cycle so that the LHC cycle starts with BCID 1. This choice may be subject to change if it gives raise to problems (for instance for the sub-detectors which do not use the TTC protocol up to the front-end and which cannot transmit L1A and commands simultaneously).

3.4 EVID synchronisation

The ECR signal is necessary to reset the local event number counters if necessary (e.g. if a de-synchronisation has been detected). The system must guarantee that there is no L1A during the time this signal is broadcasted to all the TTCrx. This can easily be obtained in introducing dead-time at the CTP level.

4. Test and calibration signals transmission

During test and calibration periods one has to be able to send pulses and triggers to the read-out electronics. The TTCvi allows to do so in different ways, without requiring any hardware intervention.
In addition to the ATLAS L1A signal coming from the CTP, 3 other trigger inputs are available. The test signals can be transmitted as synchronous

commands on the TTC and any one of the available B-Go<3..0> signals can be used (in this case the relative phase between the test pulse and the trigger is to be adjusted externally), or sequences of commands with timing defined by the internal Inhibit<3..0> signals can be used. In this latter case the user has to decode the TTCrx command outputs to locally generate test and trigger signals. The Inhibit<3..0> signals are available as NIM signals on the TTCvi front panel and can be used to fire external logic if needed.
The command output of the TTCrx can be resynchronised with one the 2 deskewed clocks available (Bcdesk1 and Bcdesk2). This allows for instance to have a test signal with an adjustable timing with respect to the clock used by the read-out electronics.

5. Trigger-type transmission

It is necessary to have available, with each L1A, some information of the type of trigger it is (for instance calibration, physics,…). This information may be used in the RODs. The TTCvi receives an 8-bit Trigger-Type from the CTP and transmits it to the TTCrx. This transmission cannot be in phase with L1A, as there is not enough bandwidth available to transmit this word within 5 BC (the BC of the L1A followed by the 4-BCdead-time). The Trigger-Type is transmitted in an asynchronous way when the TTC system is available (i.e. when there is no transmission of synchronous commands such as BCR). The Trigger-Type is available at the output of the TTCrx between one and two µs after the L1A has been issued, assuming there was no L1A in the previous 2 µs. In case of consecutive L1A within short period of time, the Trigger-Type transmission is queued and then the Trigger-Type of a given L1A will be available later at the output of the TTCrx. This is deemed to not be a problem as the Trigger-Type is used only at the ROD level where the event data are subject similar fluctuations in arrival time.

6. Timing set-up

It is important to be able to develop a strategy to adjust the timing of experiment with the TTC system when the beam arrives (or when one makes cosmic ray trigger or other special runs). Each sub-system must define this procedure and make sure that the available functionality of the TTC allows it.

One has to adjust:

- BC (clock phase) at the front-end level
- L1A arrival time
- Bunch Counter Reset (BCR) arrival time to have a coherent BCID.

The fine BC adjustment will be done by looking at the data and for instance looking for a peak position.
The BCR will be adjusted in sending random triggers and histogramming number of hits as a function of BCID. The LHC structure should appear and BCR adjusted so that there is a coincidence between the LHC structure and the constructed histogram.
The L1A delay can then be adjusted in sending a L1A signal at a known BC. L1A delay will be adjusted so that the read-out data contain the proper BCID.

Figure 3 gives a flow chart of the steps in setting up the timing.

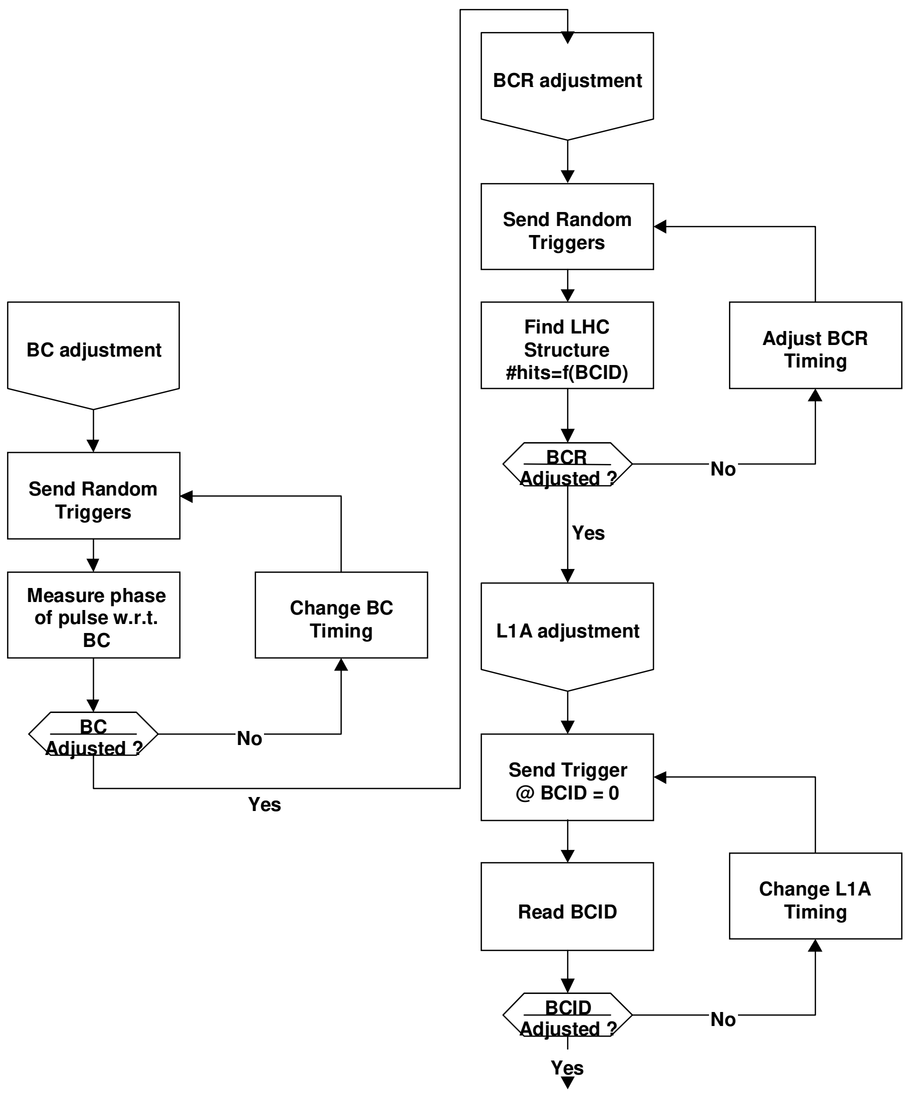

Figure 3. Flow chart of timing adjustment

7. Example of timing set-up

Here the example of a (not yet finalised) proposal for the TRT timing set-up is given for illustration.

There will be 4 TTC partitions for the TRT: one per end-cap side and one per barrel side. There is one timing adjustment at the front-end level of the TRT for 1/32 of an end-cap wheel and 1/32 of a barrel module; these zones contain from 200 to 800 straw-tube channels. One can extract from the read-out data a bit indicating that there has been a hit in a channel. To adjust the timing one looks at the logical OR of these bits for the channels of the zone (or at the number of set bits if the noise level is not low enough). The occupancy of the TRT being high, it is expected to be able to have high statistics in a relatively short time even if the beam luminosity is low.

In addition to the data from each channel, one gets with each event a 4-bit BCID number which is fed at the input of the level-1 pipeline in the Read-out chip (Figure 4).

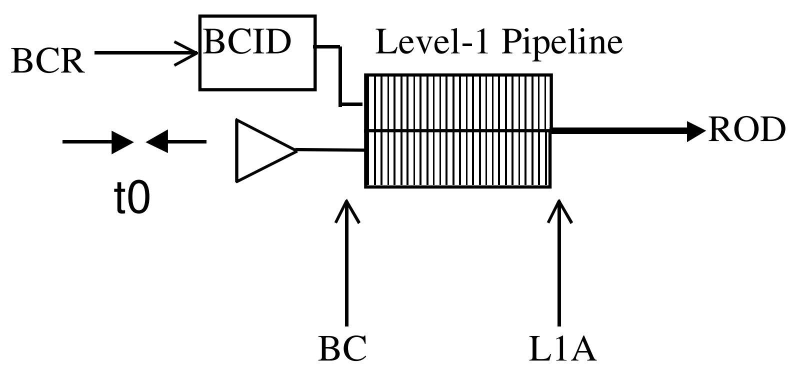

Figure 4. Simplified front-end organisation

Sending random L1A and plotting the number of hits versus BCID, one should see histogram which looks like the LHC structure as shown in figure 2 and taken as reference. This histogram will be shifted in time with respect to the reference as long as the BCID=1 is not properly placed. In addition there will be noise in the empty bunches and there will be data in two additional bunches at the beginning of each gap because of the electrons drift time in the straws (Figure 5). In case of unexpected empty bunches, some additional structure will appear. In applying a threshold to the bin content, another histogram is built with only 0 and 1. One has to shift this histogram so that it coincides with the reference one. To check the coincidence of the two histograms one can build a third one which plots the XOR of their bins (bin3[I] = bin1[I] XOR bin2[I]). The

two histograms can be said “in coincidence” when the number of 1 in the third one is minimum.
The BCR timing is then adjusted to get BCID=1 at the correct place.
Then one runs with a L1A at BC = 1 (or any other value but always the same). The event read-out will give a BCID not equal to 1 as L1A timing has not been adjusted. This timing is then adjusted accordingly.
All these operations can be done with the TTC system, using the facilities of the TTCvi and of the TTCrx.
The very precise BC phase adjustment can only be done in looking at data and reconstructing tracks. Nevertheless, an adjustment at the level of a few nanoseconds (5 – 6 ns) is still necessary because of the zero-suppression scheme used in the ROD; it needs to be worked out but could be done for instance by looking at the trailing edge of the signals in the last bunch of a packet.

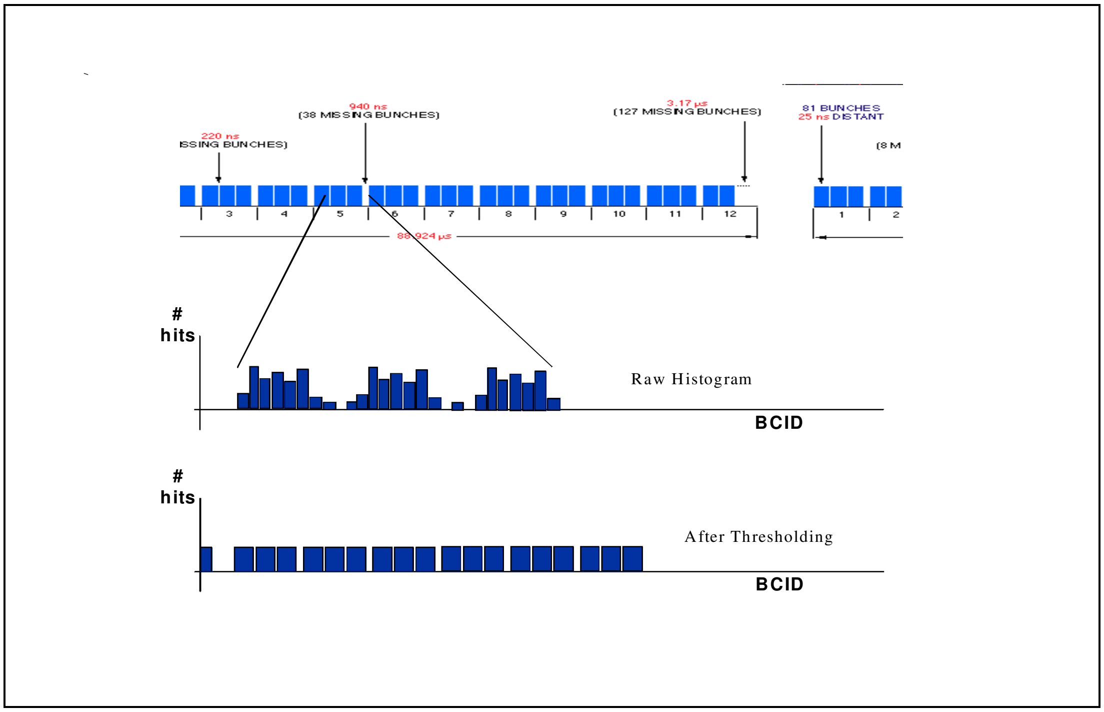

Figure 5. Histograms

Remark

It may be (in order to save silicon area in the front-end chip) that the BCID is formed after the pipeline when the L1A occurs (as shown in figure 6). In this case if one has a bad timing of L1A and BCR, the BCID will be wrong and equal to $BCID_{true} + Error_{L1A} + Error_{BCR}$. The procedure described above is still valid but the correction on L1A and BCR will only be done after the two steps are done as we’ll have a system of 2 equations with 2 unknown parameters.

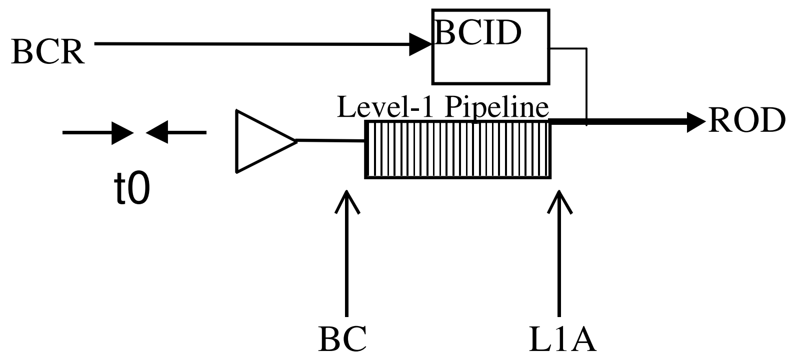

Figure 6. Simplified front-end organisation with BCID formed after the level-1 pipeline