Trigger, Timing & Control Specification

DRAFT 0.3

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Definitions and Acronyms

BC	The 40 MHz clock, linked to the LHC machine, used to synchronise the pipelined processing system.
CTP	Central Trigger Processor — electronic system that accepts inputs from the muon and calorimeter level-1 trigger processors and forms the global (yes/no) level-1 trigger decision for each bunch crossing.
DAQ	Data acquisition.
L1MT	Level-1 muon trigger (system).
LVL1	Level-1 or level-1 trigger.
LVL2	Level-2 or level-2 trigger.
L1A	Level-1 accept signal [1].
ROB	Read-Out Buffer [1].
ROD	Read-Out Driver [1].
ROD_BCID	Number provided by TTC system, used to tag event fragments; corresponds to bunch number in the LHC machine.
ROD_L1ID	Number provided by TTC system, used to tag event fragments; event number defined by counting LVL1 trigger signals.
TTC	Trigger, Timing and Control.
URD	User Requirements Document.
URL	Universal Resource Locator (address used by WWW).
WWW	World-Wide Web.

References

[1] FE interface requirements document, ATLAS-DAQ-NO-049 (see WWW for latest revisions, http://atlasinfo.cern.ch/Atlas/GROUPS/DAQTRIG/FRONTEND/fe.html).
[2] TTC URD, http://atlasinfo.cern.ch/Atlas/GROUPS/DAQTRIG/LEVEL1/LVL1ctpttc.html
[3] RD12 TTC system, http://www.cern.ch/TTC/Intro.html
[4] TTC crate, http://www.cern.ch/TTC/WWWstuff/TxCrateco.GIF
[5] TTCvi Specifications, http://www.cern.ch/TTC/TTCviSpec.pdf
[6] TTCrx Specifications, http://pcvlsi5.cern.ch:80/MicDig/ttc/MANUAL22.PDF

TTC Specification

1. Introduction

The ATLAS read-out electronics elements need the Bunch Crossing (BC) signal to store the front-end signal in the level-1 buffer, and the L1A signal to initiate the read-out. As requested in Ref. [1], each front-end element has to produce an Event Identifier (EVID) and a Bunch Crossing Identifier (BCID) with each event. It is therefore necessary to make available some synchronisation signals in order to maintain coherency between these identifiers across the experiment. These signals are the Bunch Counter Reset (BCR) and the Event Counter Reset (ECR). During test and calibration periods, the read-out electronics elements (Front-end electronics, Read-out Drivers [ROD], possibly Read-out Buffers [ROB]) also need to receive test and calibration signals. All these signals must be made available in thousands of places and their timing must be adjustable.

The Trigger, Timing and Control (TTC) system allows to distribute to the read-out electronics elements (Front-end electronics, Read-out Drivers [ROD], possibly Read-out Buffers [ROB]) the timing signals (LHC clock [BC], synchronisation signals [BCR, ECR]), the trigger signals (ATLAS L1A, test triggers, calibration triggers); it also allows to adjust the timing of all of these signals. It shall fulfil the requirements defined in Ref. [2]. Some sub-detectors require excellent stability and low jitter on the timing signals.

The TTC system is based on an optical fan-out system developed within the framework of RD12 and which allows to distribute signals from one source to about 1000 destinations. This system allows sub-detectors to run either using the central ATLAS timing and trigger signals, or independently, each of them using their specific timing and trigger signals. This leads to a partitionable system. A context diagram with several partitions is shown in figure 1.

The way the TTC system will be used in different sub-detectors depends on the specific requirements of each of them. It will be necessary to have close collaboration between the sub-detectors communities and the TTC team.

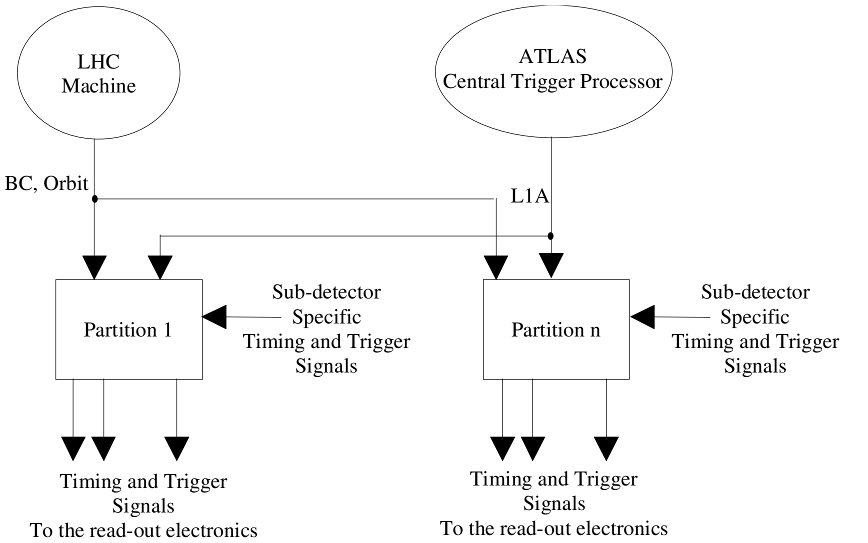

Figure 1. TTC context diagram

Most of the sub-systems will use more than one partition to allow concurrent running of different parts of the detector in different trigger modes during commissioning or calibration periods.

The backbone of the TTC system is based on the optical distribution RD12 TTC system [3]. Some of the ATLAS sub-detectors will use this system up to the on-detector front-end electronics (eg. Liquid Argon Calorimeter); others will stop this system at the level of the RODs at which point they will change the protocol and the functionality (e.g. Inner Tracker). Figure 2 summarises the different configurations.

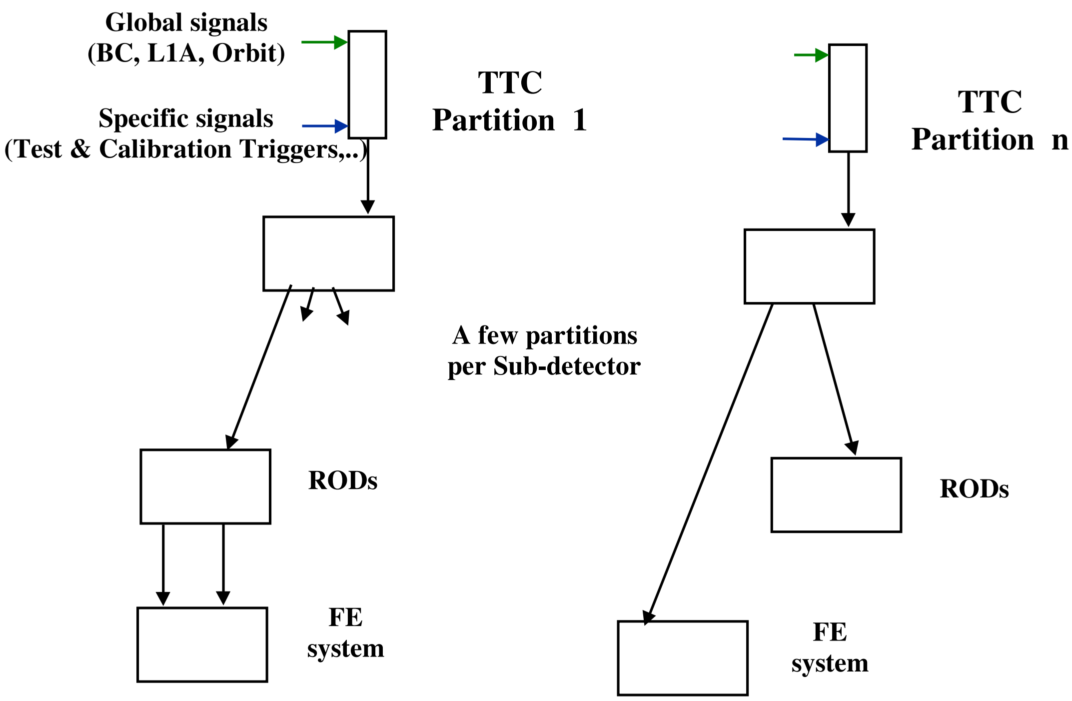

Figure 2. TTC distribution

The RD12 TTC system receives the LHC 40 MHz clock (BC) and the ORBIT signal from the LHC, the L1A signal from the trigger logic, and commands and data from the user. A proper encoding allows to transmit these information on a single optical link which is fan-out to up to 1024 destinations. At the receiving end, an ASIC decodes the incoming signal and makes available the BC clock, the L1A signal, the Event Counter and Bunch Counter Resets signals (ECR and BCR), the Event and Bunch Crossing Identifiers (EVID, BCID) and the user commands and data. Provision is made to adjust the timing of all the signals.

In ATLAS, the TTC system will used in different ways:

- In normal running, it receives its clock from the LHC and the L1A from the Central Trigger Processor (CTP) . The BCR is derived from the LHC ORBIT signal. After each L1A, an 8-bit Trigger-type is forwarded to the destinations as well as (optionally) a 24-bit event ID. It can also transmit user data and commands without introducing dead-time (e.g. test pulses when there is no bunches [LHC gap], front-end parameters [e.g. delay values]) .
- During commissioning and for test and calibration runs, triggers can be injected locally in each TTC system.

This document will go through the specification of the different components of the backbone system and then through the functionality of the system.
References are given to more detailed technical documents.

2. Backbone components

The backbone components are:

- The TTC crate and the fibre network
- The TTC VME Interface (TTCvi)
- The TTC receiver chip (TTCrx)

The TTC crate receives electrical signals from the TTCvi and the LHC machine, and performs the encoding and the electrical-to-optical conversion. An optical tree network with optical passive fan-outs distributes the encoded optical signals to up to 1024 destination nodes. These nodes consist of an optical-to-electrical conversion device followed by a receiver ASIC (TTCrx) which decodes the incoming frame and makes available all the timing, trigger and control signals.
The TTCvi is a VME module which provides the trigger and control signals to the TTC crate in the form of two encoded signals (A Channel and B Channel). This module allows the user to select the trigger source and to generate any command at known times.
A TTC partition consist of a TTCvi, a TTC crate, an optical network and as many receivers as necessary. An example is shown in figure 3.

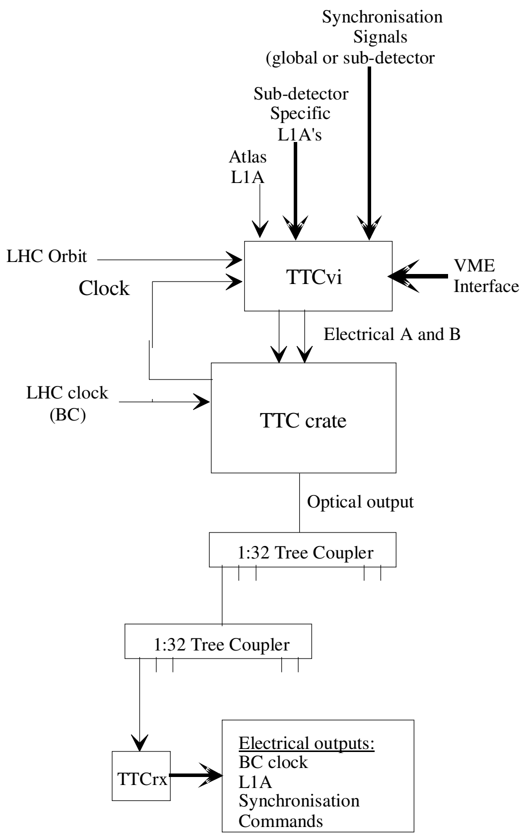

Figure 3. A TTC partition

Detailed specifications of these components are available [4], [5] and [6].

2.1 The TTC crate

The TTC crate receives two electrical signals from the TTCvi and performs the final encoding and the electrical to optical conversion.
The TTC transmitter crate includes a high-power laser transmitter incorporating a 1310 nm laser head module. At this wavelength the chromatic dispersion of normal optical fibre is negligible.

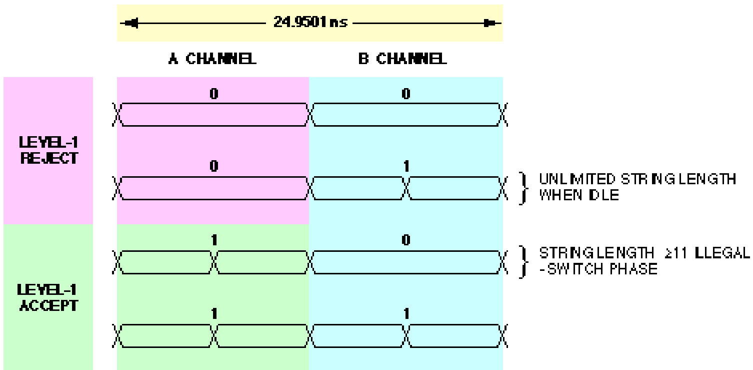

Figure 4. Two channels encoding

The transmitter crates incorporate a 160.32 MBaud biphase mark encoder which time-division multiplexes the 2 input signals (A-channel and B-channel, [figure 4]) using a balanced DC-free code. The primary phase lock loop (PLL) plus encoder jitter when transmitting data is about 7 ps rms. A narrow bandwidth PLL with a low-noise voltage controlled oscillator (VCXO) having low sub-harmonic feedthrough allows an rms output jitter of less than 10 ps to be maintained with an input LHC reference jitter of several hundred ps.
The low-latency A-channel is dedicated to the transmission of level-1 trigger accepts. The B-channel transmits framed and formatted broadcast and individually-addressed commands and data using forward error-correction for high reliability. The format supports up to 16K receivers per distribution zone (partition), each of which may be associated with up to 256 internal and external sub-addresses. Figure 5 gives the encoding format.

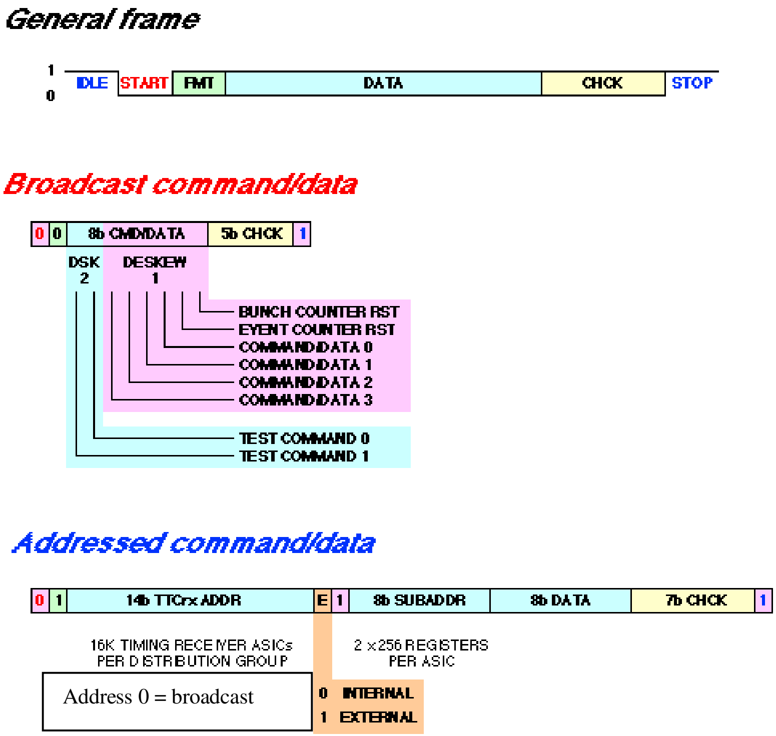

Figure 5. Encoding format

2.2 The TTC VME Interface (TTCvi)

The complete specification is available in [5].
A simplified block diagram of this module is given in figure 6 and a view of the front panel can be seen in figure 7.

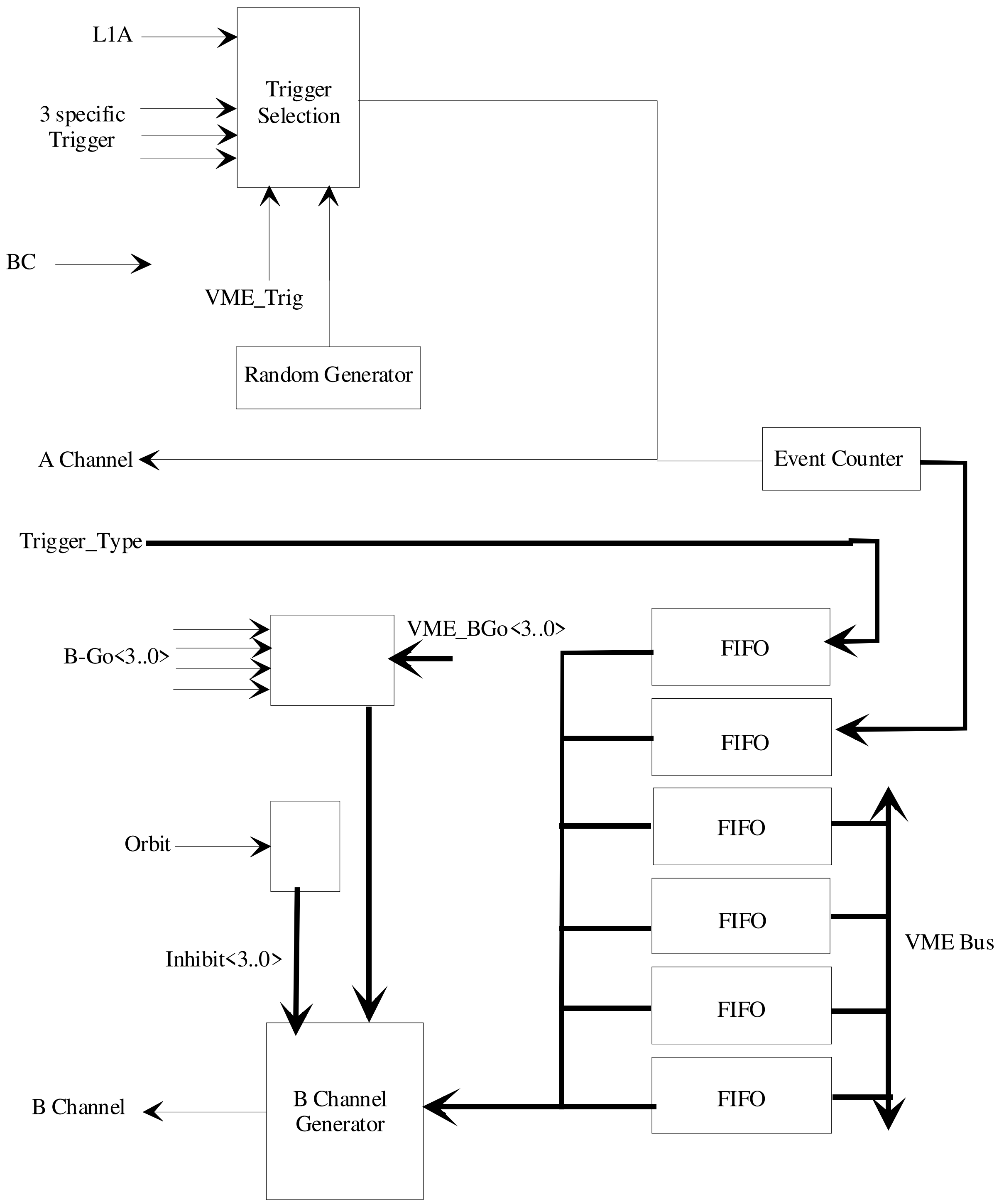

Figure 6. TTCvi Block Diagram

The TTCvi delivers the A Channel and B Channel signals to the TTC transmitter crate. These two signals carry trigger, timing and control information.

The TTC **A Channel** is used only to transmit the Level-1 Accept (L1A) signal.

The TTC **B Channel** is used to transmit framed and formatted commands and data. These can be either:

- Short-format synchronous or asynchronous broadcast command/data cycles. If synchronous, the timing of these cycles relative to the LHC orbit is controlled precisely. Such cycles are used for the broadcasting of the bunch counter reset signals which control the phases of the TTCrx bunch counters, and for the transmission of other fast synchronous broadcast controls and test commands which can be decoded at the receiving end (after TTCrx) and used to produce test pulses, calibration pulses, etc...
- Long-format asynchronous individually-addressed or broadcast command/data cycles. The timing of these cycles with respect to the LHC orbit is indeterminate and they are not individually deskewed in TTCrx ASICs. They are used for the transmission of parameters and non-time-critical commands. For instance, this is used to transmit the trigger type and the event number for each L1A.

The TTCvi is the master of a TTC partition. It is fully controlled through a VME interface by the partition user. It is at this level that the user decides to include this partition in the global ATLAS read-out system or to run it in independent test or calibration runs. In this last case it uses its own timing and trigger signals.

2.2.1 Clock inputs

The TTCvi module is normally driven by a 40.08 MHz clock signal which it receives from the LHC machine.

For test purposes one can select the clock used by the TTCvi from two sources:

- 1 front panel input which is the normal clock from the LHC machine.
- An internal 40.08 MHz oscillator (not phase-locked to the TTC system).

2.2.2 Trigger inputs

Although in normal running the trigger input to the module is the L1A signal provided by the Central Trigger Processor, the TTCvi allows other trigger sources to be selected for test or calibration purposes without modifying the cabling. These sources are synchronised with the 40.08 MHz clock in the TTCvi.

The latency introduced by the module on the L1A coming from the CTP is minimised and is about 3 ns.

Four front panel external inputs (including the one for the standard L1A input) are provided, with programmable selection of the one in use. In addition, it is possible to generate a trigger by a VME access to a key address and an internal random trigger generator is provided for test purposes. The internal generator provides a L1A signal; the number of L1A per unit of time follows a Poisson distribution with a mean rate programmable from about 1 Hz to 160 kHz.
The selected trigger is made available as a front panel output for monitoring purposes.
An internal 24-bit event counter (which can be read and written through VME) counts the number of triggers sent.

2.2.3 Orbit input

The orbit signal is a square wave of period 88.924 μs which is received from the LHC machine and distributed to the TTCvi and other components for the generation of signals which are synchronised to the LHC orbit. Adjustment of the phase of the Orbit signal permits a global control of the timing of the entire TTC system relative to the LHC bunch structure.
To allow tests to be performed when the LHC orbit signal is not available, the TTCvi incorporates an internal pseudo orbit signal source obtained by dividing the 40.08 MHz clock by 3564.

2.2.4 Inhibit<3..0> signals

In order to be able to send B Channel signals at known times within the LHC cycle, four independently-programmable timing signals called Inhibit<3..0> are generated within the TTCvi module. Each Inhibit signal starts a programmable (12-bit) number of clock cycles after the start of the orbit signal and has a duration of a programmable (8-bit) number of clock cycles. Transmission of the associated synchronous command commences at the end of the Inhibit signal duration.

Each Inhibit signal is assigned a different priority level, such that Inhibit<0> has higher priority than Inhibit<1>, etc. When an Inhibit signal becomes active, the transmission of any command associated with a lower priority Inhibit is allowed to complete, but further such commands are held off until the higher priority one has been sent. Since the Inhibit signals are always programmed to have a duration exceeding that required for the transmission of even a long-format cycle (about 1.05 μs), the higher priority signal is always transmitted at a determinate time relative to the LHC orbit.

The highest priority Inhibit <0> is used to initiate the transmission, during the LHC extractor gap, of a broadcast command containing the bunch counter reset. This signal, after deskewing in the individual receiver ASICs, is used to control the phase of the TTCrx bunch counters. The three other Inhibit signals are available for the generation of other synchronous commands including those required for triggering test pulse generators. All four Inhibit signals are made available as front panel outputs for monitoring purposes.

Through appropriate preprogramming, one can ensure that synchronous commands at all priority levels are always sent at well defined times.

2.2.5 Generation of B Channel cycles

The TTCvi permits synchronous and asynchronous short- and long-format B Channel command/data cycles to be generated in a number of different ways:

• Short- and long-format asynchronous cycles.

Asynchronous cycles may be initiated by writing the required data (a single byte for short-format or two 16-bit words for long-format) to specified TTCvi VME addresses. Normally short-format cycles are used for broadcast commands or data while long-format cycles are used for individually-addressed commands or data. However, a broadcast of 16 bits of data can be made with long-format cycles if TTCrx address 0 is chosen. The timing of these cycles is not synchronised with the LHC orbit.

• Pre-loaded synchronous or asynchronous cycles.

Four VME-addressable FIFOs are provided which may be pre-loaded with commands and data to be transmitted by B Channel cycles. For each of the four channels, the actual transmission of the pre-loaded information is initiated by a signal called B-Go<3..0>. Sequences of B Channel cycles can be generated by loading the FIFOs with several parameters.
If synchronous mode is selected, the B-channel cycle is generated at the end of the Inhibit<i> signal. The cycle can be programmed to be either single or repetitive. In single mode, only one cycle is generated if a B-Go<i> has occurred before Inhibit<i>. In repetitive mode, the cycle is generated at the end of each Inhibit<i> signal (i.e., once per LHC orbit). The bunch counter reset command, for example, is sent in repetitive mode.
If asynchronous mode is selected, the B Channel cycle is generated when the B-Go<i> signal occurs. There will be one cycle and one cycle only for each occurrence of the signal.
In addition, a special mode has been implemented to allow the download of large amount of data (e.g. at the beginning of a run if the TTC system is used to download parameters). In this mode, the B Channel cycle is initiated as soon as the selected FIFO contains data.

• Event number and trigger type cycle.

After each L1A is transmitted, the contents of the 24-bit event counter in the TTCvi can optionally be broadcast together with an 8-bit trigger type parameter which is received from the Central Trigger Processor via a front panel connection. This broadcast, is made asynchronously and takes about 4.4 µs if the B Channel is free. Internally, the event number and the trigger type are stored in FIFOs to avoid any losses due to the random time of arrival of L1A.

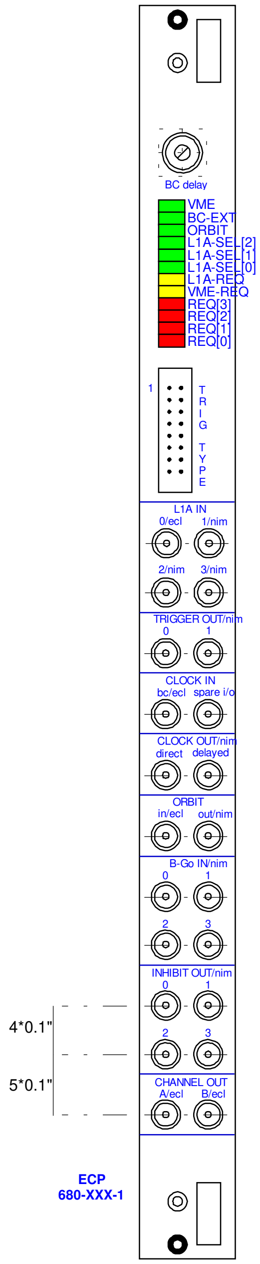

Figure 6 TTCvi front panel

2.3 TTC receiver chip (TTCrx)

The TTCrx (figure 7) is a custom IC that receives control and synchronisation information from the central TTC system and makes it available to the read-out electronics. The TTCrx can be programmed to compensate for particle times of flight and for propagation delays associated with the detectors and their electronics. The IC delivers the LHC timing reference signal, the first level trigger decision and its associated bunch and event numbers. In addition, it provides for receiption of synchronised broadcast commands and individually-addressed controls and parameters.

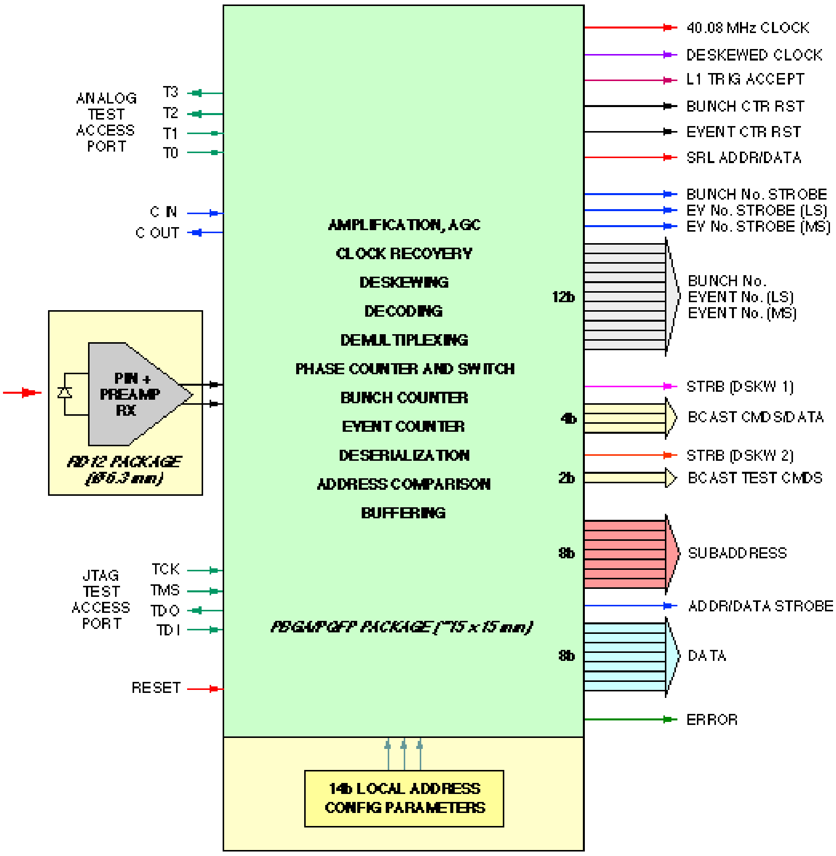

Figure 7 TTCrx diagram

One of the main functions of the TTCrx is to recover and distribute the 40.08 MHz LHC reference clock with minimal jitter (70 ps rms). The timing receiver makes also available to the detector electronics the first-level trigger-accept decisions (L1A signal) and their associated bunch crossing and event identification numbers. The latency introduced on the L1A signal (input frame to output signal) is 3 clock cycles (75 ns).

Each TTCrx IC is identified in the distribution network by a unique 14-bit channel Identification (ID) number. This number is read from a serial PROM at power up or after a reload ID broadcast command is received. The ASIC control logic identifies the A and B channels, deserializes the data in the B channel and continuously monitors it to look for the presence of its ID channel number.

The TTCrx IC has already been mapped into a standard 1mm CMOS digital process. The ASIC footprint is 4.5 mm x 4.5mm and has been packaged in a 100 pin BGA package. A new version is being developed in a radiation hard technology.

The ASIC receives the TTC system data in the form of an electrical signal from the optical to electrical converter. The LHC system clock is recovered with minimum jitter, and the trigger (A) and data (B) channels are separated. The recovered clock is then fed to a “Programmable Fine Deskew” unit where two different clock phases, synchronous with the LHC system clock, are generated. The phases of the two clocks can be controlled independently in steps of 104 ps between 0 and 25 ns.

With each L1A, the TTCrx delivers a 12-bit BC identifier (BCID) and a 24-bit Level-1 identifier (L1ID) on a 12-bit bus. Hence, three clock cycles are necessary.

The Bunch Counter Reset (BCR) and Event Counter Reset (ECR) are decoded in the chip and made available.

The other broadcast commands bits are made available as an 8-bit word for external decoding.

The phase of each signal can be adjusted. In addition, L1A, BCR, ECR and the command word can individually be delayed by up to 16 clock cycles in order to have these signals available at the right bunch crossing.

The delays can be programmed via commands on the B channel or through a local I2C interface for the new version (I2C will be implemented instead of JTAG and used for programming the internal registers).

Provision is for error detection on the incoming frame is done and internal error registers are incremented each time an error is detected.

All internal registers can be dumped on the external data bus for reading. This is done via commands on the B channel or through a local I2C interface.

3. Expected latency on L1A

Table 1 and figure 9 show the different elements which contribute to the latency on L1A signal. The delay introduced by the cables between the CTP and the TTCvi's are computed assuming that all TTC crates are close to the CTP. This model is very likely to be false as one can expect the sub-detector teams wish to have their TTC crates and interfaces close to their read-out electronics and additional electronics they could need for test and calibration.

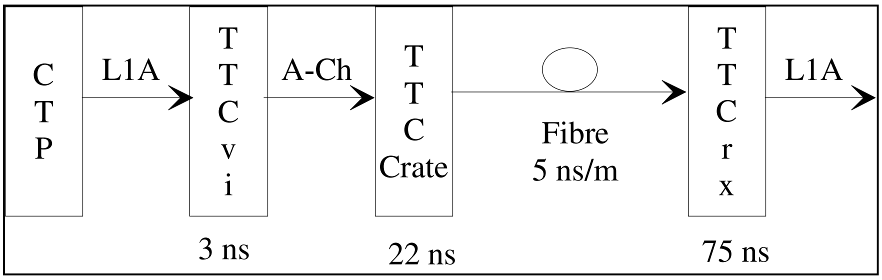

Figure 9. Latency components

Element	Delay	Remark
CTP-TTCvi	50 ns	Cable and fan-out
TTCvi	3 ns	3 ECL stages
TTCvi to TTC crate	3 ns	Cable
TTC crate	22 ns	Modulator etc…
Fibre	400 ns	80 m
TTCrx	75 ns	Receiver
Total delay excluding cables and fibres	**100ns**	TTCvi + TTC crate + TTCrx
Total Latency	***553 ns***	*About 21 BC*

Table 1. Latency elements