

TTCrx Reference Manual

***A Timing, Trigger and Control Distribution
Receiver ASIC for LHC Detectors***

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Summary of changes

Version 2.2

- ⇒ New TTCrx test board (see: Test Board).
- ⇒ Deskew mapping table (see: Unfolding Table).
- ⇒ TTCrx new package – Ball Grid Array (see: TTCRX package).
- ⇒ Test results (see: Measurements).

Version 2.0

- ⇒ TTCrx L1A latency reduced to 100 ns (see: Trigger latency).
- ⇒ New configuration bits introduced in the “Configuration Register” and register bits re-assigned (see: Configuration register).
- ⇒ The ERDUMP and the L1A sequence have been changed to maintain consistency between the different operation modes (see: ERDUMP and L1A sequence).
- ⇒ Test signals A_test0, A_test1, A_test2 and A_test3 have been removed and signals TestIn and TestOut introduced (see: TTCrx signals).
- ⇒ JTAG boundary scan functionality and pins JTAGTCK, JTAGTDI, JTAGTDO, JTAGTMS and JTAGTRST_b added (see: TTCrx signals and Boundary Scan Register).
- ⇒ A new signal (ClockL1Accept) that combines the clock and trigger information has been introduced (see: TTCrx signals).
- ⇒ New Test Signal VcoOn added – for test purposes only, not available as a package pin (see: TTCrx signals).

Chapter 1

Introduction

The TTCrx is a custom IC that was designed by the CERN ECP Microelectronics group. It acts as an Interface between the Timing Trigger and Control Distribution (TTC) system for LHC detectors and its receiving end users. The ASIC receives control and synchronisation information from the central TTC system and makes it available to the front-end electronics controllers in the detectors. The TTCrx can be programmed to compensate for particle times of flight and for propagation delays associated with the detectors and their electronics. The IC delivers the LHC timing reference signal, the first level trigger decisions and its associated bunch and event numbers. Besides, it provides for transmission of synchronised broadcast commands and individually-addressed controls and parameters.

This document is intended to provide a functional and physical description of the TTCrx IC from the user perspective.

TTC SYSTEM OVERVIEW

The Timing Trigger and Control (TTC) system for LHC detectors has been specified and complete descriptions of the system and its functionality can be found in references [1] and [2]. However, a brief overview of the TTC system features that are most relevant for the understanding and utilisation of the TTCrx IC is made here.

In each LHC experiment the TTC system controls the detector synchronisation and delivers to the front-end electronics controllers the fast signals and messages that

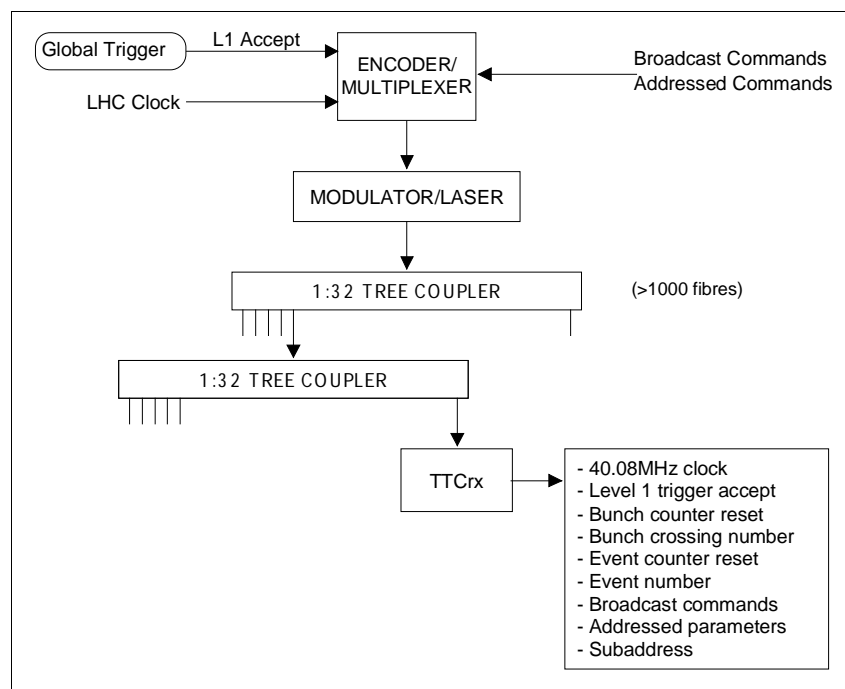


Figure 1 TTC optical distribution network

are necessary to run the experiments. Figure 1 illustrates the basic architecture of the TTC system: at the top of the TTC tree structure, two communication channels are Time Division Multiplexed (TDM), BiPhase Mark (BPM) encoded and transmitted over a passive optical fibre distribution network using a single laser source. One of the TDM channels (channel A) is exclusively dedicated to broadcast the first-level trigger-accept (L1A) decisions, delivering a one-bit decision for every bunch crossing. The other, (channel B) is used to broadcast data to all or specific system destinations. The TTC system is also used to distribute the LHC 40.08 MHz bunch-crossing reference clock signal. This signal is not explicitly transmitted over the network and has to be recovered from the incoming data at each TTC system destination.

Data in channel B can be of two types [1], [2]: broadcast commands or individually-addressed data/commands. Broadcast commands are used to distribute messages to all TTC destinations in the system. When detected, these commands are executed by all the TTC receivers. The individually-addressed data/commands are implemented in the system to transmit user-defined data and commands over the network. These commands have two distinct modes of operation. In the first mode, they are aimed at the TTC receivers themselves and their user-defined content is used to control the receiver's operation. In the second mode, the data are intended for the external electronics. In this case, both the data and sub-address contents of the received commands are made externally available by the addressed TTC receiver.

Both the broadcast and the individually-addressed commands are transmitted over the TTC network using a frame format that has been specified in reference [1] and which is schematically represented in Figure 2. The frame structure contains several fields to control the transmission and includes a field in which several redundant bits are inserted for error detection and correction. The coding scheme used is a standard Hamming code with the capability of double error detection and single bit error correction. The error correction coding covers the 8-bit data word in the case of a broadcast command/data frame and the 32-bit data in the case of an individually-addressed command/data frame¹. The address space selection bit (E) instructs the addressed TTC receiver either to execute an internal operation or to make the received individually-addressed command/data externally available. Using this scheme it is possible to address up to 256 internal and external subaddresses associated with up to 16K timing receivers in each timing distribution group.

¹Start, frame type and stop bits are not included in the error correction scheme.

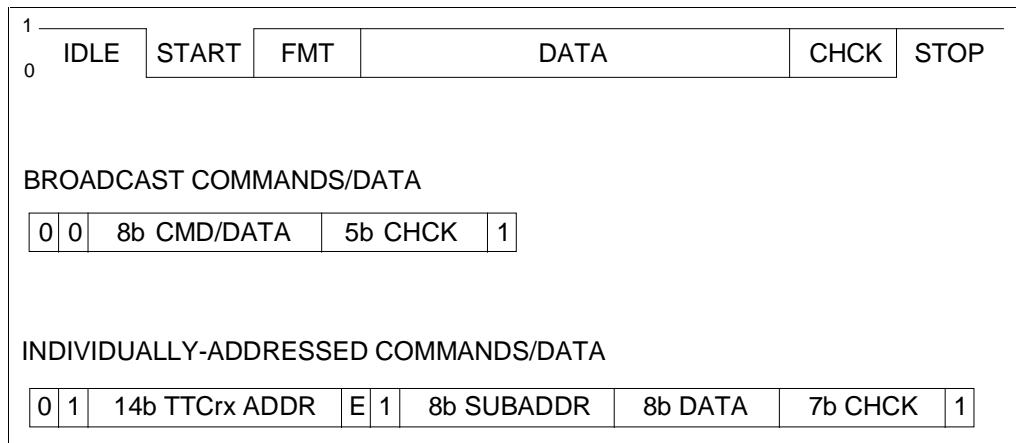


Figure 2 Data transmission frame format

Each frame is identified by a header bit (FMT) which indicates its type. Start (logical “0”) and stop (logical “1”) bits are always included at the beginning and end of the frame transmission to facilitate correct synchronisation.

As mentioned before, channels A and B are time division multiplexed and biphas mark encoded before transmission over the network. With this type of encoding there is a fundamental phase ambiguity between the recovered clock and the two transmitted channels. This ambiguity is resolved automatically in the receivers by monitoring constraints imposed on the channel A data structure. Figure 3 shows the TTC signal encoding for the two TDM channels.

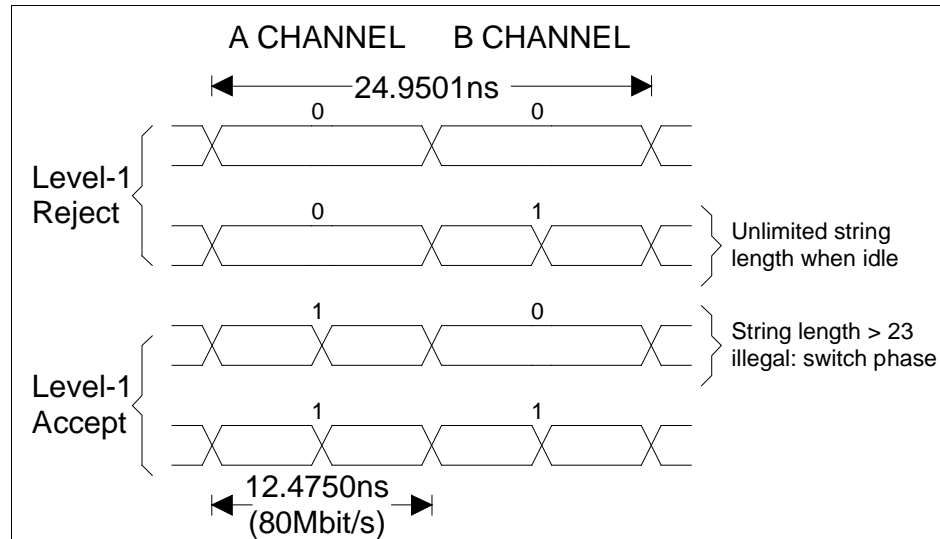


Figure 3 TDM biphas mark encoding

TTCrx OVERVIEW

A timing receiver is associated with each of the outputs of the TTC optical distribution network. Each receiver is composed of a commercial integrated photodetector-preamplifier and of the special purpose custom IC (TTCrx) described in this manual [3]. The TTCrx ASIC receives, decodes, executes and distributes the commands and data broadcast over the TTC distribution network. It recognises

individually-addressed commands for purposes of internal and external control and supports the transmission of synchronised broadcast commands. One of the main functions of the TTCrx is to recover and distribute the 40.08 MHz LHC reference clock with minimum jitter. The timing receiver makes also available to the detector electronics the first-level trigger-accept decisions and their associated bunch crossing and event identification numbers. Each TTCrx IC is identified in the distribution network by a unique 14-bit channel Identification (ID) number. This number is read from a serial PROM at power up or after a reload ID broadcast command is received. The ASIC control logic identifies the A and B channels, deserializes the data in the B channel and continuously monitors it to look for the presence of its ID channel number.

The TTCrx IC has been mapped into a standard 1 μ m CMOS digital process from ES2 with all the analogue and time-critical functions implemented in full custom. Standard cells were used to implement the digital and the non time-critical functions. The ASIC footprint is 4.5 \times 4.5mm and has been packaged in a 100 pin BGA package.

TTCrx architecture

Figure 4 shows the architecture chosen to implement the TTCrx functionality. As shown in this figure, the ASIC receives the TTC system data in the form of an electrical signal from the optical preamplifier. Due to the optical power levels detected by the preamplifier, this signal needs to be amplified to CMOS levels before it can be used for clock recovery, data decoding and demultiplexing. The unit marked as “Linear Receiver” in Figure 4 implements that function. Signal level detection and automatic gain control are also taken care of inside this block. After the signal is restored to CMOS levels, it is fed to the “Clock Extraction” and the “Data Decoder/Demultiplexer” units where the LHC system clock is recovered with minimum jitter, and the trigger (A) and data (B) channels are separated. The recovered clock is then fed to the “Programmable Fine Deskew” unit where two different clock phases, synchronous with the LHC system clock, are generated. The phases of the two clocks can be controlled independently via commands on the B channel. The “Programmable Fine Deskew” unit allows the two clock phases to be changed in steps of 104 ps between 0 and 25 ns.

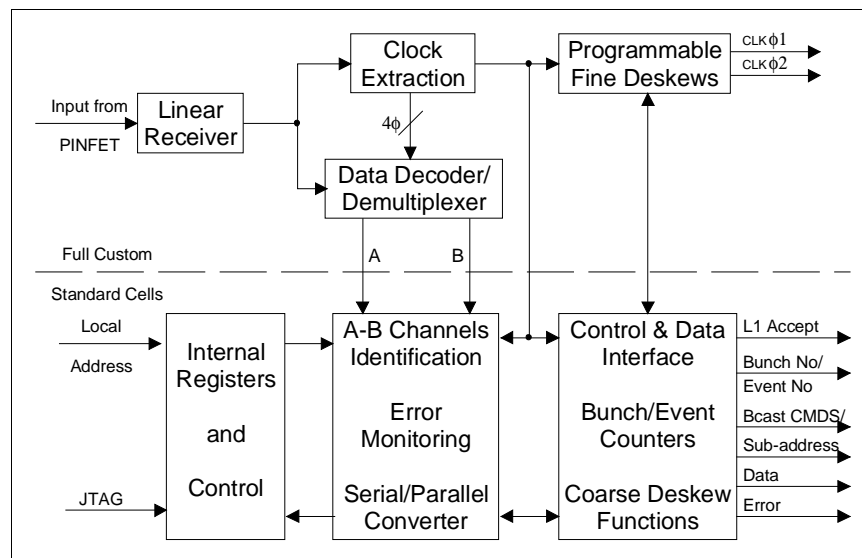


Figure 4 Timing receiver block diagram

The TTCrx control logic consists of three major blocks. The first block contains the internal configuration and status registers and implements the logic necessary to

read a 14 bit number from an external serial configuration PROM that supplies the TTCrx ASIC with its unique system address.

The second block identifies the trigger and data channels and constantly monitors the data in channel B for transmission errors. It deserializes the received data and decides if this is addressed to the IC itself or to some external addressable or common space. Finally, the third functional block implements two independently programmed coarse deskewing functions for the first-level trigger signal and the broadcast commands. The related control registers can be programmed by individually-addressed data transmitted over the B channel. Both first-level trigger and broadcast commands can be deskewed over a range of 16 bunch-crossing intervals.

TTCrx internal registers

The TTCrx contains several internal registers used for control and monitoring of its operation. These registers are:

- Configuration register;
- Control register;
- Coarse Delay register;
- Fine Delay registers;
- Bunch Counter;
- Event Counter register;
- Single Bit Error;
- Double Bit/Frame Error counter.

The **Configuration** register contains the configuration bits read during initialisation from the external serial PROM. It is used to store the 14-bit chip ID and to set up some of the different ASIC operation and test modes.

The **Control** register is used to minimise the IC power consumption by allowing the disabling of some of the chip functionality in applications that do not require it. For instance, the Event and Bunch counters and the Address and Data buses can be disabled if not required by the external electronics.

The **Coarse Delay** register holds the deskewing parameters for the First Level Trigger Accept (L1A) and the Bunch Counter Reset signals. The contents of this register in conjunction with that of the Fine Delay register affects the total amount of deskewing. Since the same deskewing is applied to the L1A signal and the broadcast commands, deskewing of the latter ones will also have to be performed at the source of the TTC system to compensate for the time necessary to transmit and decode these commands.

The **Fine Delay** registers hold the deskewing parameters that control the programmable delay generator discussed previously. When combined with the coarse deskewing functions, a compensation range of 16 bunch-crossing intervals is obtained. This allows a substantial margin beyond the possible maximum variations due to differences in time-of-flight and optical fibre path lengths in the detectors.

The **Bunch** and the **Event Counters** are free running counters that are incremented by the recovered clock and the L1A signals, respectively. These counters can be reset by specially defined broadcast commands. The Bunch Counter register content, which is a 12-bit number, is normally available to the outside logic. However, during the two clock cycles following a trigger accept, the 24-bit Event Number register content can optionally be made available to the outside electronics on the same 12 output lines.

Finally, the **Single Bit Error** and the **Double Bit/Frame Error counters** are used to keep track of the number of errors occurring during data reception. Since the receiver Hamming decoder is capable of fully recovering from single bit errors, the data are accepted after correction and the Single Bit Error register incremented. When a double bit error is recognised by the receiver logic or a frame error is detected, the data are ignored and the contents of the Double Bit/Frame Error register incremented. The contents of the internal error counters are dumped on the external data bus when an error dump broadcast command is issued by the central TTC system.

Chapter 2

TTC System Frame Formats

This chapter discusses the frame formats used for transmission of broadcast commands and individually-addressed commands/data in the TTC system. This topic has been introduced in section “TTC system overview” of chapter 1.

FRAME FORMATS

Two basic frame formats are used to transmit broadcast commands and individually-addressed commands/data to the TTC receivers. The frames are sent with several redundant bits for single bit error correction and double bit error detection. The coding scheme used is a standard Hamming code with one additional even parity bit to detect double bit errors [4]. A start and a stop bit are included in each frame for correct frame synchronisation. The two adopted frame formats are defined as follows:

Broadcast frame

The broadcast frame is used to distribute messages to all TTC receivers in the system (broadcast commands). This type of frame is identified by a “0” in its header bit (FMT). All TTCrxs, after having performed appropriate checking on the received packet, execute the operation requested in the data part of the frame. For broadcast frames, error correction and detection are made on the 8 data bits.

START	FMT	CMD/DATA <7:0>	CHCK <4:0>	STOP
0	0	ddddddd	eeee	1

Individually-addressed commands/data frame

Individually-addressed commands/data frames are identified by a “1” in the header bit (FMT). This frame is used to address a single TTCrx in the system². Data sent to a particular TTCrx are output to the data bus and the Data Qualifier <3:0> bus is set to “0” to validate the data bus content. The error correction coding covers the entire 32 data bits in the frame. Start, header and stop bits are not included in the error correction scheme.

START	FMT	TTCrx ADDR <13:0>	E	1	SUBADDR <7:0>	DATA <7:0>	CHCK <6:0>	STOP
0	1	tttttttttt	i	1	sssssss	ddddddd	eeeeeee	1

²See “TTCrx Addressing” for exception on the TTCrx ADDR “0”.

Chapter 3

Receiver Addressing

This chapter discusses the different receiver addressing modes implemented in the TTC distribution system and recognised by the TTCrx ASIC.

TTCrx ADDRESSING

Each TTCrx IC is identified in the distribution network by a unique 14-bit channel Identification (ID) number. This number is read from a serial PROM³ at power up or after a reload ID broadcast command is received. Each TTCrx in the distribution system deserializes the data in channel B and continuously monitors it to look for the presence of its ID channel number.

Individual addressing

The individually addressable space for each TTCrx is split into two: internal and external. The internal address space is used to write in the TTCrx internal registers while the external space allows commands and data to be transmitted to the detectors electronics. When an individually-addressed commands/data frame⁴ is received with the bit E equal to “0” the internal address space is assumed. A “1” received in the E bit indicates external addressing and the external subaddress and data buses are set according to the data contents of the received command.

The TTCrx **internal addressing space** is allocated as follows:

SUBADDR <1:0>	Location
00000000	Fine Delay Register 1 <7:0>
00000001	Fine Delay Register 2 <7:0>
00000010	Coarse Delay Register <7:0>
00000011	Control Register <7:0>

Global addressing

Simultaneous addressing of all the receivers in a TTC distribution group is made using broadcast commands. Every TTCrx in a distribution group should execute the received command. In addition to the broadcast addressing provided by the broadcast frame⁵, another method of sending data to all TTCrxs is provided by reserving the lowest TTCrx address (i.e. ADDR<13:0> = “0”) to mean a broadcast message with 8 bit of data to all chips. The external/internal bit (E) and the subaddress range still remain active for this message type.

³Serial PROM type XC1736D from Xilinx [5].

⁴See “Frame formats” for individually-addressed command/data frame specification.

⁵See “Frame formats” for broadcast frame specification.

Chapter 4

Receiver Internal Registers

In this chapter, the TTCrx internal registers are described in detail. A brief summary of the TTCrx registers and their functionality can be found in section “TTCrx overview” of chapter 1.

TTCrx REGISTERS

The TTCrx contains several internal registers for control and monitoring of its operation. These registers are listed below:

- Configuration register;
- Control register;
- Coarse Delay register;
- Fine Delay registers;
- Bunch Counter register;
- Event Counter register;
- Single Bit Error counter;
- Double Bit/Frame Error counter.

Configuration register

This 69-bit register contains the string of configuration bits read at initialisation time from the external serial PROM. It is used to store the 14-bit chip ID and to set up some of the different ASIC operation and test modes. The register is not directly readable but it can be dumped on the external data bus after reception of a CRDUMP broadcast command. If this instruction is executed, the register is dumped onto the data bus in a sequence of bytes, starting from the lowest one (bits 7 to 0). The **configuration register** bit allocation is as follows:

PROM bit(s) ⁶	Function/internal signals	Recommended parameters
68–64	aux_mux_select<4:0>	“00001”
63	enable_reinitialise	User defined
62	dll_input_mux	“0”
61	dll_reset_mux	“0”
60–56	dll_isel_b<4:0>	“11110”
55–52	lock_period<3:0>	“1111”
51–48	check_period<3:0>	“1111”
47–46	vco_isel<1:0>	“01”

⁶ Bit aux_mux_select<4> is the first bit to be read from the serial PROM and bit ID<0> the last.

45–41	pfd_isel_b<4:0>	“11101”
40–36	pd_isel_b<4:0>	“11101”
35–31	dll_isel_b<4:0>	“11101”
30–28	aux_mux<2:0>	“000”
27	decode_mux	“0”
26	pll_mux	“0”
25	ref_gen_mux ⁷	“0”
24	ref_gen_on	“1”
23	fpd_on	“1”
22	enable_clk_trig	User defined
21	gain_select	“0”
20–16	amp_isel_b<4:0>	“10000”
15	Enable Clock40Des2	User defined
14	Enable Hamming decoding	“1”
13–0	TTCrx ID<13:0>	User defined

With the exception of the user defined parameters, the configuration register recommended parameters should never be modified by the user.

Control register

The control register is used to minimise the IC power consumption by allowing the disabling of some of the chip functionality in applications that do not require it. Several bits are available in the **control register** and they are allocated as follows:

	Function	Reset state
0	Enable Bunch Counter operation	1 (enabled)
1	Enable Event Counter operation	1 (enabled)
2	Reserved	
3	Enable Single Bit Error Init.	0 (disabled)
4	Enable Double Bit Error Init.	0 (disabled)
5	Enable Parallel A/D bus ⁸	0 (disabled)
6	Enable Serial A/D bus	0 (disabled)
7	Enable non-deskewed 40 MHz output	1 (enabled)

Bits 3 and 4 are used to control the re-initialisation process. If receiver re-initialisation is enabled in the configuration register then, bits 3 and 4 control the re-initialisation conditions.

Coarse delay register

The Coarse Delay register holds the deskewing parameters for the First Level Trigger Accept (L1A) and the Bunch Counter Reset signals. The content of this

⁷ This bit must be set to “1” if bypassing⁷ of the post-amplifier is required. In this case, the TDM biphasic mark signal should be provided to the TestIn input. This input requires CMOS levels for correct operation.

⁸ Setting this bit forces to “0” the following output pins: Dout<7:0>, DQ<3:0>, SubAddr<7:0> and DoutStr. All the other outputs function normally.

register in conjunction with that of the Fine Delay register affects the total amount of deskewing applied to these signals. Since the same deskewing is applied to the L1A signal and the broadcast commands, deskewing of the latter ones will have also to be performed at the source of the TTC system to compensate for the time necessary to transmit and decode these commands.

The 8 bit **coarse delay register** holds two sets of four bits, each determining the coarse deskewing of two groups of registers. The coarse delay register bits <3:0> and <7:4> control the amount of deskewing applied to the external strobe signals BrcstStr1 and BrcstStr2 respectively.

Bits	Deskewing function
<3:0>	Bunch counter reset (deskew 1)
<7:4>	User broadcast command (deskew 2)

Fine delay registers

Two 40.08 MHz clock outputs are provided by the TTCrx. These outputs are controlled by two separate registers. The fine delay registers are loaded by sending data to them using an individually-addressed commands/data frame addressed to locations “0” and “1” in a given TTCrx. These are 8 bit registers allowing the clock phase to be changed in steps of 104 ps between 0 and 25 ns.

Notice that the mapping of the eight bits in a linear delay requires a mapping table which will be provided as a software subroutine (see “Unfolding Table”).

Bunch counter

The bunch counter is a free running counter incremented by the received clock signal. This counter is 12 bit long and is reset uniquely by the BCRST broadcast command and by the chip initialisation procedure.

Event counter

The event counter is a free running counter incremented by the L1Accept signal. This counter is 24 bit long and is reset uniquely by the ECRST broadcast command and by the chip initialisation procedure.

Single bit error counter

This 16-bit counter keeps track of the number of single bit errors recognised by the receiver’s Hamming decoder. Since these errors are fully recovered, received commands and data are accepted by the TTCrx after correction in the receiver block itself.

Double bit error and frame error counter

This 16 bit counter keeps track of the number of double bit errors recognised by the receiver logic and of the number of frame errors (stop bit not equal to one). After such an error, received data are not used and no action is taken. The TTCrx tries to resynchronise to the next start bit. In the process of resynchronisation, errors can again occur.⁹

⁹ Note that both the single error counter and double bit and frame error counter are disabled once their content reaches 65535. A re-initialisation sequence is necessary to reactivate and reset these counters.

Chapter 5

Broadcast Messages

This chapter describes the system and user defined broadcast commands/data.

BROADCAST COMMANDS/DATA

The TTCrx can accept up to 256 different broadcast messages, encoded in the 8-bit broadcast packet. Broadcast messages are deskewed by a delay equal to the coarse delay programmed in the Coarse Delay register bits <3:0>. Since this delay also affects the L1Accept signal, deskewing of the broadcast commands will also have to be performed at the source of the TTCrx system to compensate for the time necessary to transmit these commands.

The most common broadcast commands are enumerated below:

Command	Format #	Function
NOP	uu ssss 00	Do nothing ¹⁰
BCRST	uu ssss 01	Bunch counter reset
ECRST	uu ssss 10	Event counter reset
EBCRST	uu ssss 11	Reset event and bunch counters
ERDUMP	uu 0001 bb	Dump internal error counter to Data Bus
CRDUMP	uu 0010 bb	Read PROM to Data Bus ¹¹
RESERVED	uu 0011 bb	
INIT	uu 0100 bb	Reload TTCrx ID and re-initialise
USER	uu xxxx bb	User defined broadcasts ¹²

The “uu” bits in the table indicate user defined broadcast messages (test commands). The four “ssss” bits are used for system wide broadcast messages (run commands). Some of these messages are already defined in the table (ERDUMP, CRDUMP, and INIT). The detailed operation of each of the above instruction is explained below. System wide and user broadcast commands are output in the Brcst<7:5> bus and are validated by the strobe signals BrcstStr1 and BrcstStr2. Both signals are activated once a broadcast command is received. However, these signals can be independently programmed to occur at different instants.

BCRST

Bunch counter reset: a bunch counter reset is performed.

¹⁰ Used for testing purposes.

¹¹ See “Configuration register” for detailed explanation of the dump sequence.

¹² The broadcast packet is written to broadcast bus

EBCRST

Event and bunch counter reset: an event and bunch counter reset is performed.

ECRST

Event counter reset: an event counter reset is performed.

ERDUMP

Error dump: the internal error counters are dumped on the external data bus. For this operation the data qualifier bits are used as follows:

DQ	Data bus content
0001	Single Bit Error Counter Low
0010	Single Bit Error Counter High
0011	Double Bit Error Counter Low
0100	Double Bit Error Counter High

Data are output in the external data bus in consecutive clock cycles. As for a normal data transfer, the data strobe line (DoutStr) signals the presence of valid data on the bus and the DQ bits indicate the status in the error dump sequence.

CRDUMP

Configuration register dump: The internal configuration and control registers are dumped on the external data bus. For this operation the data qualifier bits are used as follows:

DQ	Data bus content
0101	Fine Delay register 1
0110	Fine Delay register 2
0111	Coarse Delay register
1000	Control register
1001	Configuration register bit <7:0>
1010	Configuration register bit <15:8>
1011	Configuration register bit <23:16>
1100	Configuration register bit <31:24>

INIT

This instruction performs a warm re-initialisation of the TTCrx. Since in order to be recognised, this instruction requires a working analogue front end, re-initialisation is limited to the digital part of the TTCrx (no PLL re-initialisation).

USER

User defined command: this instruction sets the two user defined external broadcast pins to the data received in the user defined part of a broadcast command.

Chapter 6

Receiver Operation

TTCrx OPERATION

Reset sequence

To initialise the TTCrx after a power on, the reset_b pin is activated. This active low signal reinitialises the TTCrx completely. Upon completion of the initialisation sequence the TTCrx activates the TTCReady signal. The external reset signal forces the TTCrx to go through a complete re-synchronisation sequence and reloads all the system parameters from the serial PROM. The resynchronisation sequence can take up to 25 μ sec.

A TTCrx cold re-initialisation is performed every time the internal PLL lock signal is lost.

INIT sequence

A warm re-initialisation sequence is performed each time an INIT broadcast command is received. The re-initialisation sequence is limited to the digital part of the TTCrx. During execution the external serial PROM is read, channels A and B identified, and frame synchronisation acquired. At the end of the re-initialisation the TTCReady pin is asserted.

L1A sequence

On reception of an L1Accept signal on the A channel, the TTCrx outputs the following sequence of signals on the respective pins:

Control Register, bit <1:0>	Cycle	Sequence
00	0	Event counter low on bunch counter bus
01	0	Bunch counter on bunch counter bus
10	0	Event counter low on bunch counter bus
	1	Event counter high on bunch counter bus
11	0	Bunch counter on bunch counter bus
	1	Event counter low on bunch counter bus
	2	Event counter high on bunch counter bus

The number of cycles depends on the setting of the two low bits in the control register, as explained in "Control register".

Broadcast sequence

The content of the received broadcast command is output on the broadcast bus (Brcst<7:2>). The strobe lines BrcstStr1 and BrcstStr2 are activated (for a clock period) after the delays specified in the coarse delay register have elapsed.

Data sequence.

Upon reception of an individually-addressed commands/data frame, its data content is output on the data bus (Dout<7:0>) and its subaddress content on the subaddress bus (SubAddr<7:0>). The data qualifier bits (DQ<3:0>) are set to "0" to indicate data transmission and the data strobe line (DoutStr) is set to indicate valid data during a clock cycle. When the received command is intended for the internal addressing space the strobe line DoutStr is not activated and the contents of the data and subaddress buses remain unchanged.

TTCrx configuration

In order to adapt the operation of the TTCrx to different environments, several optional features can be programmed after reset by reading an external serial PROM. The TTCrx uses three dedicated pins (PromReset, PromClk and PromD) to implement a serial protocol identical to the one used in devices such as the Xilinx 1736 or equivalent. The user is referred to the data sheets of this product for detailed information [5].

In addition to containing configuration parameters, the serial PROM is also used to store testing parameters. These parameters have been specified in section "TTCrx registers". ***With the exception of the user defined parameters, the configuration register recommended parameters should never be modified by the user.***

Chapter 7

TTCrx Signals and Timing

This chapter describes the TTCrx external signals and the most important timing relations among these signals.

TTCrx EXTERNAL SIGNALS

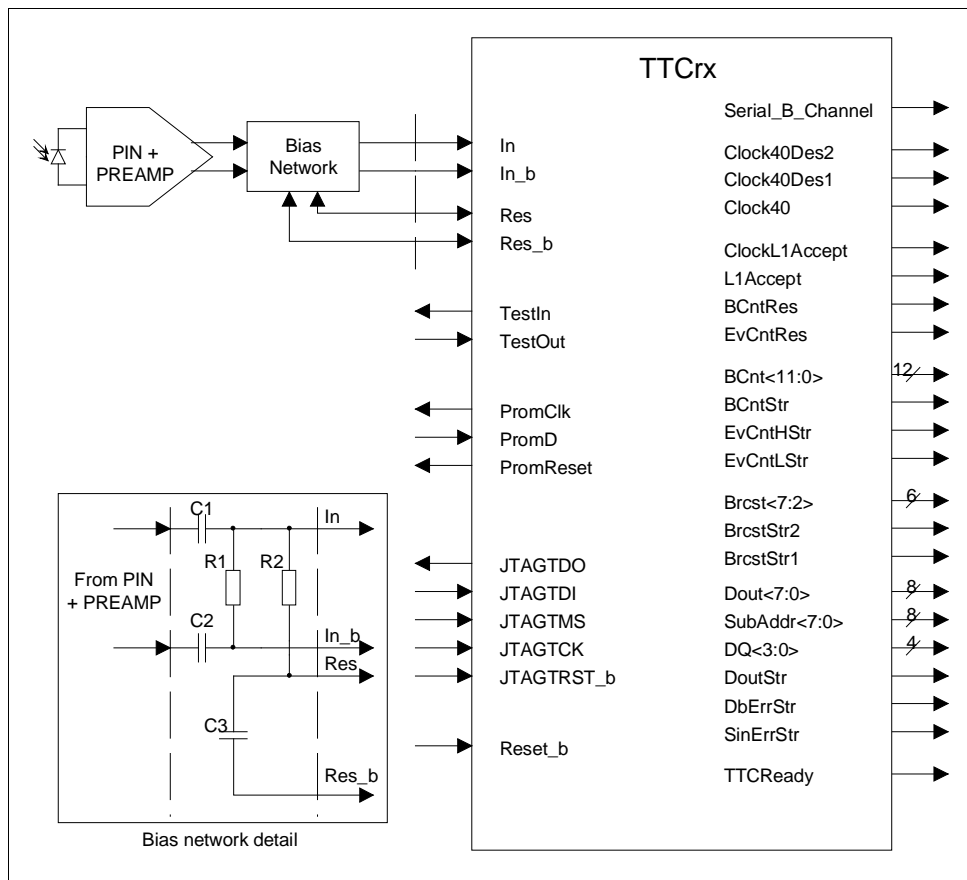


Figure 5 TTCrx external signals and analogue inputs bias arrangement.

The TTCrx signals available to the user and the bias arrangement required for interfacing with the photodetector-preamplifier are represented in Figure 5. A description of the functionality of each individual signal is given next.

TTCrx signals

TestIn

Full custom/standard cells test input.

TestOut

Full custom/standard cells test output.

BCnt<11:0>

Bunch counter output bus. This bus usually reflects the content of the bunch counter register. After a first level trigger accept decision it can be optionally used to provide the event number. Its mode of operation is controlled by the control register and its data type is validated by the signals BCntStr, EvCntHStr and EvCntLStr.

BCntRes

Bunch counter reset signal. Indicates a bunch counter reset. As the L1Accept signal, its deskewing is controlled by bits <3:0> in the coarse delay register and by the content of the fine delay register with subaddress "0". See "Coarse delay register" and "Fine delay registers".

BCntStr

Bunch counter strobe. Indicates that a bunch number is present on the output BCnt<11:0> bus.

Brcst<7:6>

Broadcast commands/data output bus. User defined part of a broadcast message. See "Broadcast commands/data".

Brcst<5:2>

Broadcast commands/data output bus. System wide part of a broadcast message. See "Broadcast commands/data".

BrcstStr1

Broadcast messages strobe 1. The total amount of deskewing applied to this strobe signal is controlled by bits <3:0> of the coarse delay register (see "Coarse delay register").

BrcstStr2

Broadcast messages strobe 2. The total amount of deskewing applied to this strobe signal is controlled by bits <7:4> of the coarse delay register (see "Coarse delay register").

Clock40

LHC 40.08 MHz non-deskewed reference clock signal. This output can be enabled/disabled by writing into the "control register".

Clock40Des1

LHC 40.08 MHz deskewed reference clock 1. The deskewing factor is controlled by writing into the TTCrx subaddress “0” (see “Fine delay registers”).

Clock40Des2

LHC 40.08 MHz deskewed reference clock 2. The deskewing factor is controlled by writing into the TTCrx subaddress “1” (see “Fine delay registers”). It is enabled by bit number 20 in the configuration register.

ClockL1Accept

This signal combines the non-deskewed clock and the first level trigger-accept information. The signal is coded such that, in absence of a first level trigger-accept decision it is identical to the Clock40 signal. When a valid first level trigger-accept decision occurs the clock signal is suppressed (logic level “0”) during a clock cycle. This signal is enabled by bit number 22 in the configuration register.

DbErrStr

Double error or frame error strobe. Indicates that a double error or a frame error has occurred.

Dout<7:0>

Data bus. This bus is normally used to output the data content of an individually-addressed commands/data. However, it is also used for dumping the contents of the internal error counters and of the configuration register (see “ERDUMP” and “CRDUMP”). The type of data present in the bus is validated by signals DQ<3:0>. Bus operation can be enable/disabled by writing into the control register.

DQ<3:0>

Data qualifier bits. This bus indicates the type of data present on the data bus register (see “ERDUMP” and “CRDUMP”).

DoutStr

Data out strobe. Indicates valid data on the data bus.

EvCntHStr

Event counter high word strobe. Indicates that the output bus BCnt<11:0> contains the high word of the event number.

EvCntLStr

Event counter low word strobe. Indicates that the output bus BCnt<11:0> contains the low word of the event number.

EvCntRes

Event counter reset signal. Indicates an event counter reset. As the L1Accept signal, its deskewing is controlled by bits <3:0> in the coarse delay register and by the content of the fine delay register with subaddress “0”. See “Coarse delay register” and “Fine delay registers”.

In and In_b

Differential analogue input. Signals **In** and **In_b** interface with the photodetector-preamplifier using the bias network detailed in Figure 5. Correct operation of the TTCrx IC requires the peak to peak amplitude of the input differential signal to be within 5 mV_{pp} and 2 V_{pp}. The input signal has to be BiPhase Mark encoded (see “TTC system overview”) and the frame formats specified in sections “TTC system overview” and “Frame formats” have to be respected for correct receiver operation.

JTAGTCK

JTAG test clock.

JTAGTDI

JTAG test data in.

JTAGTDO

JTAG test data out.

JTAGTMS

JTAG test mode select.

JTAGTRST_b

JTAG test reset

L1Accept

First level trigger-accept signal. The total amount of deskewing applied to this signal is controlled by bits <3:0> in the coarse delay register and by the content of the fine delay register with subaddress “0”. See “Coarse delay register” and “Fine delay registers”.

PromClock

Serial configuration PROM clock signal. See “Individual addressing”, “Configuration register” and reference [5].

PromD

Serial configuration PROM reset signal. See “Individual addressing”, “Configuration register” and reference [5].

PromReset

Serial configuration PROM data output. See “Individual addressing”, “Configuration register” and reference [5].

Reset_b

Active low reset signal. See “Reset sequence”.

Res an Res_b

Analogue input bias. See inset in Figure 5 for details on the bias circuit.

Serial_B_Channel

This signal is used to make available to the users the serial data received on channel B (including frame, start and stop bits) The bit rate is 40.08 Mbit/s. This output can be enabled/disabled by writing into the control register.

SinErrStr

Single error strobe. Indicates that a single error has occurred.

SubAddr<7:0>

Subaddress bus. Used to output the subaddress content of an individually address commands/data. Bus operation can be enable/disabled by writing into the control register.

TTCReady

TTCrx ready.

VcoOn

A logic "0" in this pin disables the PLL VCO. This input contains a pull up resistor so that when the signal is not connected the VCO will be enabled. This signal is used for test purposes only and is not available in the package as a physical pin (bond pad only).

TTCrx TIMING

The general timing relations among the TTCrx output signals are illustrated in Figure 6. The timing relations among some of these signals can be modified by the user. The internal registers that control the TTCrx timing are: the coarse delay register and the fine delay registers 1 and 2. The contents of these registers can be modified using individually-addressed commands/data as explained in sections “TTCrx registers” and “Broadcast commands/data”

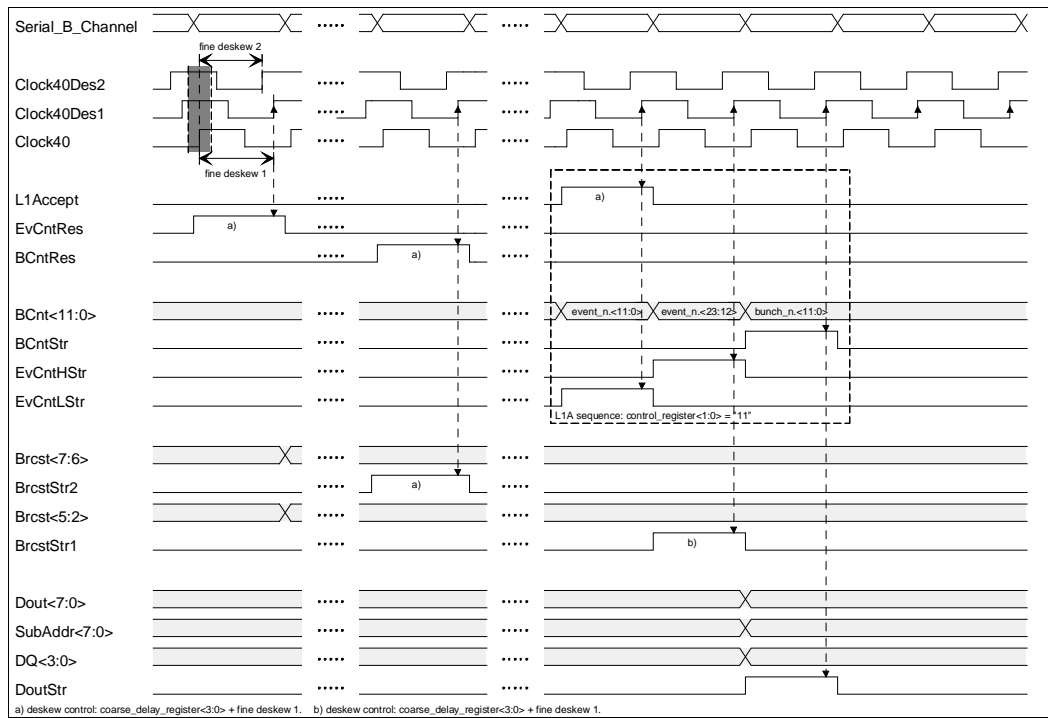


Figure 6 TTCrx timing

Signals L1Accept, EvCntRes, BCntRes BrcstStr1 and BrcstStr2 are used for purposes of system synchronisation. These signals do not convey any precise timing information on their own. Accurate timing information is only obtained when these signals are used in combination with the clock signal Clock40Des1. The rising edge of this clock signal marks the instant when those signals are valid. This is illustrated in Figure 7 for the BrcstStr1 signal.

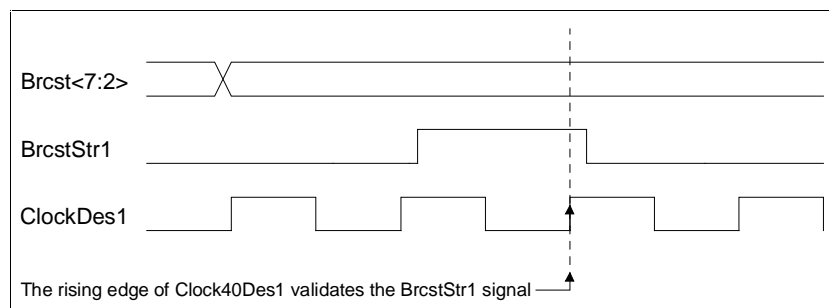


Figure 7 Timing validation example

Note that the contents of the buses Brcst<7:2>, Dout<7:0>, SubAddr<7:0> and DQ<3:0> is modified as soon as the corresponding data is received by the TTCrx IC.

However, The validity of the contents of these buses is only asserted by the corresponding strobe signal together with the rising edge of the Clock40Des1 signal.

Trigger latency

The TTCrx trigger latency has now been reduced to 100 ns. This value does not take into account any other contributions to the system latency such as the delay in the optical fibres, optical-preamplifier or in the TTC transmitter. Figure 1 illustrates the definition used to measure the trigger latency.

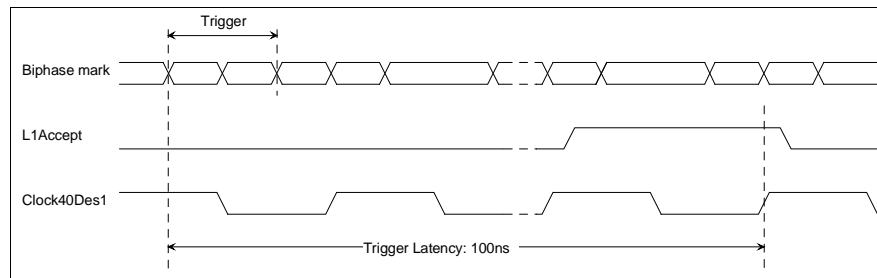


Figure 8 Trigger latency

Chapter 8

TTCrx Packaging and Pin Assignments

The TTCrx has been packaged in a 100-pin BGA 15 mm side package. The BGA package physical outline and pin assignments are specified in this chapter.

TTCrx PACKAGE

Physical outline

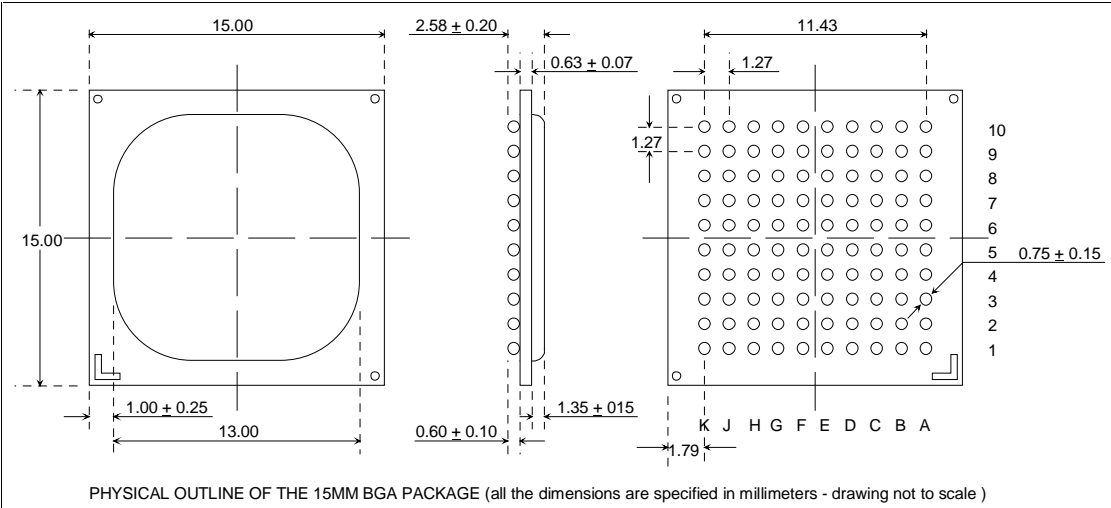


Figure 9 TTCrx package physical outline (drawing not to scale)

Pin assignments

The following two tables list the IC pin names and numbers sorted by bond pad number on the chip and by module ball position on the package.

Pin assignments: sorted by IC bonding pad number

IC B. Pad #	PIN #	Name	Type	Description
1	A 02	Reset_b	in	General reset input
2	B 02	PromD	in	Serial Prom data
3	A 01	PromClk	out	Serial Prom clock
4	C 02	PromReset	out	Serial Prom CE* and reset
5	B 01	TTCReady	out	TTCCrx is ready and stable
6	D 03	D_VDD	pwr	Digital supply (I/O)
7	C 01	D_GND	pwr	Digital ground (I/O)
8	D 02	D_VDD	pwr_core	Digital supply (core)
9	E 04	D_GND	pwr_core	Digital ground (core)
10	E 03	A_GND	pwr	Analogue ground
11	D 01	In_b	in	Input from PIN receiver -
12	E 01	In	in	Input from PIN receiver +
13	F 05	Res_b	in	Biasing input-
14	E 02	Res	in	Biasing input+
15	F 01	A_VDD	pwr	Analogue supply
16	F 02	D_VDD	pwr	Digital supply (I/O)
17	F 03	D_GND	pwr	Digital ground (I/O)
18	F 04	D_VDD	pwr_core	
19	G 01	D_GND	pwr_core	
20	G 02	TestIn	in	full custom/standard cells test in
21	G 03	TestOut	out	full custom/standard cells test out
22	N.C.	VcoOn	in	VCO enable in (no package pin)
23	H 01	JTAGTDO	out	JTAG data out
24	H 02	JTAGTDI	in	JTAG data in
25	J 01	JTAGTMS		JTAG mode select
26	H 03	JTAGTCK	in	JTAG clock
27	K 01	JTAGTRST_b	in	JTAG reset
28	J 03	Serial_B_Channel	out	Serial B channel
29	J 02	BCnt<11>	out	Bunch counter / Ev Counter bus
30	K 02	BCnt<10>	out	Bunch counter / Ev Counter bus
31	G 04	D_VDD	pwr	Digital supply (I/O)
32	H 04	D_GND	pwr	Digital ground (I/O)
33	K 03	BCnt<9>	out	Bunch counter / Ev Counter bus
34	J 04	BCnt<8>	out	Bunch counter / Ev Counter bus
35	H 05	BCnt<7>	out	Bunch counter / Ev Counter bus
36	G 05	BCnt<6>	out	Bunch counter / Ev Counter bus
37	K 04	BCnt<5>	out	Bunch counter / Ev Counter bus
38	J 05	BCnt<4>	out	Bunch counter / Ev Counter bus
39	H 06	BCnt<3>	out	Bunch counter / Ev Counter bus
40	K 05	BCnt<2>	out	Bunch counter / Ev Counter bus
41	K 06	BCnt<1>	out	Bunch counter / Ev Counter bus
42	F 06	BCnt<0>	out	Bunch counter / Ev Counter bus
43	H 07	D_VDD	pwr	Digital supply (I/O)
44	J 06	D_GND	pwr	Digital ground (I/O)
45	G 06	BCntStr	out	Bunch counter strobe
46	K 07	EvCntHStr	out	Event counter high strobe
47	H 08	EvCntLStr	out	Event counter low strobe
48	J 07	BCntRes	out	Bunch counter reset
49	J 08	EvCntRes	out	Event counter reset strobe
50	K 08	L1Accept	out	L1 accept strobe
51	K 09	Brcst<7>	out	User defined broadcast bus

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52	J 09	Brcst<6>	out	User defined broadcast bus
53	K 10	BrcstStr2	out	Strobe for user defined broadcast
54	H 09	Brcst<5>	out	System broadcast bus
55	J 10	Brcst<4>	out	System broadcast bus
56	H 10	D_VDD	pwr_core	Digital supply (core)
57	G 08	D_VDD	pwr	Digital supply (I/O)
58	G 07	D_GND	pwr	Digital ground (I/O)
59	G 09	D_VDD_C	pwr special	
60	F 08	Clock40	out	40.08 MHz clock
61	G 10	D_GND_C	pwr special	
62	F 07	D_VDD_C	pwr special	Digital supply (I/O)
63	F 09	Clock40Des1	out	Deskewed 40.08 MHz clock 1
64	E 06	D_GND_C	pwr special	Digital ground (I/O)
65	E 08	D_VDD_C	pwr special	Digital supply (I/O)
66	F 10	Clock40Des2	out	Deskewed 40.08 MHz clock 2
67	E 10	ClockL1Accept	out	Clock/Trigger output
68	E 07	D_GND_C	pwr special	Digital ground (I/O)
69	D 08	D_VDD	pwr	Digital supply (I/O)
70	E 09	D_GND	pwr	Digital ground (I/O)
71	D 10	D_GND	pwr_core	Digital ground (core)
72	C 08	Brcst<3>	out	System broadcast bus
73	D 09	Brcst<2>	out	System broadcast bus
74	C 10	BrcstStr1	out	Strobe for system broadcast bus
75	C 09	SinErrStr	out	Single bit error strobe
76	B 10	DbErrStr	out	Double bit error strobe
77	B 09	SubAddr<0>	out	External subaddress bus
78	A 10	SubAddr<1>	out	External subaddress bus
79	B 08	SubAddr<2>	out	External subaddress bus
80	A 09	SubAddr<3>	out	External subaddress bus
81	A 08	SubAddr<4>	out	External subaddress bus
82	D 07	D_GND	pwr	Digital ground (I/O)
83	C 07	D_VDD	pwr	Digital supply (I/O)
84	C 06	SubAddr<5>	out	External subaddress bus
85	D 06	SubAddr<6>	out	External subaddress bus
86	E 05	SubAddr<7>	out	External subaddress bus
87	B 07	DQ<0>	out	Data qualifier
88	A 07	DQ<1>	out	Data qualifier
89	C 05	DQ<2>	out	Data qualifier
90	B 06	DQ<3>	out	Data qualifier
91	A 06	DoutStr	out	Data strobe
92	A 05	Dout<0>	out	Data output bus
93	C 04	Dout<1>	out	Data output bus
94	B 05	D_GND	pwr	Digital ground (I/O)
95	A 04	D_VDD	pwr	Digital supply (I/O)
96	D 05	Dout<2>	out	Data output bus
97	C 03	Dout<3>	out	Data output bus
98	D 04	Dout<4>	out	Data output bus
99	B 04	Dout<5>	out	Data output bus
100	A 03	Dout<6>	out	Data output bus
101	B 03	Dout<7>	out	Data output bus

Pin assignments: sorted by pin number

IC B. Pad #	PIN #	Name	Type	Description
3	A 01	PromClk	out	Serial Prom clock
1	A 02	Reset_b	in	General reset input
100	A 03	Dout<6>	out	Data output bus
95	A 04	D_VDD	pwr	Digital supply (I/O)
92	A 05	Dout<0>	out	Data output bus
91	A 06	DoutStr	out	Data strobe
88	A 07	DQ<1>	out	Data qualifier
81	A 08	SubAddr<4>	out	External subaddress bus
80	A 09	SubAddr<3>	out	External subaddress bus
78	A 10	SubAddr<1>	out	External subaddress bus
5	B 01	TTCReady	out	TTCrX is ready and stable
2	B 02	PromD	in	Serial Prom data
101	B 03	Dout<7>	out	Data output bus
99	B 04	Dout<5>	out	Data output bus
94	B 05	D_GND	pwr	Digital ground (I/O)
90	B 06	DQ<3>	out	Data qualifier
87	B 07	DQ<0>	out	Data qualifier
79	B 08	SubAddr<2>	out	External subaddress bus
77	B 09	SubAddr<0>	out	External subaddress bus
76	B 10	DbErrStr	out	Double bit error strobe
7	C 01	D_GND	pwr	Digital ground (I/O)
4	C 02	PromReset	out	Serial Prom CE* and reset
97	C 03	Dout<3>	out	Data output bus
93	C 04	Dout<1>	out	Data output bus
89	C 05	DQ<2>	out	Data qualifier
84	C 06	SubAddr<5>	out	External subaddress bus
83	C 07	D_VDD	pwr	Digital supply (I/O)
72	C 08	Brcst<3>	out	System broadcast bus
75	C 09	SinErrStr	out	Single bit error strobe
74	C 10	BrcstStr1	out	Strobe for system broadcast bus
11	D 01	In_b	in	Input from PIN receiver -
8	D 02	D_VDD	pwr_core	Digital supply (core)
6	D 03	D_VDD	pwr	Digital supply (I/O)
98	D 04	Dout<4>	out	Data output bus
96	D 05	Dout<2>	out	Data output bus
85	D 06	SubAddr<6>	out	External subaddress bus
82	D 07	D_GND	pwr	Digital ground (I/O)
69	D 08	D_VDD	pwr	Digital supply (I/O)
73	D 09	Brcst<2>	out	System broadcast bus
71	D 10	D_GND	pwr_core	Digital ground (core)
12	E 01	In	in	Input from PIN receiver +
14	E 02	Res	in	Biasing input+
10	E 03	A_GND	pwr	Analogue ground
9	E 04	D_GND	pwr_core	Digital ground (core)
86	E 05	SubAddr<7>	out	External subaddress bus
64	E 06	D_GND_C	pwr special	Digital ground (I/O)
68	E 07	D_GND_C	pwr special	Digital ground (I/O)
65	E 08	D_VDD_C	pwr special	Digital supply (I/O)
70	E 09	D_GND	pwr	Digital ground (I/O)
67	E 10	ClockL1Accept	out	Clock/Trigger output
15	F 01	A_VDD	pwr	Analogue supply

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16	F 02	D_VDD	pwr	Digital supply (I/O)
17	F 03	D_GND	pwr	Digital ground (I/O)
18	F 04	D_VDD	pwr_core	
13	F 05	Res_b	in	Biasing input-
42	F 06	BCnt<0>	out	Bunch counter / Ev Counter bus
62	F 07	D_VDD_C	pwr special	Digital supply (I/O)
60	F 08	Clock40	out	40.08 MHz clock
63	F 09	Clock40Des1	out	Deskewed 40.08 MHz clock 1
66	F 10	Clock40Des2	out	Deskewed 40.08 MHz clock 2
19	G 01	D_GND	pwr_core	
20	G 02	TestIn	in	full custom/standard cells test in
21	G 03	TestOut	out	full custom/standard cells test out
31	G 04	D_VDD	pwr	Digital supply (I/O)
36	G 05	BCnt<6>	out	Bunch counter / Ev Counter bus
45	G 06	BCntStr	out	Bunch counter strobe
58	G 07	D_GND	pwr	Digital ground (I/O)
57	G 08	D_VDD	pwr	Digital supply (I/O)
59	G 09	D_VDD_C	pwr special	
61	G 10	D_GND_C	pwr special	
23	H 01	JTAGTDO	out	JTAG data out
24	H 02	JTAGTDI	in	JTAG data in
26	H 03	JTAGTCK	in	JTAG clock
32	H 04	D_GND	pwr	Digital ground (I/O)
35	H 05	BCnt<7>	out	Bunch counter / Ev Counter bus
39	H 06	BCnt<3>	out	Bunch counter / Ev Counter bus
43	H 07	D_VDD	pwr	Digital supply (I/O)
47	H 08	EvCntLStr	out	Event counter low strobe
54	H 09	Brcst<5>	out	System broadcast bus
56	H 10	D_VDD	pwr_core	Digital supply (core)
25	J 01	JTAGTMS		JTAG mode select
29	J 02	BCnt<11>	out	Bunch counter / Ev Counter bus
28	J 03	Serial_B_Channel	out	Serial B channel
34	J 04	BCnt<8>	out	Bunch counter / Ev Counter bus
38	J 05	BCnt<4>	out	Bunch counter / Ev Counter bus
44	J 06	D_GND	pwr	Digital ground (I/O)
48	J 07	BCntRes	out	Bunch counter reset
49	J 08	EvCntRes	out	Event counter reset strobe
52	J 09	Brcst<6>	out	User defined broadcast bus
55	J 10	Brcst<4>	out	System broadcast bus
27	K 01	JTAGTRST_b	in	JTAG reset
30	K 02	BCnt<10>	out	Bunch counter / Ev Counter bus
33	K 03	BCnt<9>	out	Bunch counter / Ev Counter bus
37	K 04	BCnt<5>	out	Bunch counter / Ev Counter bus
40	K 05	BCnt<2>	out	Bunch counter / Ev Counter bus
41	K 06	BCnt<1>	out	Bunch counter / Ev Counter bus
46	K 07	EvCntHStr	out	Event counter high strobe
50	K 08	L1Accept	out	L1 accept strobe
51	K 09	Brcst<7>	out	User defined broadcast bus
53	K 10	BrcstStr2	out	Strobe for user defined broadcast
22	N.C.	VcoOn	in	VCO enable in (no package pin)

Chapter 9

JTAG Boundary-Scan

The TTCrx implements a subset of the JTAG/IEEE 1149.1 standard (see for instance [6]) providing the capability for board-level connectivity tests. The complete set of Test Access Port control signals (including TRST) is implemented in the TTCrx. The JTAG logic includes a Device Identification Register and the device identification number is:

ID = "0000008F" (HEX)

BOUNDARY SCAN REGISTER

The Boundary Scan Register (BSR) includes all the I/O signals with exception of the analogue signals. Interface signals between the full custom part and the standard cells part of the design are also included in the BSR.

Boundary scan register read out order

Order	PIN #	Name	Type	Description
1	B 01	TTCReady	out	TTCrx is ready and stable
2	G 03	TestOut	out	full custom/standard cells test out
3	A 01	PromClk	out	Serial Prom clock
4	C 02	PromReset	out	Serial Prom CE* and reset
5	J 03	Serial_B_Channel	out	Serial B channel
6	C 09	SinErrStr	out	Single bit error strobe
7	B 10	DbErrStr	out	Double bit error strobe
8	F 08	Clock40	out	40.08 MHz clock
9	F 09	Clock40Des1	out	Deskewed 40.08 MHz clock 1
10	F 10	Clock40Des2	out	Deskewed 40.08 MHz clock 2
11	E 10	ClockL1Accept	out	Clock/Trigger output
12	C 10	BrcstStr1	out	Strobe for system broadcast bus
13	K 10	BrcstStr2	out	Strobe for user defined broadcast
14	J 07	BCntRes	out	Bunch counter reset
15	J 08	EvCntRes	out	Event counter reset strobe
16	D 09	Brcst<2>	out	User defined broadcast bus
17	C 08	Brcst<3>	out	User defined broadcast bus
18	J 10	Brcst<4>	out	System broadcast bus
19	H 09	Brcst<5>	out	System broadcast bus
20	J 09	Brcst<6>	out	System broadcast bus
21	K 09	Brcst<7>	out	System broadcast bus
22	K 08	L1Accept	out	L1 accept strobe
23	K 07	EvCntHStr	out	Event counter high strobe
24	H 08	EvCntLStr	out	Event counter low strobe
25	G 06	BCntStr	out	Bunch counter strobe
26	F 06	BCnt<0>	out	Bunch counter / Ev Counter bus
27	K 06	BCnt<1>	out	Bunch counter / Ev Counter bus
28	K 05	BCnt<2>	out	Bunch counter / Ev Counter bus
29	H 06	BCnt<3>	out	Bunch counter / Ev Counter bus

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30	J 05	BCnt<4>	out	Bunch counter / Ev Counter bus
31	K 04	BCnt<5>	out	Bunch counter / Ev Counter bus
32	G 05	BCnt<6>	out	Bunch counter / Ev Counter bus
33	H 05	BCnt<7>	out	Bunch counter / Ev Counter bus
34	J 04	BCnt<8>	out	Bunch counter / Ev Counter bus
35	K 03	BCnt<9>	out	Bunch counter / Ev Counter bus
36	K 02	BCnt<10>	out	Bunch counter / Ev Counter bus
37	J 02	BCnt<11>	out	Bunch counter / Ev Counter bus
38	A 06	DoutStr	out	Data strobe
39	B 09	SubAddr<0>	out	External subaddress bus
40	A 10	SubAddr<1>	out	External subaddress bus
41	B 08	SubAddr<2>	out	External subaddress bus
42	A 09	SubAddr<3>	out	External subaddress bus
43	A 08	SubAddr<4>	out	External subaddress bus
44	C 06	SubAddr<5>	out	External subaddress bus
45	D 06	SubAddr<6>	out	External subaddress bus
46	E 05	SubAddr<7>	out	External subaddress bus
47	A 05	Dout<0>	out	Data output bus
48	C 04	Dout<1>	out	Data output bus
49	D 05	Dout<2>	out	Data output bus
50	C 03	Dout<3>	out	Data output bus
51	D 04	Dout<4>	out	Data output bus
52	B 04	Dout<5>	out	Data output bus
53	A 03	Dout<6>	out	Data output bus
54	B03	Dout<7>	out	Data output bus
55	B 07	DQ<0>	out	Data qualifier
56	A 07	DQ<1>	out	Data qualifier
57	C 05	DQ<2>	out	Data qualifier
58	B 06	DQ<3>	out	Data qualifier
59	-	clk	out	Internal node
60	-	a	out	Internal node
61	-	b	out	Internal node
62	-	lock	out	Internal node
63	A 02	Reset_b	in	General reset input
64	G 02	TestIn	in	full custom/standard cells test in
65	B 02	PromD	in	Serial Prom data
66	-	VcoOn	in	VCO enable in (no package pin)

Appendix A

Fine Deskew Mapping Table

Due to the vernier principle used in the fine deskew DLL there is no direct correspondence between the value programmed in the fine deskew register and the resulting delay. In this appendix, an unfolding mapping table for fine deskew programming is given.

FINE DESKEW PRINCIPLE

In order to obtain a sub-gate delay resolution an architecture based on two staggered delay locked loops is used in the TTCrx. Its principle of operation can be easily understood with reference to Figure 10. In this scheme, a first DLL generates N replicas of the recovered clock each one of them delayed by $\Delta t_N = T/N$ seconds from the previous one, where T is the recovered clock period. One of these signals is selected as the input to the following delay locked loop. A second DLL generates $N-1$ copies of the clock signal but this time $\Delta t_{(N-1)} = T/(N-1)$ seconds apart. By appropriate output tap selection in each DLL the clock signal can be shifted with a time resolution that is given by: $\Delta t = \Delta t_{(N-1)} - \Delta t_N$

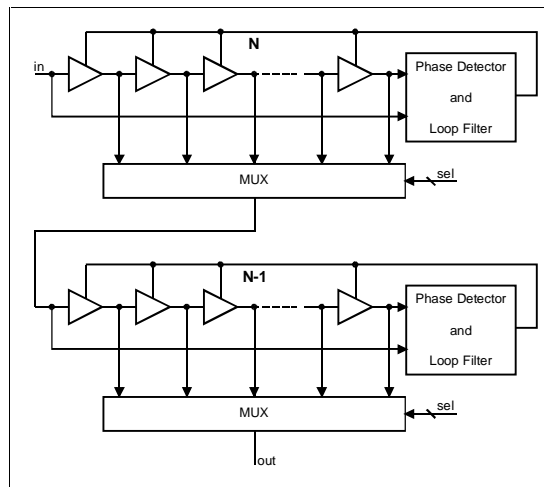


Figure 10 Fine deskew delay generator architecture

In the TTCrx $N=16$ was used resulting in a minimum time step of 104.17 ps. If the desired fine delay is $K \times \Delta t$ (where K is an integer between 0 and 239) then, the corresponding “unfolding” number to be programmed in the fine delay register should be selected according to the table below.

Unfolding Table

K	Unfolding Number
0	0
1	31
2	46

3	61
4	76
5	91
6	106

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7	121
8	136
9	151
10	166
11	181
12	196
13	211
14	226
15	1
16	16
17	47
18	62
19	77
20	92
21	107
22	122
23	137
24	152
25	167
26	182
27	197
28	212
29	227
30	2
31	17
32	32
33	63
34	78
35	93
36	108
37	123
38	138
39	153
40	168
41	183
42	198
43	213
44	228
45	3
46	18
47	33
48	48
49	79
50	94
51	109
52	124
53	139
54	154
55	169
56	184
57	199
58	214
59	229
60	4
61	19
62	34
63	49
64	64
65	95
66	110
67	125

68	140
69	155
70	170
71	185
72	200
73	215
74	230
75	5
76	20
77	35
78	50
79	65
80	80
81	111
82	126
83	141
84	156
85	171
86	186
87	201
88	216
89	231
90	6
91	21
92	36
93	51
94	66
95	81
96	96
97	127
98	142
99	157
100	172
101	187
102	202
103	217
104	232
105	7
106	22
107	37
108	52
109	67
110	82
111	97
112	112
113	143
114	158
115	173
116	188
117	203
118	218
119	233
120	8
121	23
122	38
123	53
124	68
125	83
126	98
127	113
128	128

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129	159
130	174
131	189
132	204
133	219
134	234
135	9
136	24
137	39
138	54
139	69
140	84
141	99
142	114
143	129
144	144
145	175
146	190
147	205
148	220
149	235
150	10
151	25
152	40
153	55
154	70
155	85
156	100
157	115
158	130
159	145
160	160
161	191
162	206
163	221
164	236
165	11
166	26
167	41
168	56
169	71
170	86
171	101
172	116
173	131
174	146
175	161
176	176
177	207
178	222
179	237
180	12
181	27
182	42
183	57
184	72
185	87

186	102
187	117
188	132
189	147
190	162
191	177
192	192
193	223
194	238
195	13
196	28
197	43
198	58
199	73
200	88
201	103
202	118
203	133
204	148
205	163
206	178
207	193
208	208
209	239
210	14
211	29
212	44
213	59
214	74
215	89
216	104
217	119
218	134
219	149
220	164
221	179
222	194
223	209
224	224
225	15
226	30
227	45
228	60
229	75
230	90
231	105
232	120
233	135
234	150
235	165
236	180
237	195
238	210
239	225

Appendix B

TTCrx Test Board

To facilitate testing of the current TTCrx version a PCB test board was designed and manufactured. It is available to designers wishing to integrate the TTCrx IC in their systems. The TTCrx test board is described in this appendix.

TEST BOARD

The TTCrx test board schematic is shown in Figure 11 and the placement of components in the board is represented in Figure 12 and Figure 13. The test board contains the TTCrx IC, an integrated detector/preamplifier (Honeywell Figure 15), a serial configuration PROM (XC1736D), a fibre optic post-amplifier (NE5225D) and an ECL to TTL converter (10H125). This arrangement allows the TTCrx to be used with

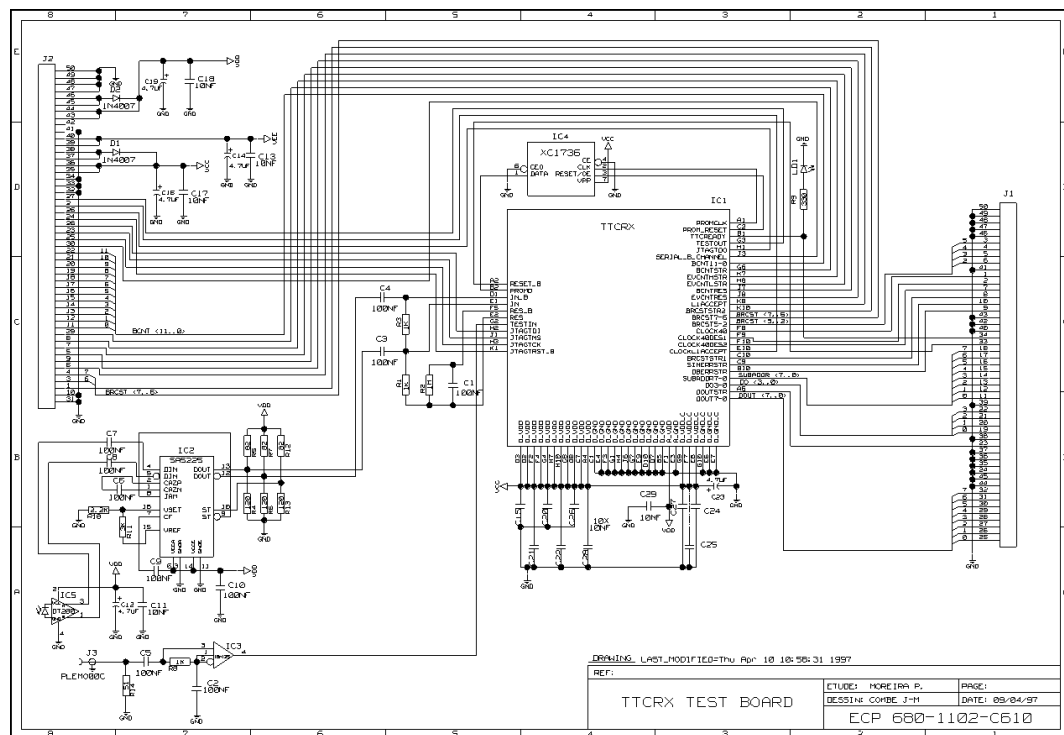


Figure 11 TTCrx test board schematic

either an optical signal, using the optical preamplifier, or with an electrical signal, using the pseudo ECL electrical input. The electrical input is terminated with a 50Ω resistor to ground and the signal is AC coupled to the ECL/TTL converter input. To enable operation using this input, bit number 25 ("ref_gen_mux") in the serial configuration PROM has to be set to "1"¹³.

¹³ For more information on the serial configuration PROM programming see "Configuration register"

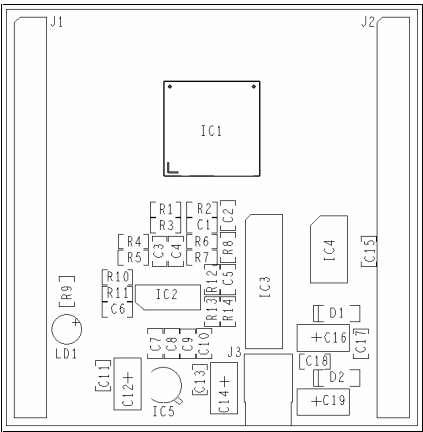


Figure 12 Components placement (C. side)

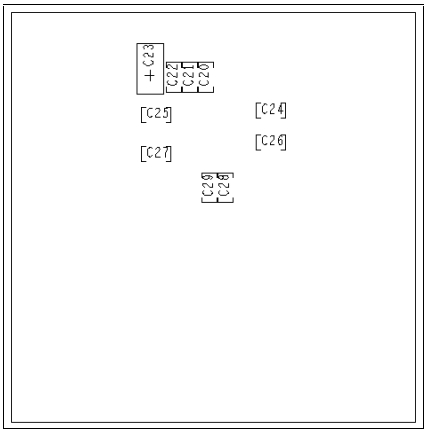


Figure 13 Components placement (W. side)

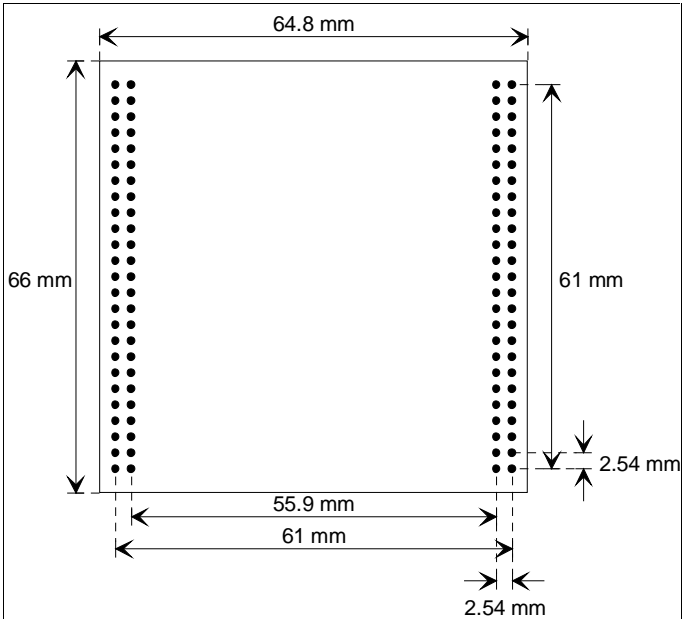


Figure 14 Test board dimensions

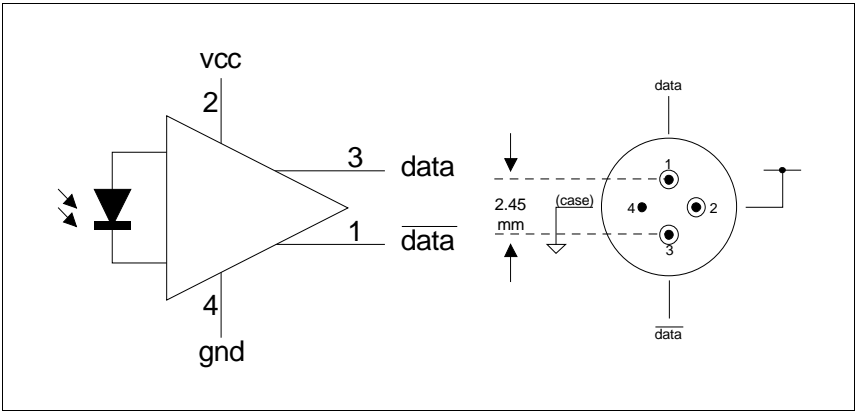


Figure 15 Honeywell pin-preamplifier pin assignments and footprint

Test board pin assignments

Connector J1

Pin #	Name
1	Clock40
2	Clock40Des1
3	Brcst<5>
4	Brcst<4>
5	Brcst<3>
6	Brcst<2>
7	Clock40Des2
8	BrcstStr1
9	DbErrStr
10	SinErrStr
11	SubAddr<0>
12	SubAddr<1>
13	SubAddr<2>
14	SubAddr<3>
15	SubAddr<4>
16	SubAddr<5>
17	SubAddr<6>
18	SubAddr<7>
19	DQ<0>
20	DQ<1>
21	DQ<2>
22	DQ<3>
23	DoutStr
24	GND
25	Dout<0>
26	Dout<1>
27	Dout<2>
28	Dout<3>
29	Dout<4>
30	Dout<5>
31	Dout<6>
32	Dout<7>
33	Reset b
34	TTCReady
35	GND
36	GND
37	GND
38	GND
39	GND
40	GND
41	GND
42	GND
43	GND
44	GND
45	GND
46	GND
47	GND
48	GND
49	GND
50	GND

Connector J2

Pin #	Name
1	BrcstStr2
2	ClockL1Accept
3	Brcst<6>
4	Brcst<7>
5	EvCntRes
6	L1Accept
7	EvCntLStr
8	EvCntHStr
9	BCntRes
10	GND
11	BCnt<0>
12	BCnt<1>
13	BCnt<2>
14	BCnt<3>
15	BCnt<4>
16	BCnt<5>
17	BCnt<6>
18	BCnt<7>
19	BCnt<8>
20	BCnt<9>
21	BCnt<10>
22	BCnt<11>
23	JTAGTMS
24	JTAGTRST b
25	JTAGTCK
26	JTAGTDO
27	TestOut
28	JTAGTDI
29	BCntStr
30	Serial B Channel
31	GND
32	GND
33	GND
34	GND
35	VCC 5
36	VCC 5
37	VCC D1
38	VCC D1
39	VEE
40	VEE
41	GND
42	GND
43	VDD
44	VDD
45	VDD D2
46	VDD D2
47	GND
48	GND
49	GND
50	GND

Appendix C

TTCrx Measurements

In this appendix measurement results are presented for the TTCrx.

MEASUREMENTS

The TTCrx IC was tested using the test board described in the previous appendix. A TTC transmitter crate, controlled by a VME module, was used to deliver the optical signal to the test board. During the tests random data and triggers were generated and continuously sent to the IC. The experimental set-up is schematically represented in Figure 16.

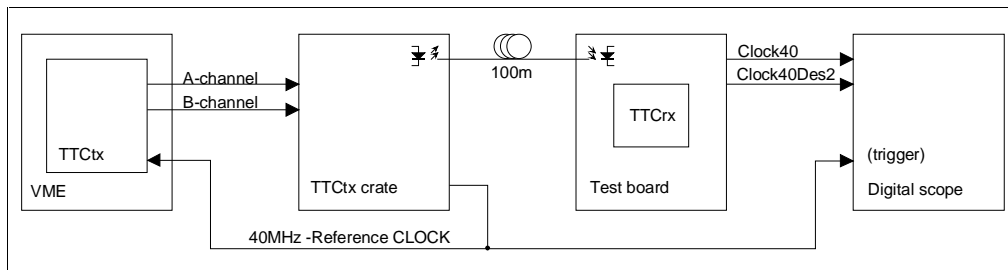


Figure 16 TTCrx test set-up

Jitter measurements

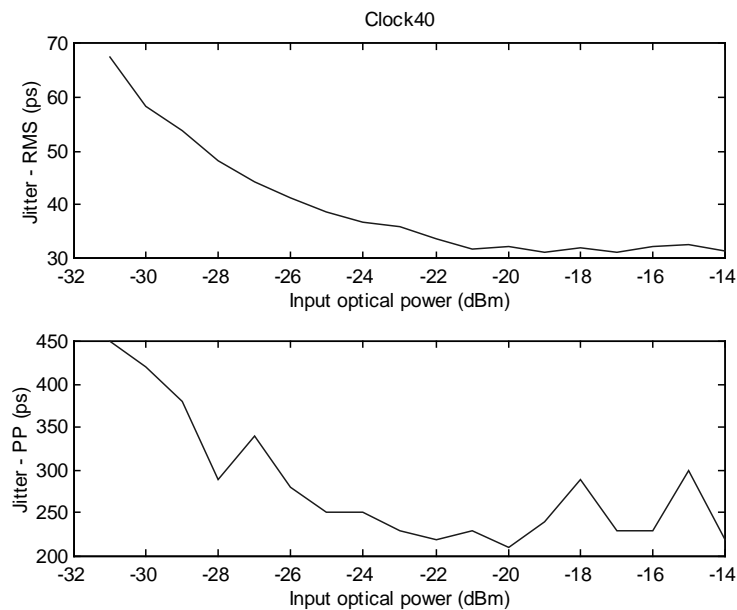


Figure 17 Non-deskewed clock jitter versus input optical power

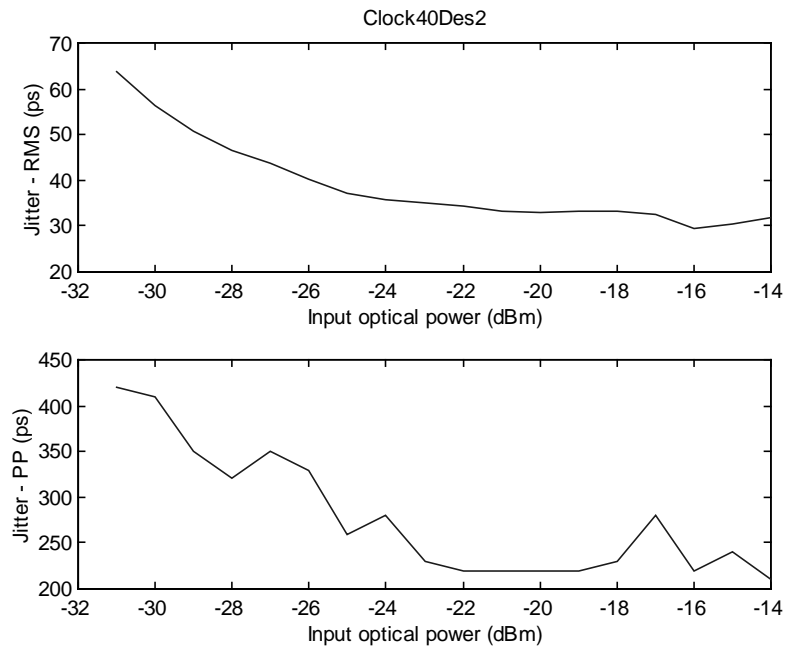


Figure 18 Deskewed clock jitter versus input optical power (maximum deskew)

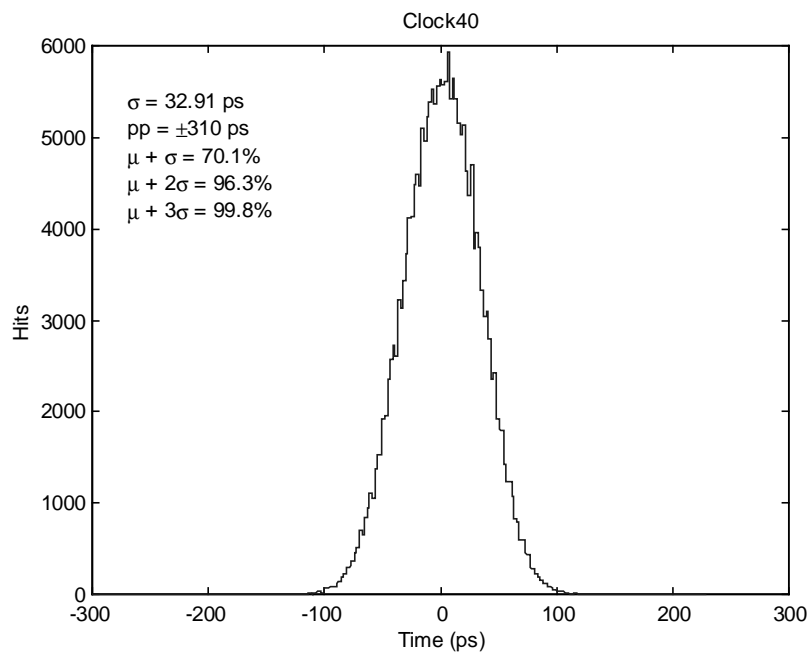


Figure 19 Non-deskewed clock jitter histogram (Pin = -20 dBm)

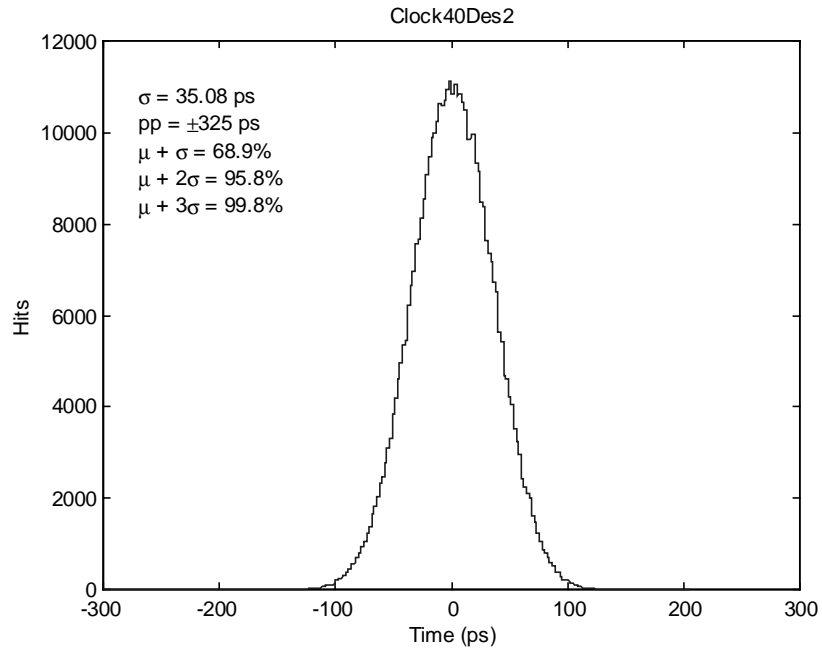


Figure 20 Deskewed clock jitter histogram (Pin = -20 dBm, maximum deskew)

Clock phase/optical power relationship

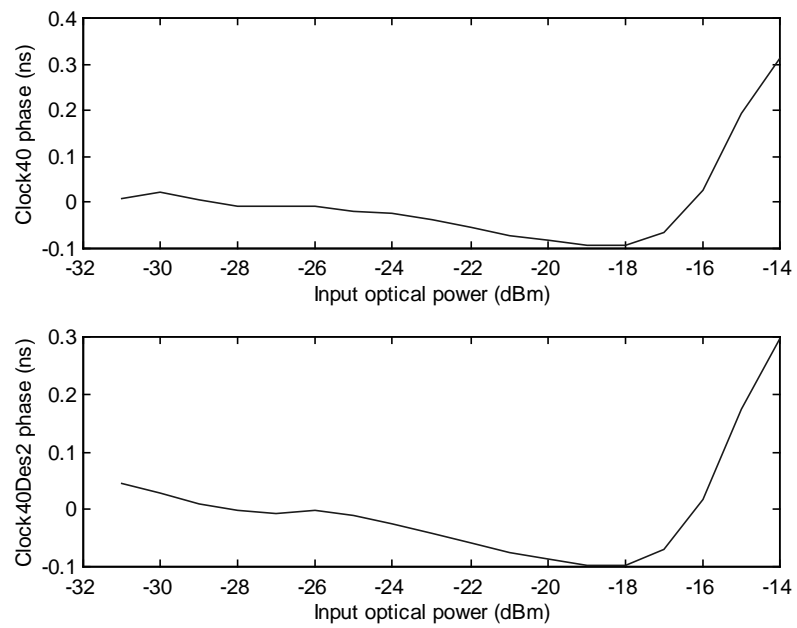


Figure 21 Clock phase versus input optical power

Deskew function linearity

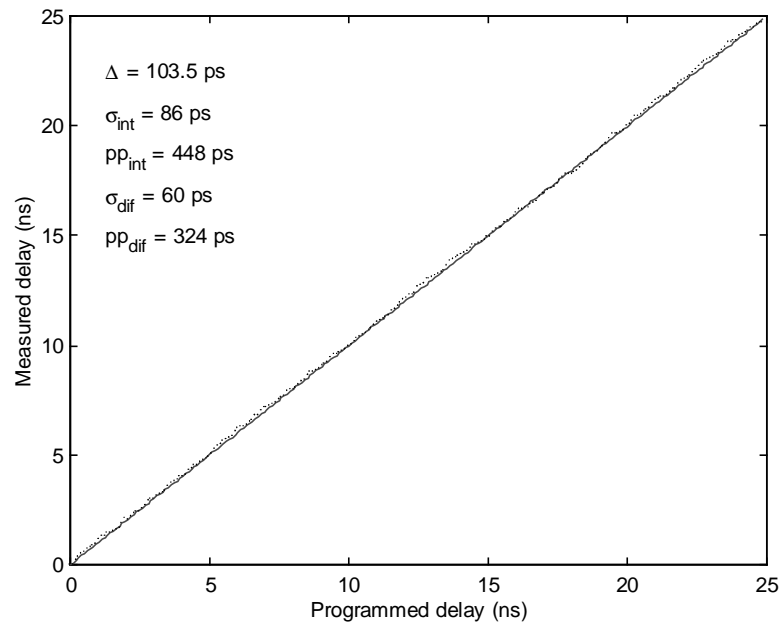


Figure 22 Measured delay as function of the programmed delay

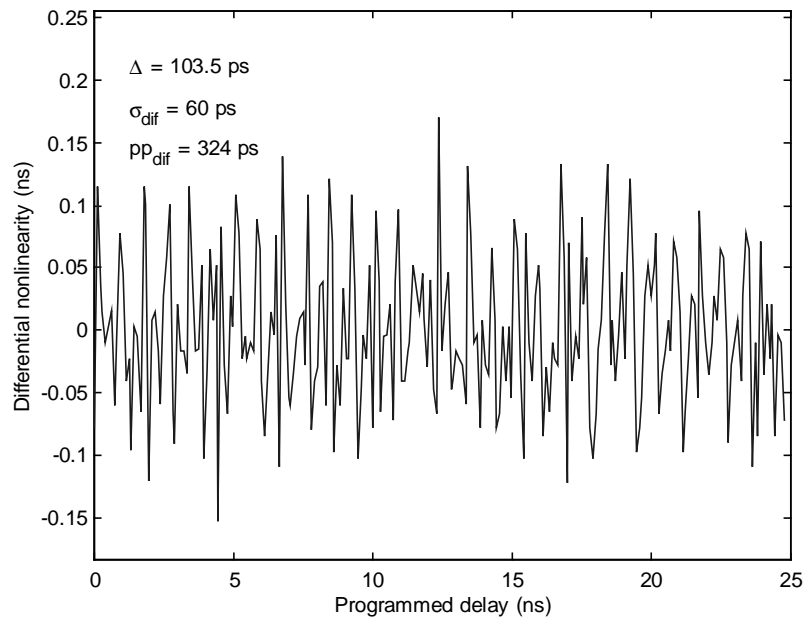


Figure 23 Measured differential nonlinearity

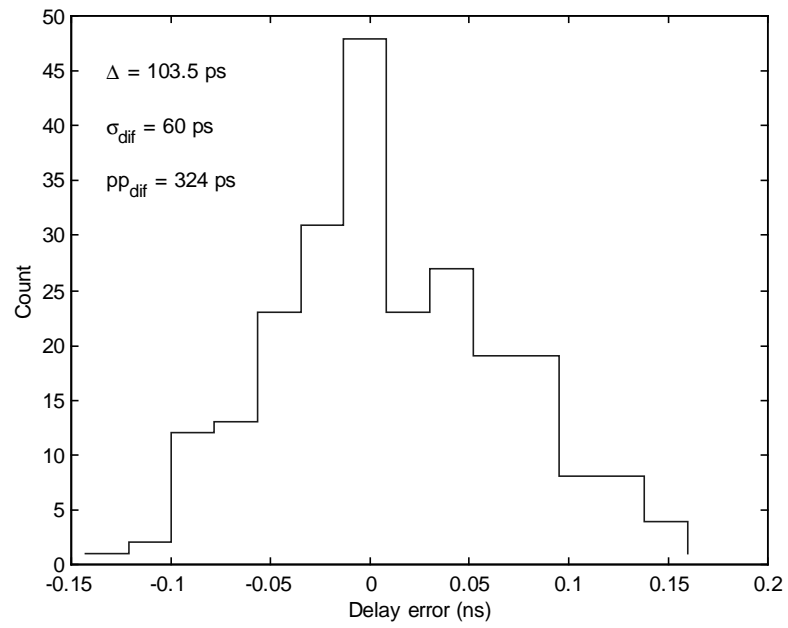


Figure 24 Measured differential nonlinearity histogram

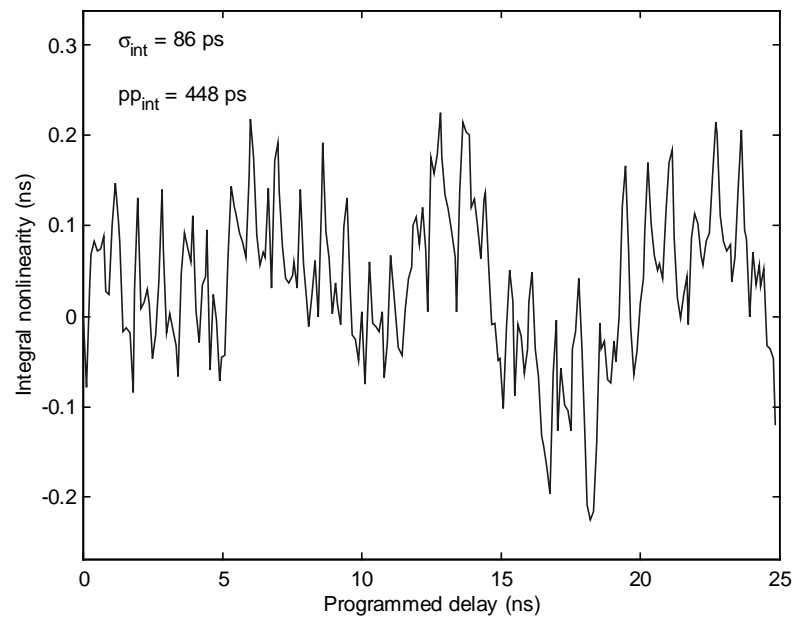


Figure 25 Measured integral nonlinearity

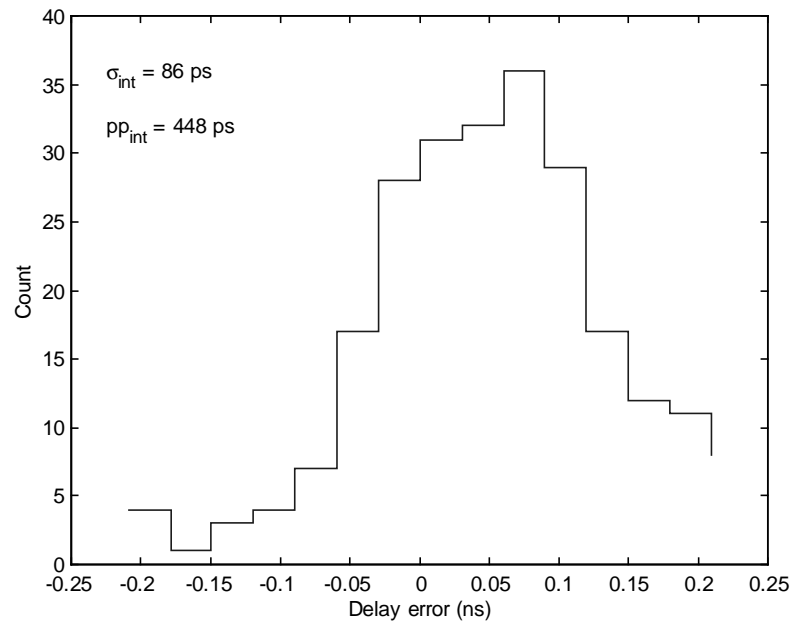


Figure 26 Measured integral nonlinearity histogram

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- [2] B. G. Taylor, "TTC Distribution," Proceedings of the First Workshop on Electronics for LHC Experiments, Lisbon, 11-15 September 1995, (CERN/LHCC/95-56), pp. 180-184.
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