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TTCrx modifications

A) Extended Supply voltage range

Absolute min/max values for VDD : 3.3-5.0 V ± 10 %

B) Radiation hardness

The chip will be fabricated in the radiation-hard DMILL technology.

C) Revised Input amplifier

The input amplifier which receives the signal from the PIN-photodiode + Preamp now has a gain high enough that an additional post-amplifier, as included on the present test board (See [1], Appendix B), can be removed. The biasing inputs **Res** and **Res_b** (See Fig. 5 and Ch. 7 in [1]) for the amplifier were removed.

D) Hard-wired ID

The hard-wired ID option was included in order to be able to set the 14 bit chip ID without the need of an initialization PROM (which would also have to be radiation-hard). While the **Reset_b** line is low, the chip disables the output drivers on the **SubAddr<7:0>** and **Dout<7:0>** buses, allowing hard-wired resistors to drive the pins to either VDD or GND, thus coding either a logical 1 or 0. The 14 bit chip ID is then loaded from the **SubAddr<5:0>**, **Dout<7:0>** buses at the rising edge of **Reset_b**. If the PROM is used for initialization, however, then the ID value stored in the PROM is used.

The minimum reset pulse length is determined by the RC-time constant on the **SubAddr<7:0>**, **Dout<7:0>** pins, i.e. if the resistor values are high (e.g. 200 kW) then the reset pulse must be long enough to allow the voltages on the pins to reach a state corresponding to a logical 0 or 1. The reset pulse must also be longer than the time it takes the supply voltage to become stable.

E) Initialization via the PROM

The PROM is no longer necessary for the operation of the circuit (i.e. all internal parameters are set to default values at reset). As an option, it can however still be used to configure the chip and to set the ID. The **enProm** Pin determines if the Prom is used for initializing the TTCrx chip. If high, the chip assumes the presence of a Prom and reads in its contents after a reset. The **PromReset** (output-)pin does not exist any more. Hence the reset signal for the PROM must now be generated on the PCB.

F) I2C Bus Interface

An I2C Bus [2] interface has been added. The I2C clock and data signals **SCL** and **SDA** are at the locations of the former pins **TestIn** and **TestOut**. All **Control**-, **ID**-, and **Configuration** registers (see attached register definition) can be read and written via the I2C interface. The two **error counter** registers, the **bunch-** and the **event counter** can be *read* and *reset* via the I2C interface.

1. Every I2C transmission is performed using only two registers: the **pointer register,** accessed when Bit 0 of I2C address = 0, contains the number of the register to be accessed, and the **data register**, accessed with Bit 0 of I2C address = 1, contains the data of the addressed register.

2. The upper 6 bits of the 14 bit chip-ID serve as the upper 6 bits of the (7 bit) I2C base address. The lowest bit of the

I2C address chooses the register (pointer or data register, as described above).

3. Although the 14-bit Chip ID can be changed via the I2C interface, the 6 bit I2C device address is specified only at the time of initialization and cannot be changed afterwards.

G) Command structure

In order to free the address space of the broadcast commands, the ERDUMP, CRDUMP and INIT **Broadcast Commands** have been replaced by **Individually Addressed Commands** (writing to SubAdr=4 for ERDUMP, SubAdr=5 for CRDUMP, SubAdr=6 for INIT). Thus, there are now 64 broadcast commands available to the user.

H) Option to use Clock40Des2 to transmit user-broadcast commands

In order to fine-adjust the timing of the user and system broadcast commands independently from the trigger and bunch-counter reset signals, it is possible to synchronize the broadcast strobe **BrcstStrb2** either to **Clock40Des2** or **Clock40Des1**. (In the old version **BrcstStrb2** is always synchronized with **Clock40Des1**.) A mode bit in the configuration register now determines which clock is used for **BrcstStrb2**.

I) Option to switch off command decoding

A bit in the configuration register allows the command decoding to be switched off. The data in the B channel are therefore not interpreted. The B channel can thus be used as a simple serial channel. In order to distinguish channel A from channel B it must however be guaranteed that the pattern in channel B regularly contains a series of 12 or more ones. (See Fig. 3 in [1])

J) List of changed Pins

IC B. Pad #	former assignment	present assignment
4	PromReset (output)	enProm (input)
11	In_b (Input from PIN)	VDD!
12	In (Input from PIN)	In_b
13	Res_b (Biasing input)	In
14	Res (Biasing input)	GND!
20	TestIn	SCL
21	TestOut	SDA (open drain)
22	VcoOn (not packaged)	- (removed)

References

[1] J. Christiansen, A. Marchioro and P.Moreira, "TTCrx Reference Manual", Version 2.2, July 1997, http://pcvlsi5.cern.ch:80/MicDig/ttc/MANUAL22.PDF

[2] http://www-us2.semiconductors.philips.com/acrobat/various/I2C_BUS_SPECIFICATION_1995.PDF