

TTCsr PMC Module

Content

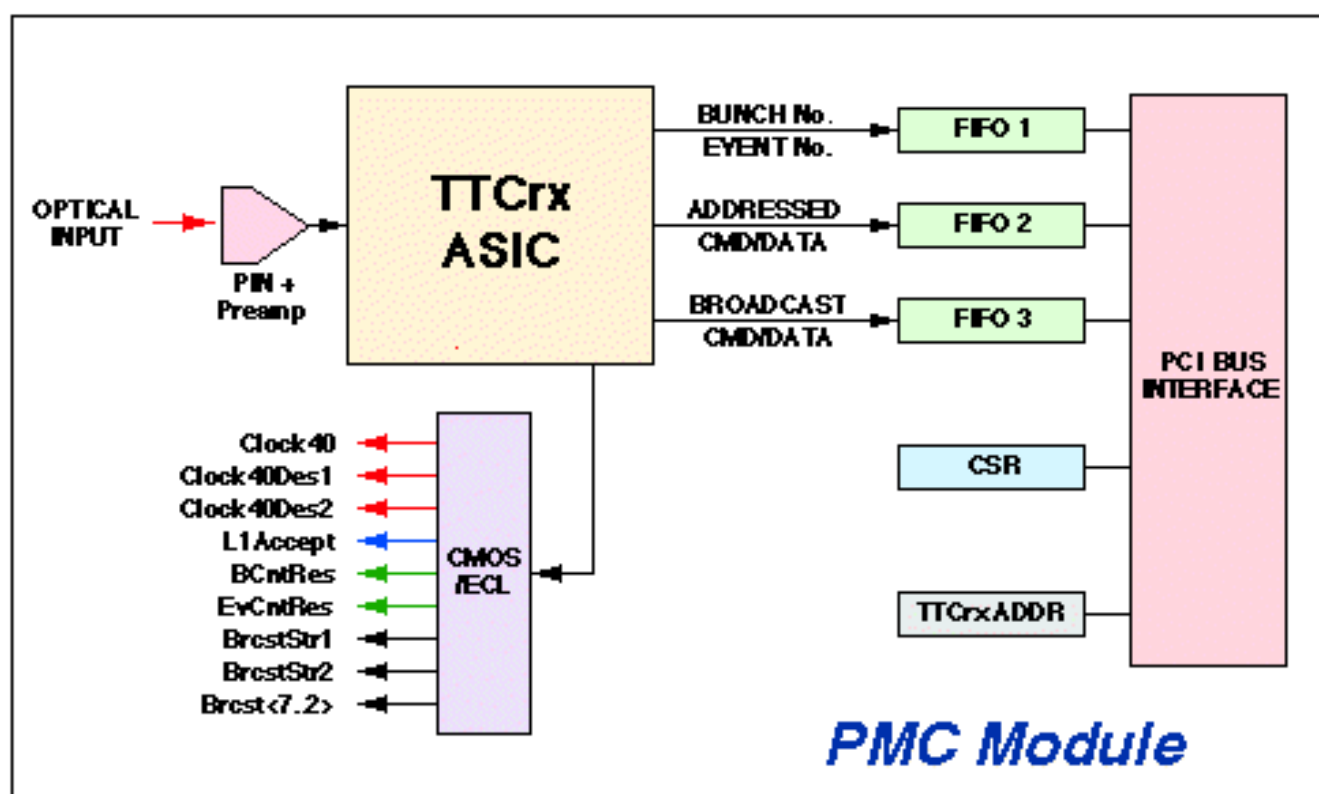
- TTCsr specifications
- Data Distribution into the FIFOs
- PCI bus properties
- PCI in VME
- Architecture of the TTCsr PMC module
- FIFOs Operation
- ORCA FPGAs
- VHDL designing
- Design Flow
- PCI Logic Analyser results

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TTC Workshop, October 30th

TTCsr specifications

- PMC module (Mezzanine Card for PCI in VME).
- 3 FIFOs: Bunch and event counters, individually addressed commands and broadcast commands/data.
- FIFOs data available from PCI.
- Main timing and control signals available on the front panel as ECL differential signals.
- Optical Input on the front panel.



Data Distribution into the FIFOs

FIFO1

- Event and Bunch Counters

Option 1	Event Counter Low (12 bits)
	Event Counter High (12 bits)
	Bunch Counter Identifier (12 bits)
Option 2	Bunch Counter Identifier (12 bits)
Option 3	Event Counter Low (12 bits)
	Event Counter High (12 bits)
Option 4	Event Counter Low (12 bits)

FIFO2

- Subaddress/Data cycles

D<0..7>	D<8..15>
Subaddress	Data

FIFO3

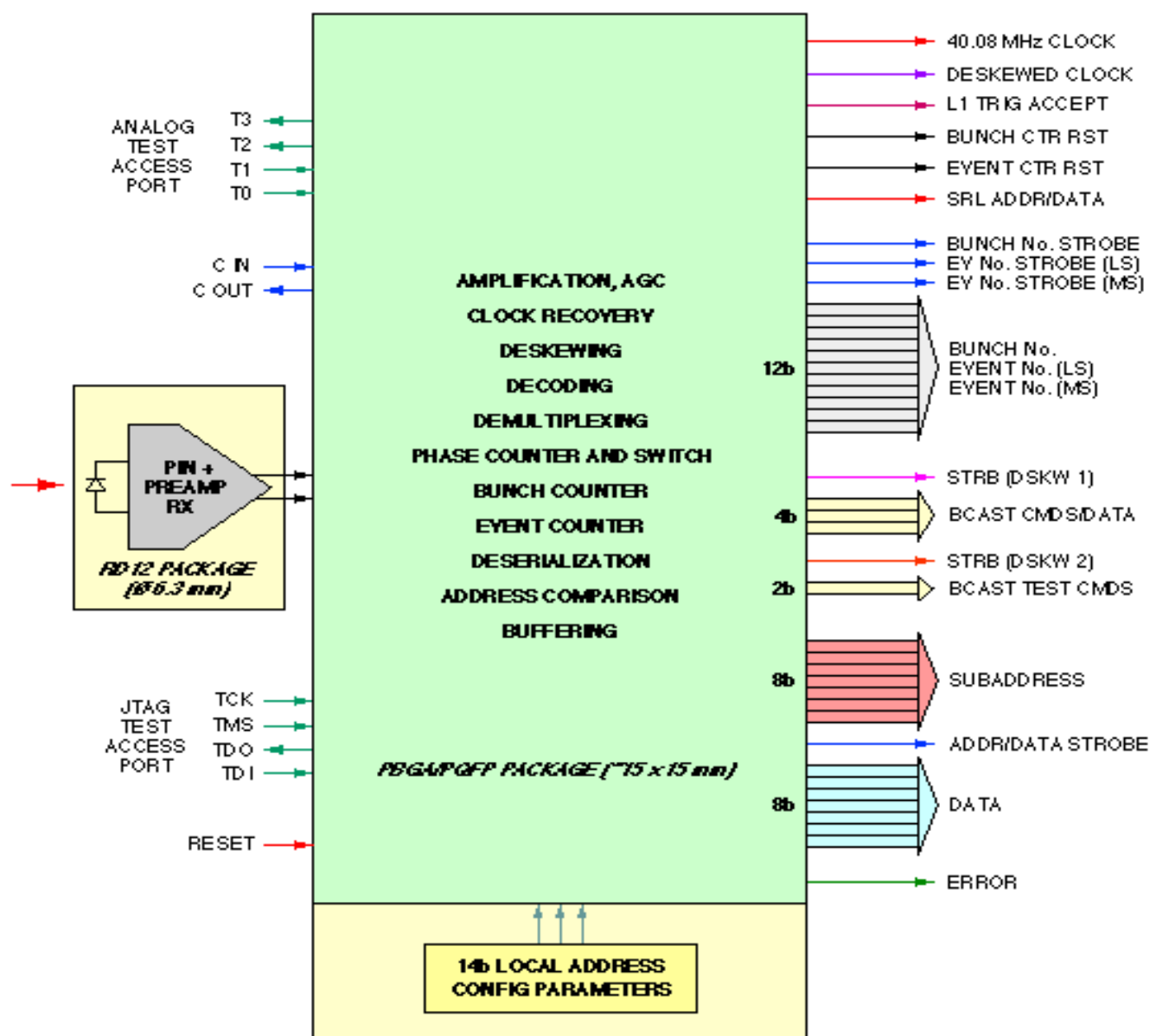
- Broadcast Commands and data issued in response

D<0..1>	D<2..5>
User Commands	System Commands

DQ	Data bus content
0001	Single Bit Error Counter High
0010	Single Bit Error Counter Low
0011	Double Bit Error Counter High
0100	Double Bit Error Counter Low

DQ	Data bus content
0101	Fine Delay register 1
0110	Fine Delay register 2
0111	Coarse Delay register
1000	Control register
1001	Configuration register bit <7:0>
1010	Configuration register bit <15:8>
1011	Configuration register bit <23:16>
1100	Configuration register bit <31:24>

Timing Receiver (TTCrx) ASIC

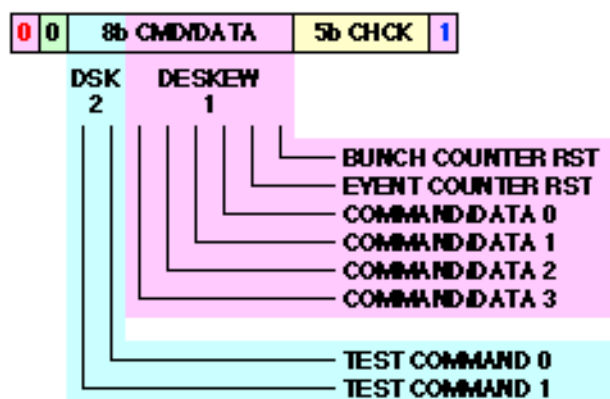


B Channel Data Format

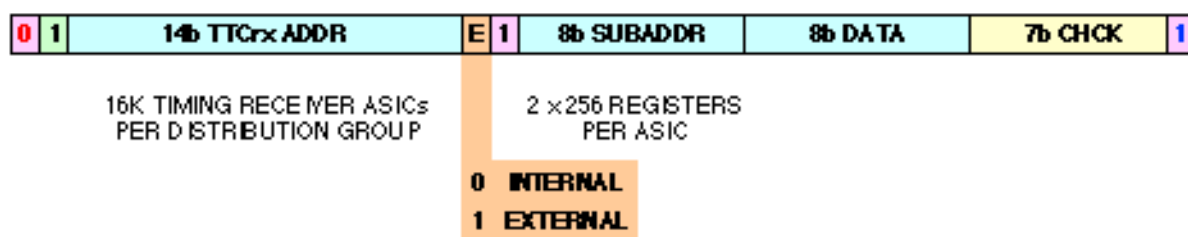
General frame



Broadcast command/data

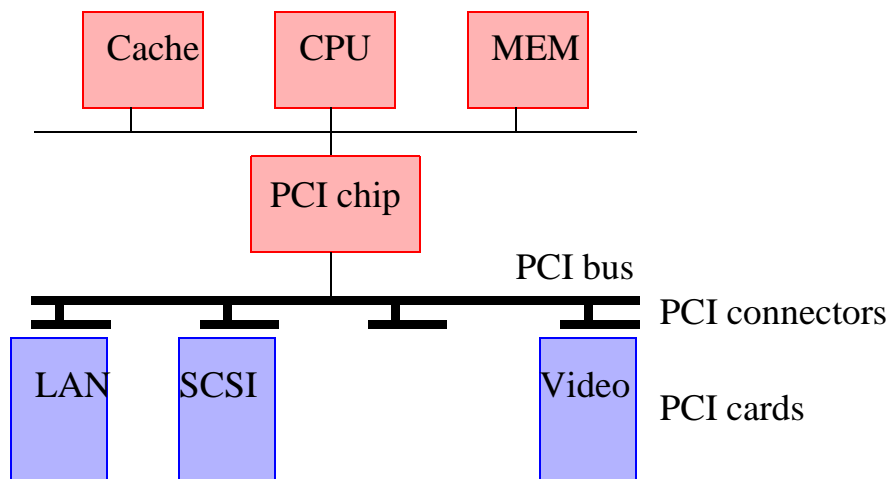


Addressed command/data



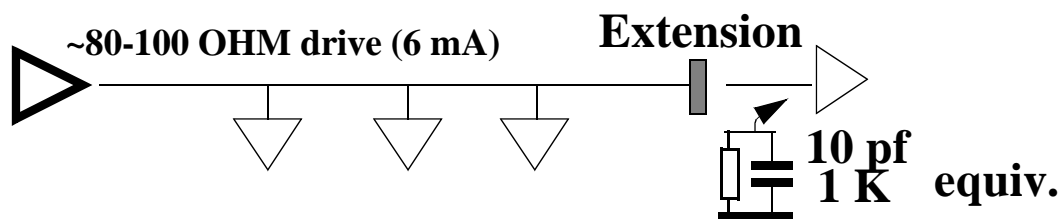
PCI bus properties

Typical PCI architecture

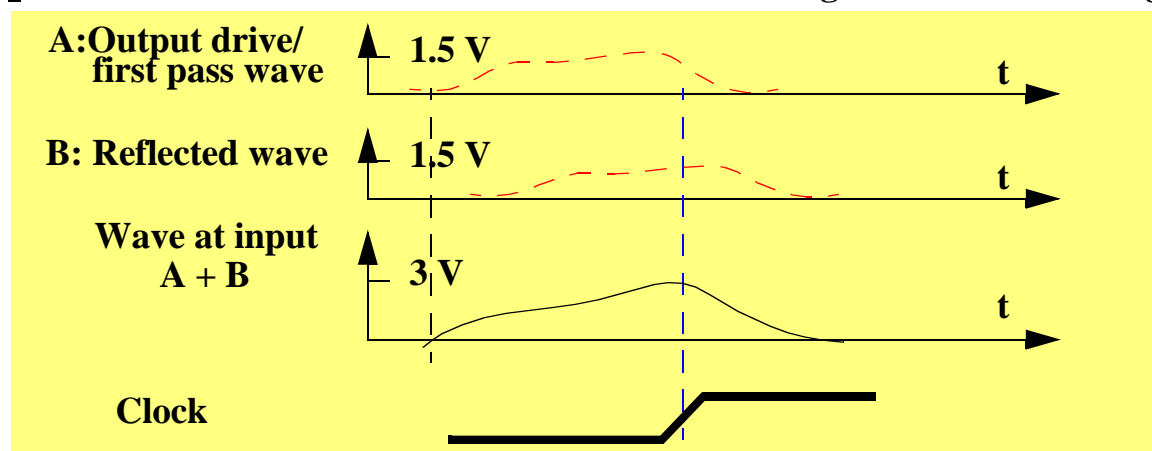


Note: PCI devices can communicate across PCI
A single PCI bus can handle up to 5 slots only:

Load/Length limitation: unterminated reflected wave technology



Data is clocked when reflected wave is received: higher threshold Voltage

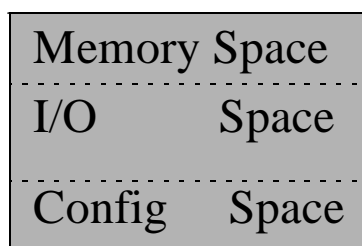
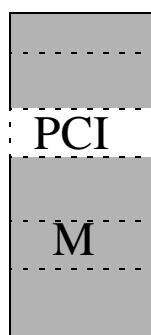


Careful with PCI load : overloaded PCI buses don't work

PCI address space

CPU address

PCI address

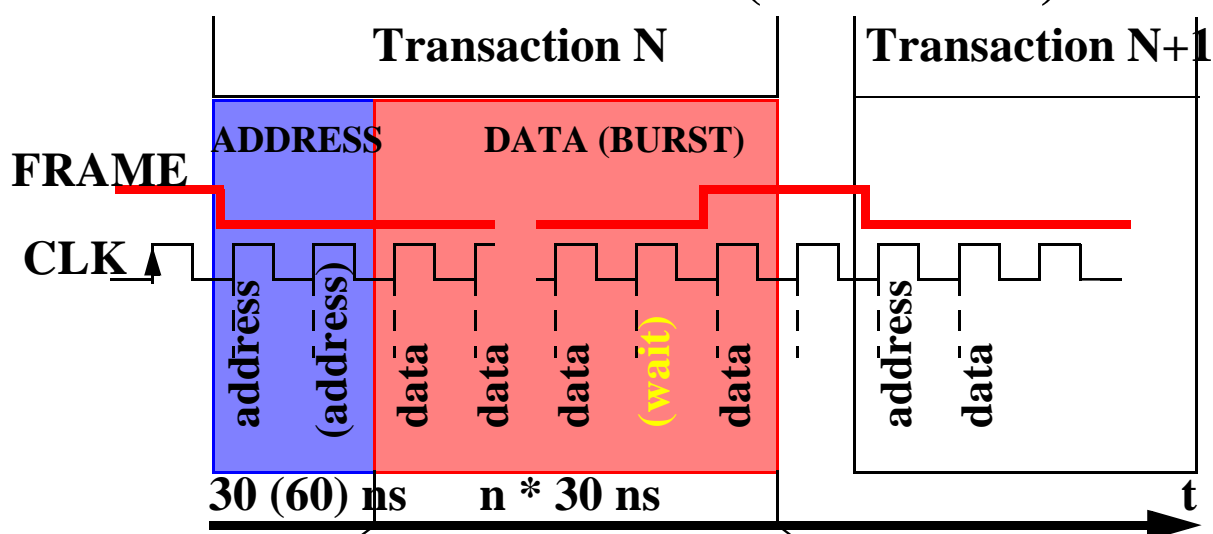


read=write

Functions, bits

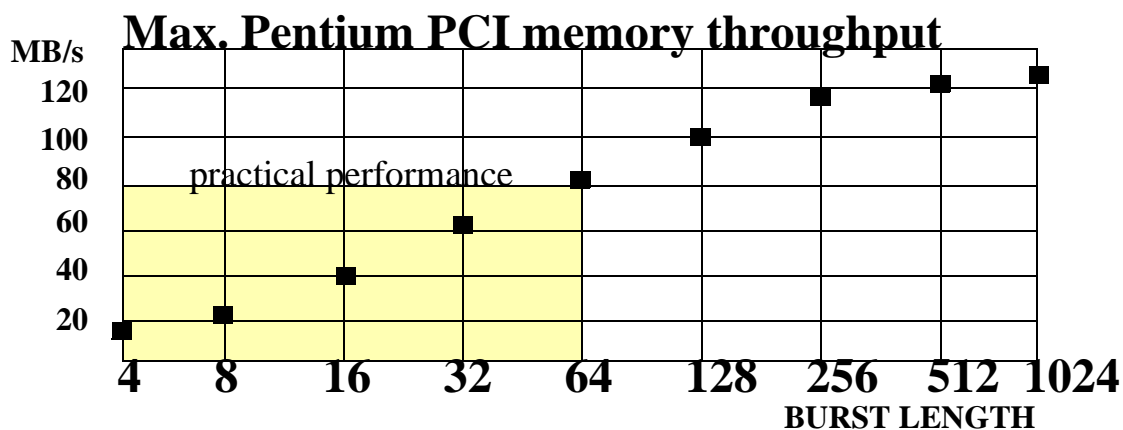
Plug&Play
configuration
registers

PCI bus transactions (r/w bursts)



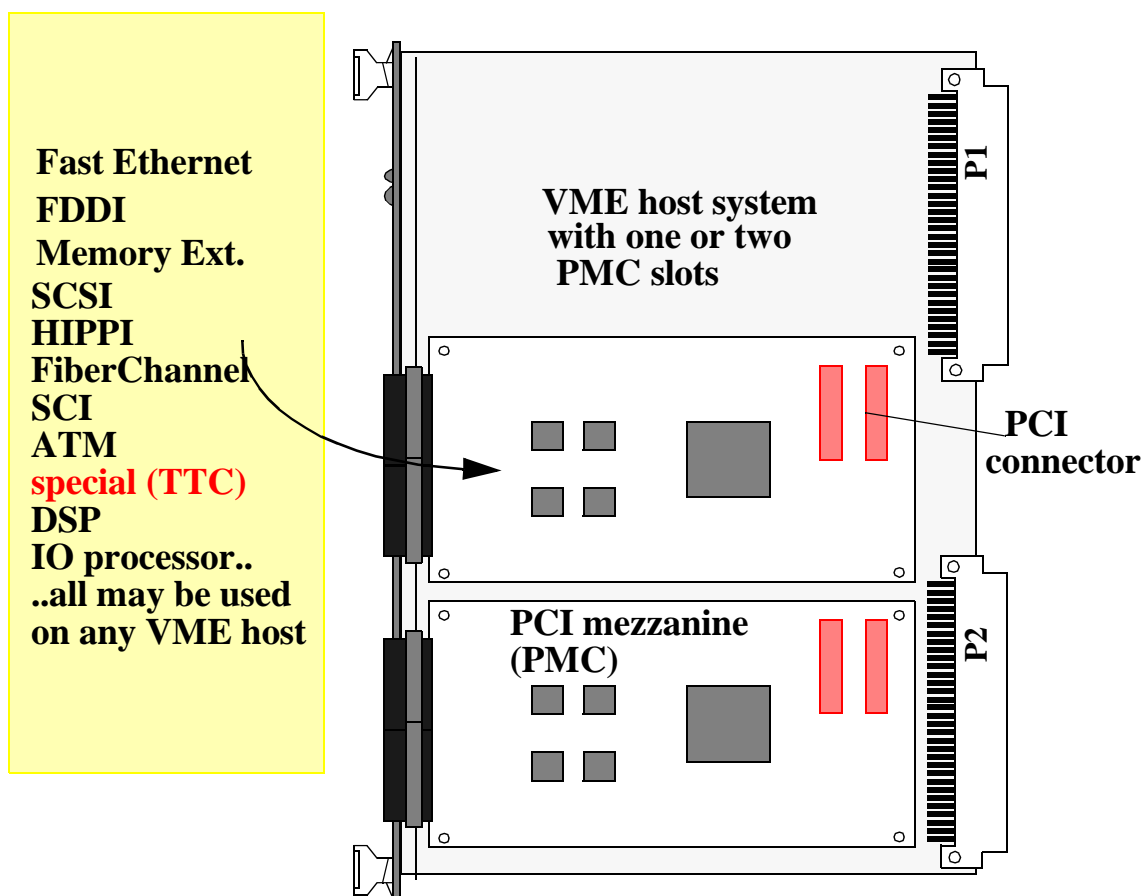
peak bandwidth:
4 byte @ 33 MHz => 132 Mbyte/s

PCI performance



PCI in VME

IEEE P1386.1 mezzanines (PMC's)



For a full list of VITA compliant mezzanines see the Mezzanine Module Product directory on <http://www.vita.com/mezzprod/mezzdirindex.html>

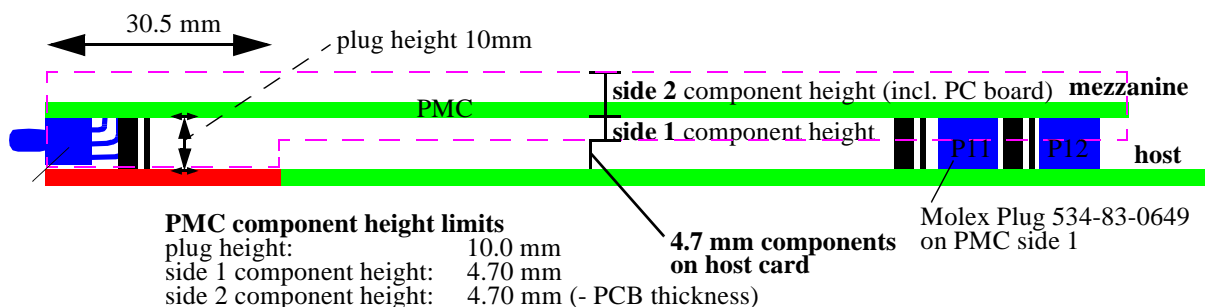
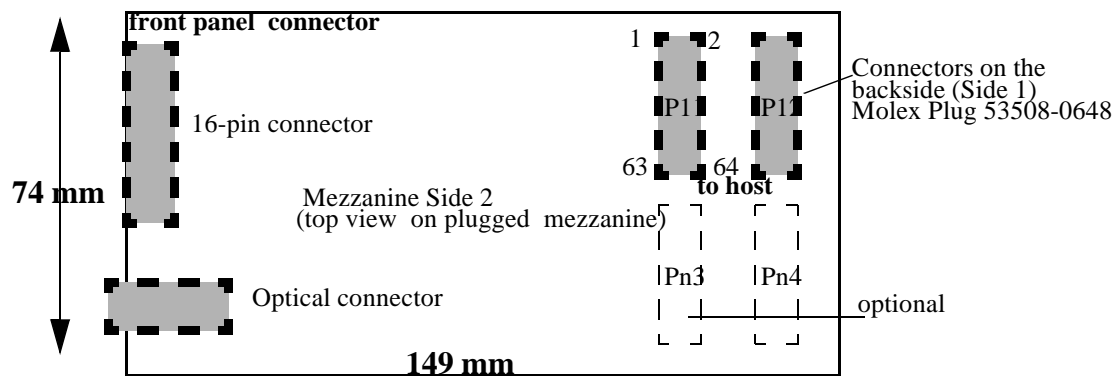
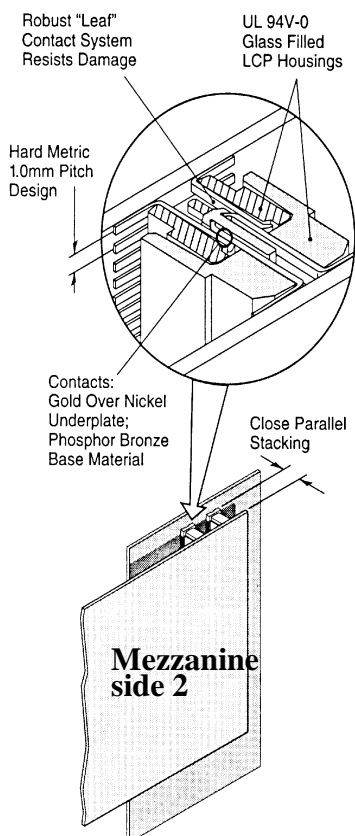
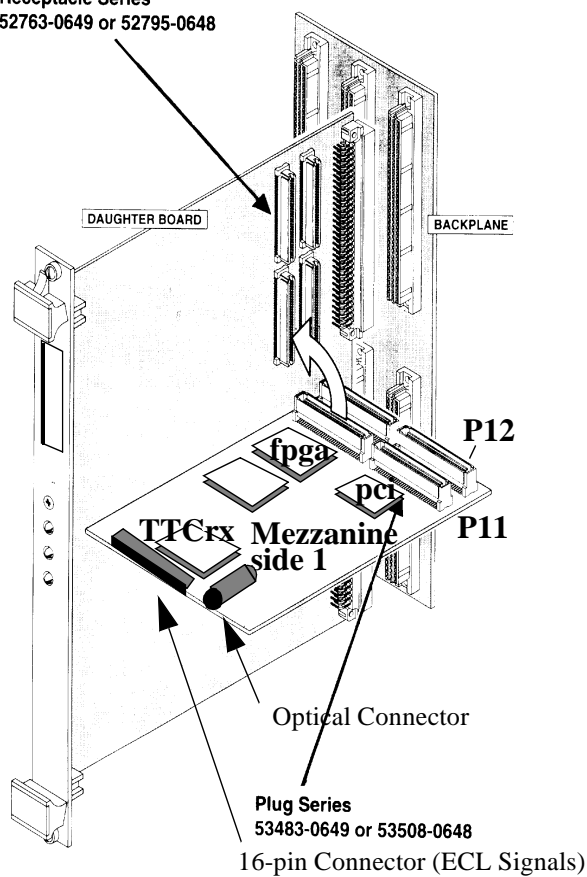
Some VME CPU's :

PowerPC:

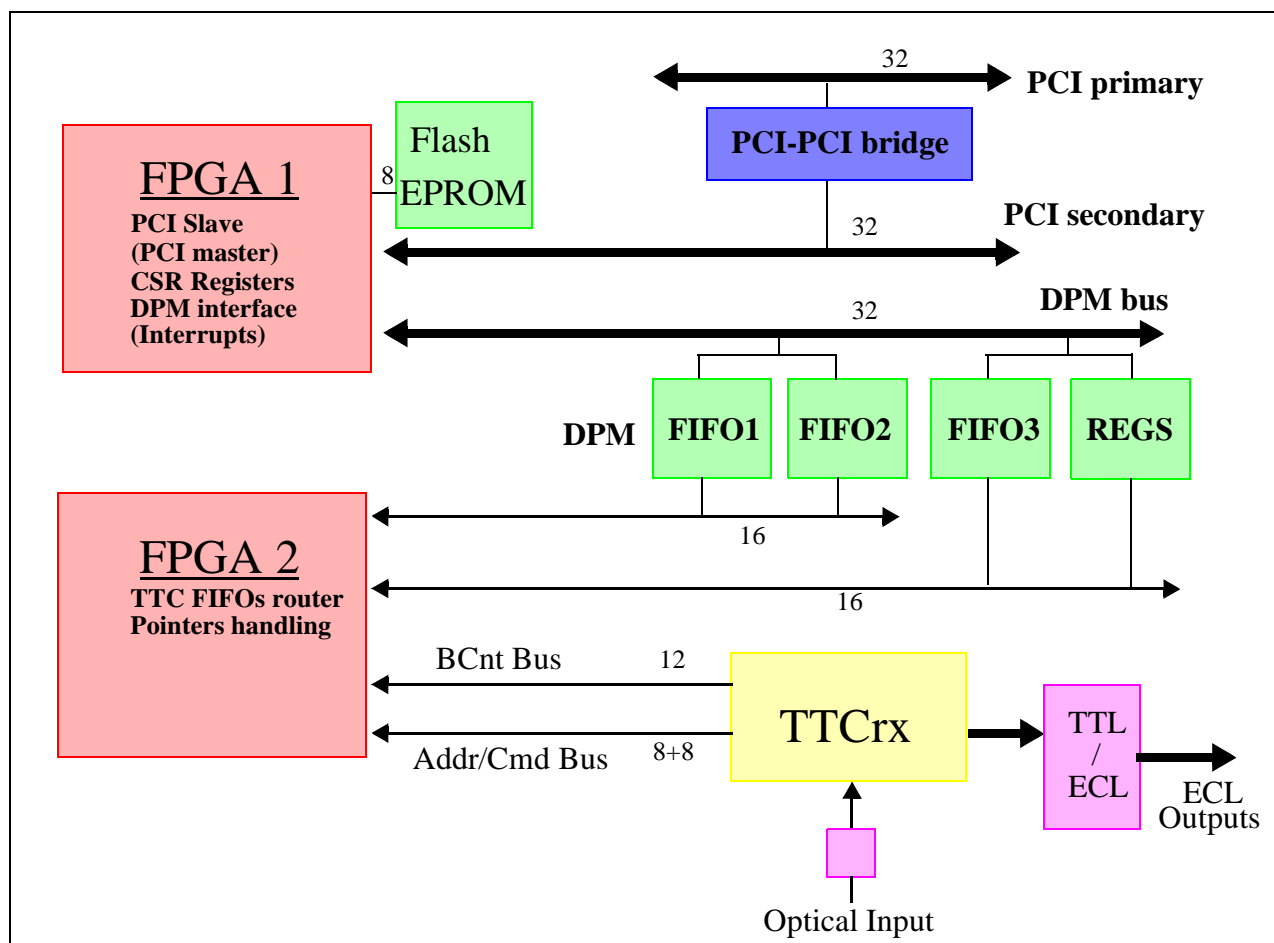
- CES RTPC 8067: (1 PMC), CES RIO 8061: (2 PMC)
- Radstone (+ CETIA) PPC604/603 (2 PMC) + (2 PMC)
- Motorola MVME1603-1 (1 PMC), MVME-1300 (2 PMC)
- Themis Power 3/64 (1 PMC)
- Force CPU-603RT (1 PMC) , Force IBC-603 (2 PMC)
(manufactured by CES)
- VI Computer Corporation Power 3eC (1 PMC)

PMC mezzanines details for VME

Receptacle Series
52763-0649 or 52795-0648



Architecture of the TTCsr PMC module

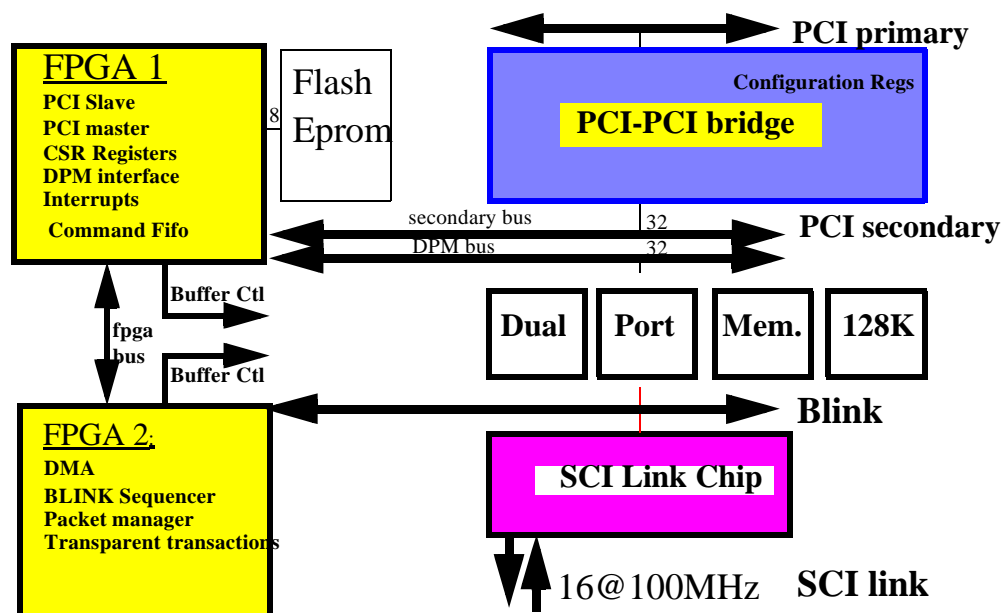


- BGA TTCrx package.
- FIFOs implemented on DPM allow PCI burst transfers.
- DPM communication buffers between FPGAs for keeping the number of data received.
- PCI FPGA already designed and tested.
- Possibility of a future use of PCI Master.

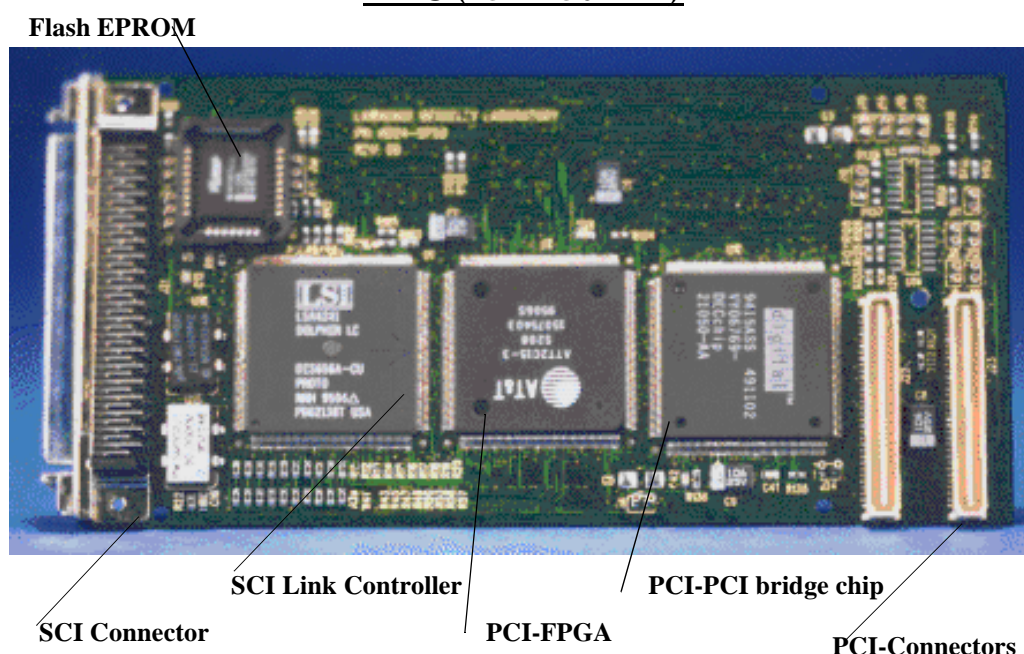
PCI-SCI adapters

- PMC and PCI card from RD24 / CERN : FPGA based design to allow implementation of DAQ specific functions (from VHDL). Drivers for Linux, LynxOS and Alpha OS/F

Architecture of the CERN PCI-SCI bridge



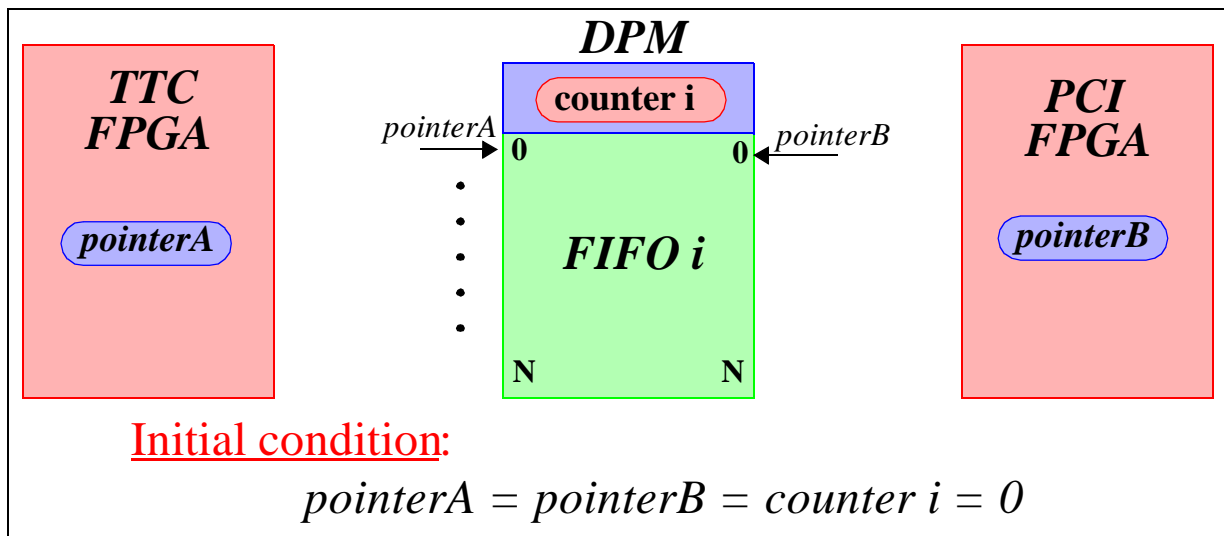
PMC (75 * 150 mm)



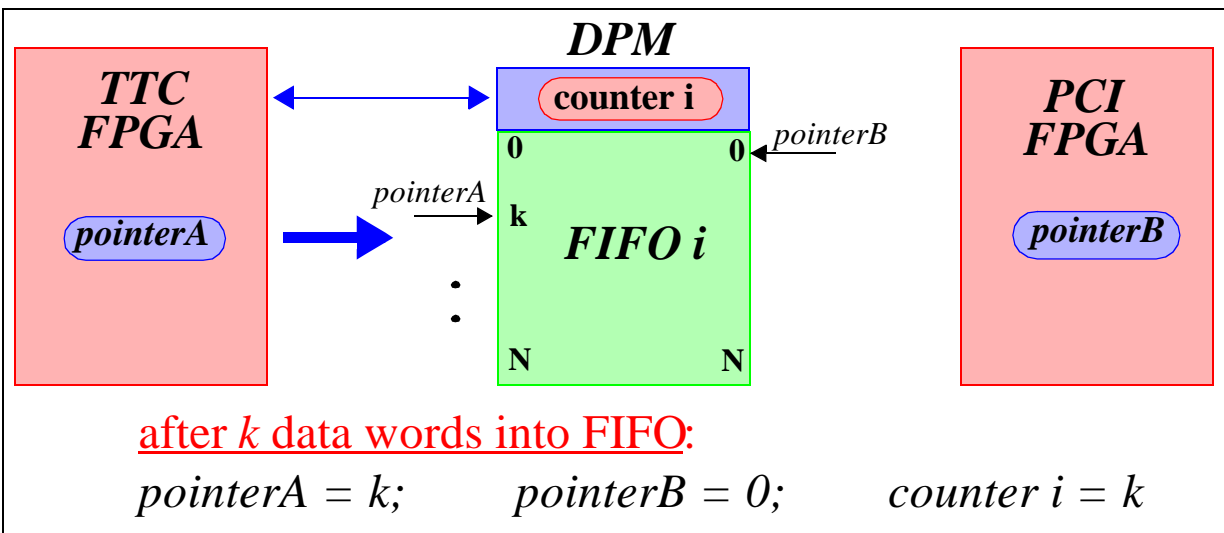
- WEB page: <http://sunshine.cern.ch:8080/PCI/PMCdesign>

FIFOs Operation with DPM

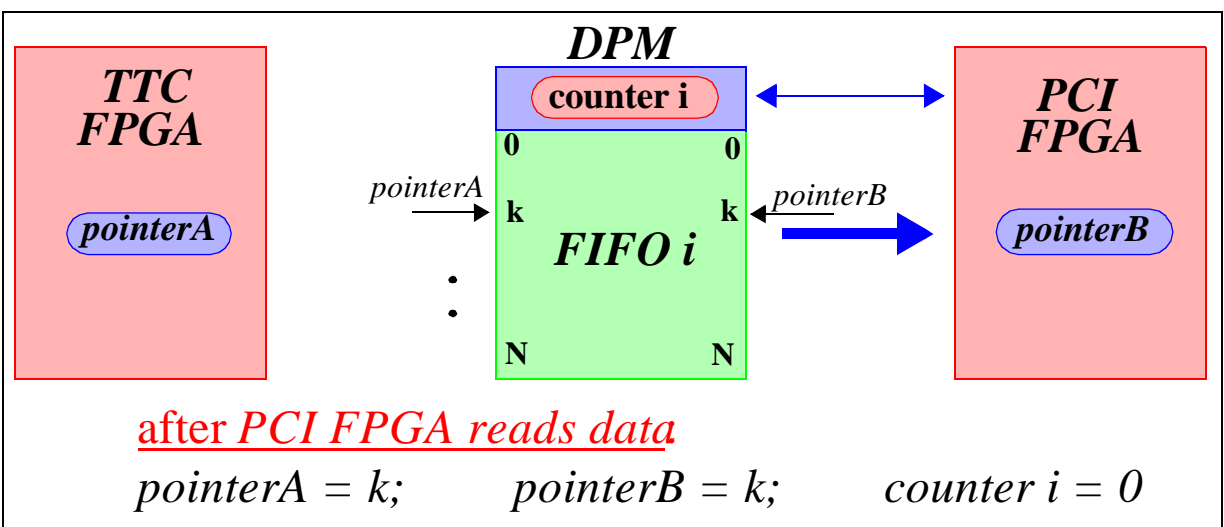
1)

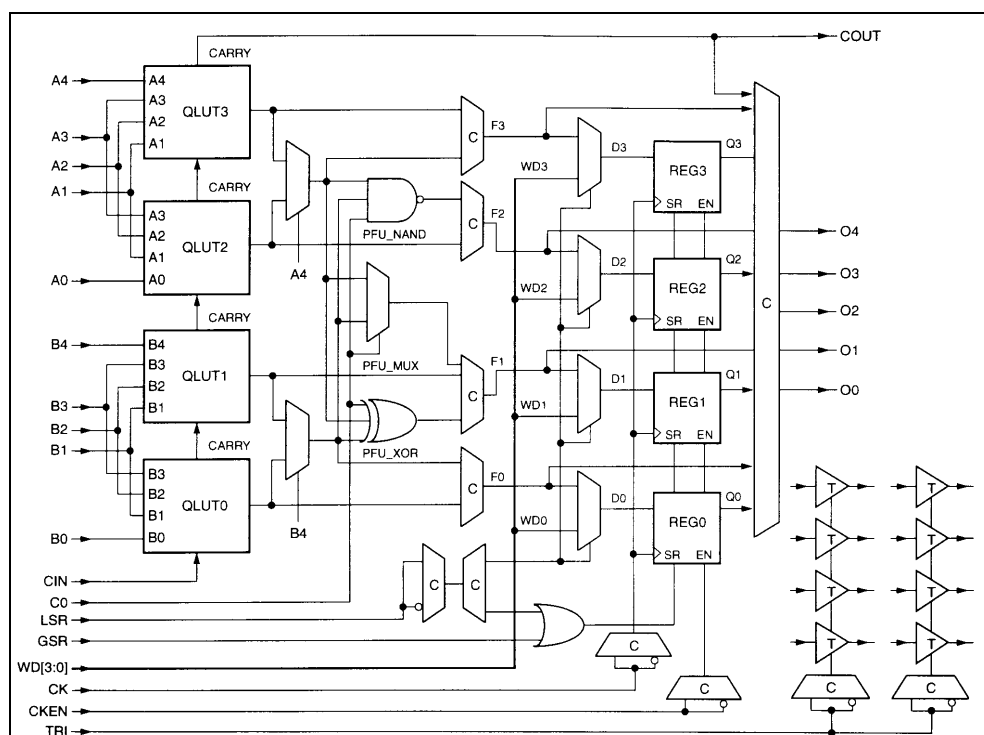


2)



3)



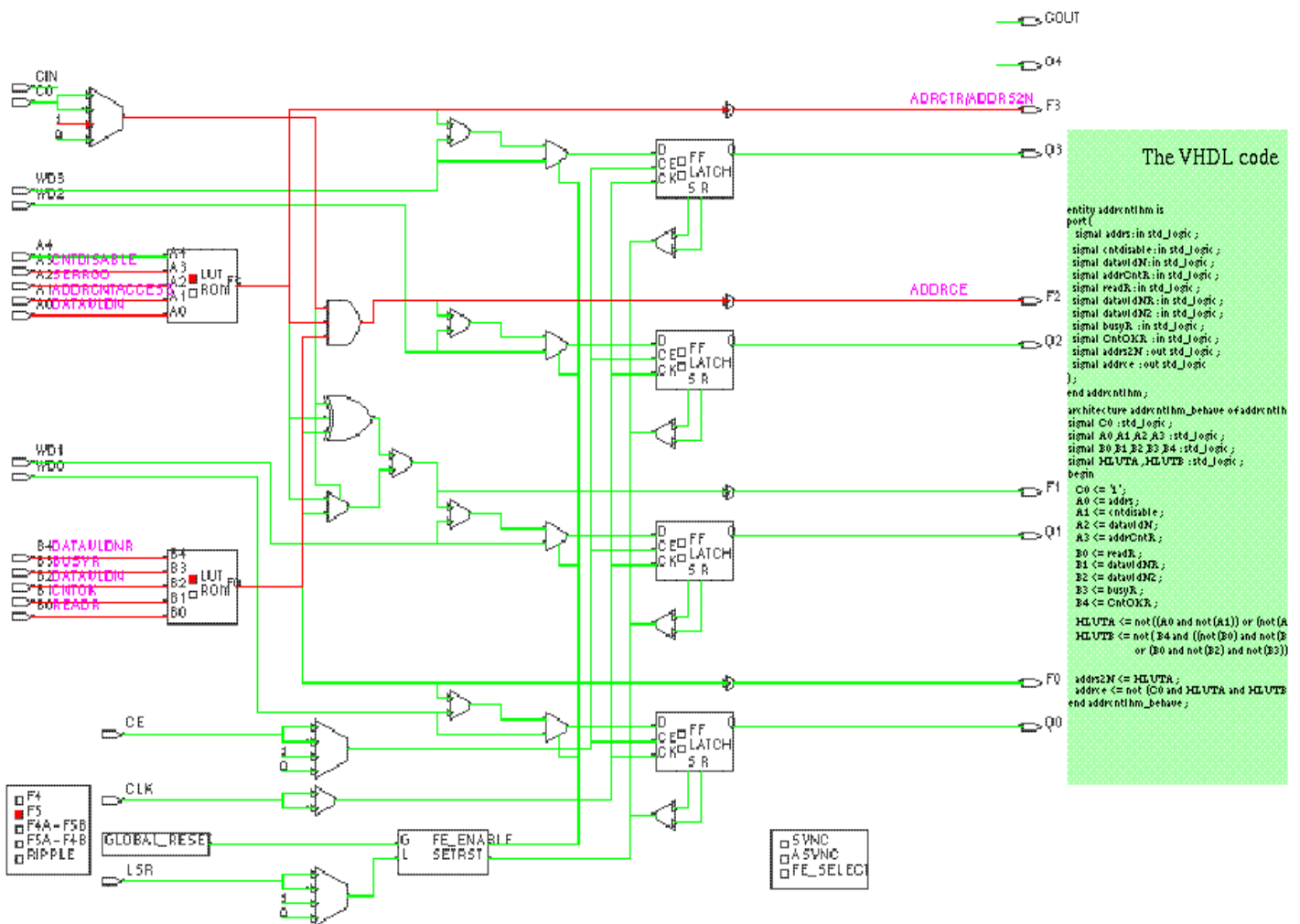


- Four 16-bit look-up tables and four latches per PFU.
- 19 external inputs and six outputs per PFU.
- Configurable to operate in different modes.

- 400/576 PLCs per FPGA.
- PLCs surrounded by Programmable Input/output Cells (PICs).
- Ability to combine PFUs to create larger structures.
- 0.35 μm CMOS technology.

	PT2	PT3	PT4	PT5	PT6	PT7	PT8	PT9	PT10	TMD	PT11	PT12	PT13	PT14	PT15	PT16	PT17	PT18	PT19	PT20		
P1	R1C1	R1C2	R1C3	R1C4	R1C5	R1C6	R1C7	R1C8	R1C9	R1C10	VQ	R1C11	R1C12	R1C13	R1C14	R1C15	R1C16	R1C17	R1C18	R1C19	R1C20	PR1
P2	R2C1	R2C2	R2C3		R2C5	R2C6	R2C7	R2C8	R2C9	R2C10		R2C11	R2C12	R2C13	R2C14	R2C15	R2C16	R2C17	R2C18	R2C19	R2C20	PR2
P3	R3C1	R3C2	R3C3	R3C4	R3C5	R3C6	R3C7	R3C8	R3C9	R3C10		R3C11	R3C12	R3C13	R3C14	R3C15	R3C16	R3C17	R3C18	R3C19	R3C20	PR3
P4	R4C1	R4C2	R4C3	R4C4	R4C5	R4C6	R4C7	R4C8	R4C9	R4C10		R4C11	R4C12	R4C13	R4C14	R4C15	R4C16	R4C17	R4C18	R4C19	R4C20	PR4
P5	R5C1	R5C2	R5C3	R5C4	R5C5	R5C6	R5C7	R5C8	R5C9	R5C10		R5C11	R5C12	R5C13	R5C14	R5C15	R5C16	R5C17	R5C18	R5C19	R5C20	PR5
P6	R6C1	R6C2	R6C3	R6C4	R6C5	R6C6	R6C7	R6C8	R6C9	R6C10		R6C11	R6C12	R6C13	R6C14	R6C15	R6C16	R6C17	R6C18	R6C19	R6C20	PR6
P7	R7C1	R7C2	R7C3	R7C4	R7C5	R7C6	R7C7	R7C8	R7C9	R7C10		R7C11	R7C12	R7C13	R7C14	R7C15	R7C16	R7C17	R7C18	R7C19	R7C20	PR7
P8	R8C1	R8C2	R8C3	R8C4	R8C5	R8C6	R8C7	R8C8	R8C9	R8C10		R8C11	R8C12	R8C13	R8C14	R8C15	R8C16	R8C17	R8C18	R8C19	R8C20	PR8
P9	R9C1	R9C2	R9C3	R9C4	R9C5	R9C6	R9C7	R9C8	R9C9	R9C10		R9C11	R9C12	R9C13	R9C14	R9C15	R9C16	R9C17	R9C18	R9C19	R9C20	PR9
P10	R10C1	R10C2	R10C3	R10C4	R10C5	R10C6	R10C7	R10C8	R10C9	R10C10		R10C11	R10C12	R10C13	R10C14	R10C15	R10C16	R10C17	R10C18	R10C19	R10C20	PR10
LMD	hIQ																					TMD
P11	R11C1	R11C2	R11C3	R11C4	R11C5	R11C6	R11C7	R11C8	R11C9	R11C10		R11C11	R11C12	R11C13	R11C14	R11C15	R11C16	R11C17	R11C18	R11C19	R11C20	PR11
P12	R12C1	R12C2	R12C3	R12C4	R12C5	R12C6	R12C7	R12C8	R12C9	R12C10		R12C11	R12C12	R12C13	R12C14	R12C15	R12C16	R12C17	R12C18	R12C19	R12C20	PR12
P13	R13C1	R13C2	R13C3	R13C4	R13C5	R13C6	R13C7	R13C8	R13C9	R13C10		R13C11	R13C12	R13C13	R13C14	R13C15	R13C16	R13C17	R13C18	R13C19	R13C20	PR13
P14	R14C1	R14C2	R14C3	R14C4	R14C5	R14C6	R14C7	R14C8	R14C9	R14C10		R14C11	R14C12	R14C13	R14C14	R14C15	R14C16	R14C17	R14C18	R14C19	R14C20	PR14
P15	R15C1	R15C2	R15C3	R15C4	R15C5	R15C6	R15C7	R15C8	R15C9	R15C10		R15C11	R15C12	R15C13	R15C14	R15C15	R15C16	R15C17	R15C18	R15C19	R15C20	PR15
P16	R16C1	R16C2	R16C3	R16C4	R16C5	R16C6	R16C7	R16C8	R16C9	R16C10		R16C11	R16C12	R16C13	R16C14	R16C15	R16C16	R16C17	R16C18	R16C19	R16C20	PR16
P17	R17C1	R17C2	R17C3	R17C4	R17C5	R17C6	R17C7	R17C8	R17C9	R17C10		R17C11	R17C12	R17C13	R17C14	R17C15	R17C16	R17C17	R17C18	R17C19	R17C20	PR17
P18	R18C1	R18C2	R18C3	R18C4	R18C5	R18C6	R18C7	R18C8	R18C9	R18C10		R18C11	R18C12	R18C13	R18C14	R18C15	R18C16	R18C17	R18C18	R18C19	R18C20	PR18
P19	R19C1	R19C2	R19C3	R19C4	R19C5	R19C6	R19C7	R19C8	R19C9	R19C10		R19C11	R19C12	R19C13	R19C14	R19C15	R19C16	R19C17	R19C18	R19C19	R19C20	PR19
P20	R20C1	R20C2	R20C3	R20C4	R20C5	R20C6	R20C7	R20C8	R20C9	R20C10		R20C11	R20C12	R20C13	R20C14	R20C15	R20C16	R20C17	R20C18	R20C19	R20C20	PR20
BMID	PB1	PB2	PB3	PB4	PB5	PB6	PB7	PB8	PB9	PB10	BMID	PB11	PB12	PB13	PB14	PB15	PB16	PB17	PB18	PB19	PB20	

VHDL designing

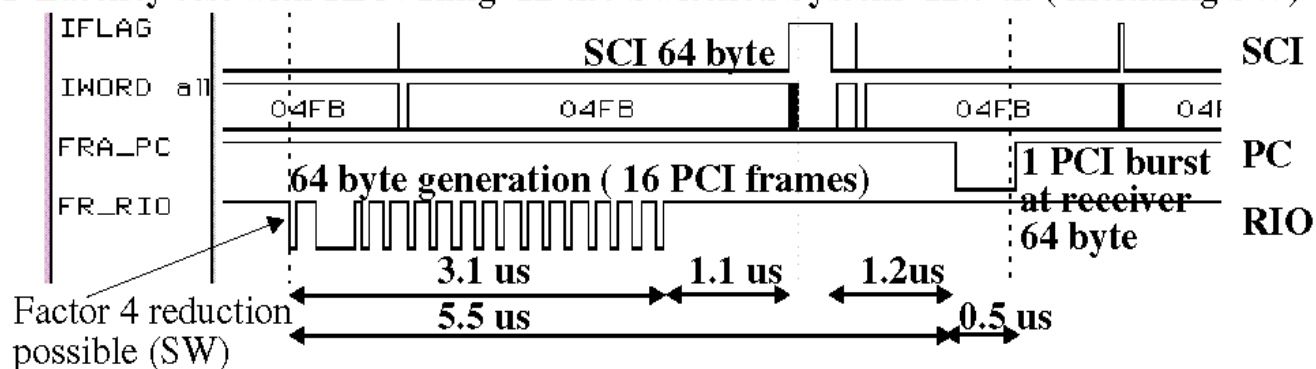


- Logic described in High Level Description Language (VHDL), easier to modify and export.
- Synthesized by means of NeoCad Foundry tools.

[illegible]

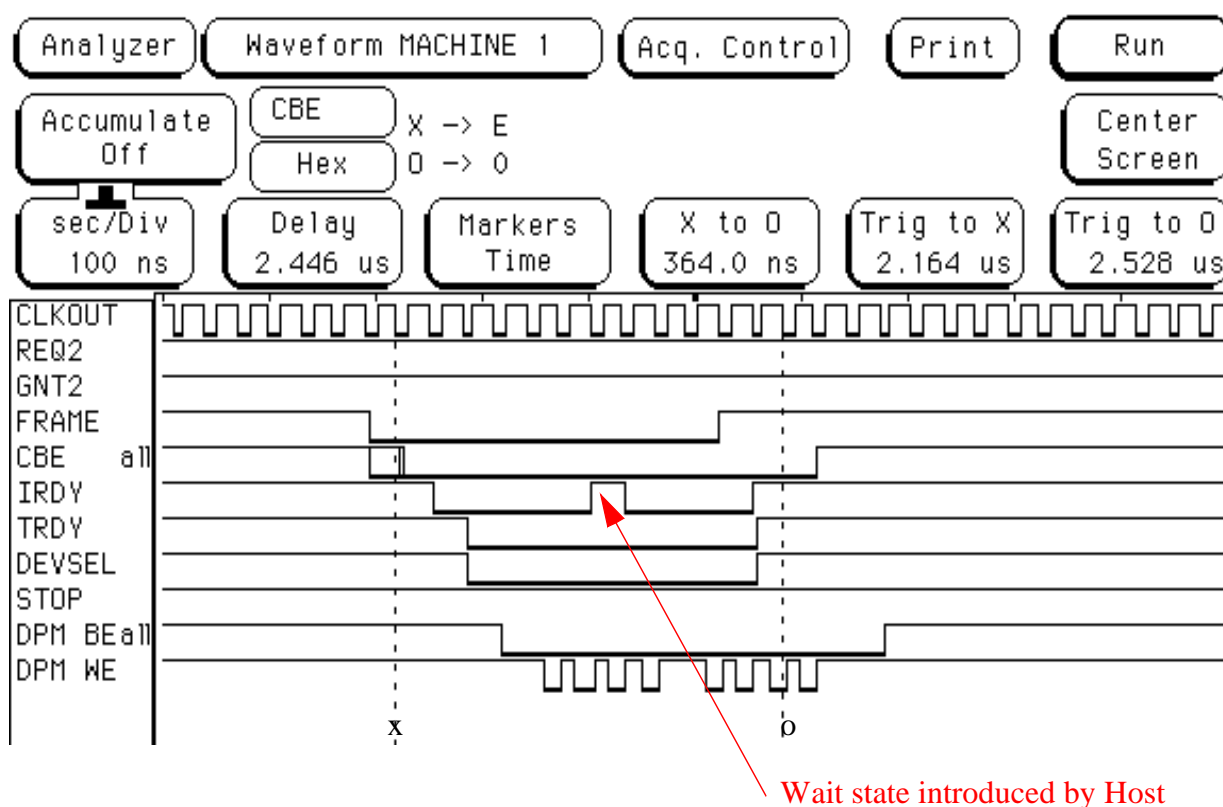
Burst vs single transfers

P-P Latency test with RIO: Ring 12 us / Switched System 12.5 us (including SW)



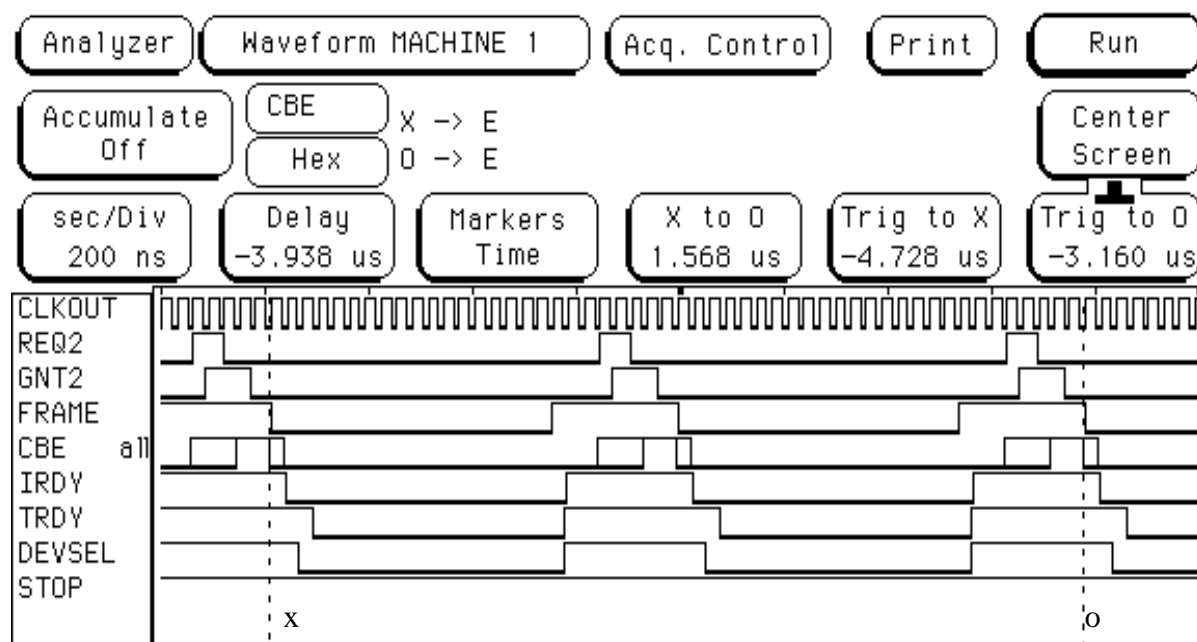
PCI slave results

- Logic Analyser Trace.
- Burst transfer is generated by CPU to access the DPM.



PCI master results

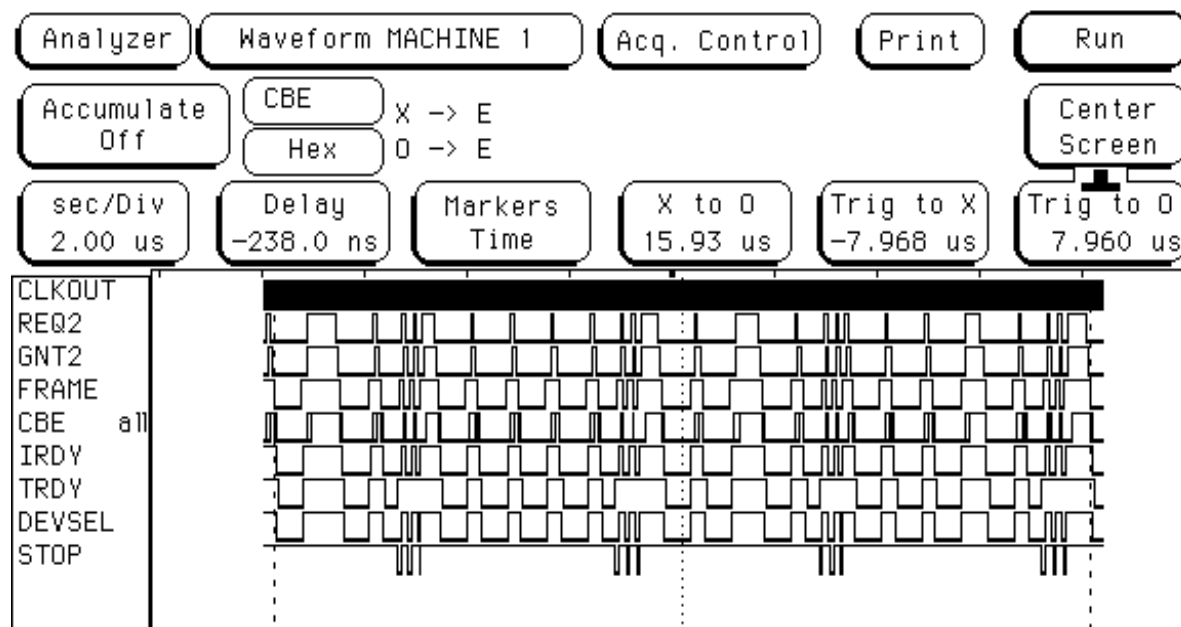
- Master performance



2*64 bytes in 1.568us -> **Peak_Bandwidth=81.6 MBytes/s**

PCI Master Performance for Write: 81.6MBytes/s

- Host performance when master is activated



17*64 in 15.93us -> **Average_Bandwidth=68.3MBytes/s**

Host PCI Performance: ~68.5 MBytes/s