

TTC-VMEbus INTERFACE

(TTCvi)

RD12 Project

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This note describes the RD12 TTC-VMEbus interface (TTCvi) module, which interfaces the TTC system to the Central Trigger Processor (Global Trigger) and to the control processors or development workstations which generate commands and data to be transmitted to the front-end electronics controllers. The note is updated at intervals.

1. Introduction

The TTCvi module is a key component of the RD12 TTC system described in <http://www.cern.ch/TTC/intro.html>. It delivers the A Channel and B Channel signals to the TTC transmitter crate for multiplexing, encoding, optical conversion and distribution to the TTCrx ASICs associated with the front-end electronics controllers.

To minimise the possibility of configuration errors, the characteristics of the module and the signal routing which it controls are fully programmable from the VMEbus.

The TTC **A Channel** is used to transmit the Level-1 Accept (L1A) signal. The TTCvi incorporates a programmable L1A source selector and an internal trigger emulator for test purposes.

The TTC **B Channel** is used to transmit framed and formatted commands and data. These can be either:

- Short-format synchronous or asynchronous broadcast command/data cycles. If synchronous, the timing of these cycles relative to the LHC orbit is controlled precisely. They are used for the broadcasting of the bunch counter reset signals which control the phases of the TTCrx bunch counters, and for the transmission of other fast synchronous broadcast controls and test commands or data.

These commands are deskewed in the TTCrx ASICs to compensate for individual differences in fibre propagation delay, electronics and detector delays and particle times-of-flight.

- Long-format asynchronous individually-addressed or broadcast command/data cycles. The timing of these cycles with respect to the LHC orbit is indeterminate and they are not individually deskewed in TTCrx ASICs. They are used for the transmission of parameters, test data, calibration data and non time-critical commands, such as channel masks, to the front-end electronics.

2. Clock inputs

The TTCvi module is normally driven by a 40.08 MHz clock signal which it receives from the TTC transmitter crate, and which is phase-locked to the LHC clock (or to a local clock generator when that signal is not available). In order to allow compensation for different cable lengths between the TTCvi and the TTC encoder, the phase of the input clock can be adjusted by means of a rotary switch on the TTCvi. The delay value can be read through VME.

This adjustment is made on installation of the module such that the A and B Channel data output signals from the TTCvi are delivered to the TTC encoder within the appropriate phase window. Once set up, it should not be altered unless the cable lengths between the TTCvi and the TTC transmitter crate are changed.

For test purposes one can select the clock used by the TTCvi from two sources:

- 1 front panel input which is the normal clock from the TTC transmitter crate.
- an internal 40.08 MHz oscillator (not phase-locked to the TTC system).

The selection is made by means of a VME register and the selected clock is available as a front panel output. The A and B Channel outputs from the TTCvi can only be transmitted by the TTC system when the TTC transmitter clock is used.

3. Trigger inputs

Although in normal running the trigger input to the module is the L1A signal provided by the Central Trigger Processor, the TTCvi allows other trigger sources to be selected for test or calibration purposes without modifying the cabling. These sources are synchronised with the TTC transmitter 40.08 MHz clock in the TTCvi.

The latency introduced by the module on the L1A coming from the CTP is minimized. In particular no resynchronisation with the clock is done.

Four front panel external inputs (including the one for the standard L1A input) are provided, with programmable selection of the one in use. In addition, it is possible to generate a trigger by a VME access to a key address and an internal random trigger generator is provided for test purposes. The internal generator provides a L1A signal; the number of L1A per unit of time follows a Poisson distribution with a mean rate programmable from about 1 Hz to 160 kHz.

The selected trigger is made available as a front panel output for monitoring purposes.

An internal 24-bit event counter (which can be read and written through VME) counts the number of triggers sent.

4. Test trigger generation

An internal random signal generator with a period of $2.15 \cdot 10^9$ allows L1A sequences to be generated for test purposes. A 16-bit “rate” register is used to define the average rate of trigger accepts generated.

The average rate can be selected in the following values: 1 Hz, 100 Hz, 1 kHz, 10 kHz, 20 kHz, 40 kHz, 80 kHz, 100 kHz and 160 kHz.

Internal logic further limits the effective L1A rate by forcing a minimum dead time of 2 clock cycles between trigger accepts and by limiting to 16 the number of L1A sent within any interval of 16 μ s.

5. Orbit input

The orbit signal is a square wave of period 88.924 μ s which is received from the LHC machine and distributed to the TTCvi and other components for the generation of signals which are synchronised to the LHC orbit. Adjustment of the phase of the orbit signal permits a global control of the timing of the entire TTC system relative to the LHC bunch structure.

To allow tests to be performed when the LHC orbit signal is not available, the TTCvi incorporates an internal pseudo orbit signal source obtained by dividing the 40.08 MHz clock by 3564. Selection between the front panel input of the LHC orbit signal and the internal source is made by a VME register and the selected signal is made available as a front panel output.

6. Inhibit<3..0> signals

Four independently-programmable timing signals called Inhibit<3..0> are generated within the TTCvi module for use in sending synchronous commands at controllable times relative to the LHC orbit. Each Inhibit signal starts a programmable (12-bit) number of clock cycles after the start of the orbit signal and has a duration of a programmable (8-bit) number of clock cycles. Transmission of the associated synchronous command commences at the end of the Inhibit signal duration.

Each Inhibit signal is assigned a different priority level, such that Inhibit<0> has higher priority than Inhibit<1>, etc. When an Inhibit signal becomes active, the transmission of any command associated with a lower priority Inhibit is allowed to complete, but further such commands are held off until the higher priority one has been sent. Since the Inhibit signals are always programmed to have a duration exceeding that required for the transmission

of even a long-format cycle (about 1.05 μ s), the higher priority signal is always transmitted at a determinate time relative to the LHC orbit.

The highest priority Inhibit <0> is used to trigger the transmission, during the LHC extractor gap, of a broadcast command containing the bunch counter reset. This signal, after deskewing in the individual receiver ASICs, is used to control the phase of the TTCrx bunch counters. The three other Inhibit signals are available for the generation of other synchronous commands including those required for triggering test pulse generators. All four Inhibit signals are made available as front panel outputs for monitoring purposes.

Through appropriate preprogramming, one can ensure that synchronous commands at all priority levels are always sent at well defined times.

For asynchronous cycles, the highest priority is given to the broadcast of L1A number and trigger type, then VME mapped cycles and then B-Go<0> to B-Go<3>.

7. Generation of B Channel cycles

The TTCvi permits synchronous and asynchronous short- and long-format B Channel command/data cycles to be generated in a number of different ways:

- Short- and long-format asynchronous cycles.

Asynchronous cycles may be initiated by writing the required data (a single byte for short-format or two 16-bit words for long-format) to specified TTCvi VME addresses. Normally short-format cycles are used for broadcast commands or data while long-format cycles are used for individually-addressed commands or data. However, a broadcast of 16 bits of data can be made with long-format cycles if TTCrx address 0 is chosen. The timing of these cycles is not synchronised with the LHC orbit.

- Pre-loaded synchronous or asynchronous cycles.

Four VME-addressable FIFOs are provided which may be pre-loaded with commands and data to be transmitted by B Channel cycles. For each of the four channels, the actual transmission of the pre-loaded information is initiated by a signal called B-Go<3..0> which can be generated either by a VME write to a key address or by an external signal applied to one of four front panel inputs. It's also possible to start the cycle transmission as soon as the FIFO is not empty. This last mode will facilitate the use of several TTCvi's in a single crate by reducing the VME access time: one can fill the FIFO in DMA mode and start the transmission as soon as the FIFO is not

empty. CSR2 is used to monitor the status of the FIFO. Sequences of B Channel cycles can be generated by loading the FIFOs with several parameters...In addition, a mode allows to load the FIFO once and to transmit allways the same cycle(s) by resetting the read pointer of the FIFO as soon as it is empty. This is used for instance to transmit repetitive commands such as Bunch Counter Reset. The VME access to the FIFO is D32 only and supports block mode.

A VME-addressable register associated with each of the channels allows the selection of synchronous or asynchronous mode, and VME or front panel generation of B-Go.

If synchronous mode is selected, the B-channel cycle is generated at the end of the Inhibit<i> signal. The cycle can be programmed to be either single or repetitive. In single mode, only one cycle is generated if a B-Go<i> has occurred before Inhibit<i>. In repetitive mode, the cycle is generated at the end of each Inhibit<i> signal (i.e., once per LHC orbit) and does not require B-Go<i> to occur. The bunch counter reset command, for example, is sent with this repetitive mode.

If asynchronous mode is selected, the B Channel cycle is generated when the B-Go<i> signal occurs. There will be one cycle and one cycle only for each occurrence of the signal.

- Event number and trigger type cycle.

After each L1A is transmitted, the contents of the 24-bit event counter in the TTCvi can optionally be broadcast together with an 8-bit trigger type parameter which is received from the Central Trigger Processor via a front panel connection. This broadcast, which is intended for check purposes, is made asynchronously and takes about 4.4 μ s if the B Channel is free. The following sub-addresses of the long B-Channel cycle are used:

- 0 Trigger type on the 8 data bits.
- 1 Event Number <23..16> on the 8 data bits.
- 2 Event Number <15..8> on the 8 data bits.
- 3 Event Number <7..0> on the 8 data bits.

Internally, the event number and the trigger type are stored in FIFOs to avoid any losses due to the random time of arrival of L1A. The status of these FIFOs is available in a CSR register.

8. TTCvi registers and VME address map

The TTCvi module is A24/D32, D16 and D08(E0). Four rotary switches are used to set the base address (A23 to A8).

Short-format asynchronous cycles

- **\$C4:** B Channel short-format asynchronous broadcast access.

D7 to D0
8b COMMAND

Long-format asynchronous cycles

- **\$C2/ \$C0:** B Channel long-format individually-addressed (or broadcast with TTCrx = 0) access.

E=0 accesses TTCrx internal registers. E=1 is for access to external subaddresses in the associated front-end electronics.

Address \$C0

D15	D14 to D1	D0
1	14b TTCrx ADDR	E

Address \$C2

D15 to D8	D7 to D0
8b SUBADDR	8b DATA

Transmission starts after the second address has been loaded from VME if one uses D16 transfer. It is not necessary to reload the first address in order to access additional subaddresses associated with the same TTCrx.

CSR1. Input selection and timing.

- **\$80:** Clock, Trigger and Orbit signal selection.
Read and Write word access.

bit	R/W	Function	Comments
15	-	Spare	
14	R/W	Random Trigger Rate MSB	100k, 80k, 40k
13	R/W	Random Trigger Rate	20k, 10k, 1k
12	R/W	Random Trigger Rate LSB	100Hz, 1Hz
11	R	BC delay MSB	Read BC delay switch value
10	R	BC delay	2 ns/step
09	R	BC delay	
08	R	BC delay LSB	
07	R	VME transfer pending	if "1" a VME request is still pending
06	W	L1A FIFO reset	if set to "1"
05	R	L1A FIFO empty	if "1"
04	R	L1A FIFO full	if "1"
03	R/W	Orbit signal select	external ORBIT if set to "0"
02	R/W	L1A trigger select MSB	VME funct if 4, Random if 5
01	R/W	L1A trigger select	L1A<2> if 2, L1A<3> if 3
00	R/W	L1A trigger select LSB	L1A<0> if 0, L1A<1> if 1

CSR2. FIFO's status.

- **\$82:** FiFo's flags and use
Read and Write word access.

bit	R/W	Function	Comments
15	W	Reset B-Go FIFO 3	if set to "1"
14	W	Reset B-Go FIFO 2	if set to "1"
13	W	Reset B-Go FIFO 1	if set to "1"
12	W	Reset B-Go FIFO 0	if set to "1"
11	R/W	Retransmit B-Go FIFO 3	if set to "0" when EMPTY
10	R/W	Retransmit B-Go FIFO 2	if set to "0" when EMPTY
09	R/W	Retransmit B-Go FIFO 1	if set to "0" when EMPTY
08	R/W	Retransmit B-Go FIFO 0	if set to "0" when EMPTY
07	R	B-Go FIFO 3 FULL	if "1"
06	R	B-Go FIFO 3 EMPTY	if "1"
05	R	B-Go FIFO 2 FULL	if "1"
04	R	B-Go FIFO 2 EMPTY	if "1"
03	R	B-Go FIFO 1 FULL	if "1"
02	R	B-Go FIFO 1 EMPTY	if "1"
01	R	B-Go FIFO 0 FULL	if "1"
00	R	B-Go FIFO 0 EMPTY	if "1"

Software L1A generation

- **\$86:** a write byte cycle at this address generates an L1A if L1AEN = 1 and L1ATEST = 1.

Inhibit<0>

- **\$92:** Inhibit<0> delay in number of clock cycles

Read and Write word access.

D11 to D0
Delay

- **\$94:** Inhibit<0> duration in number of clock cycles

Read and write byte access.

D7 to D0
Duration

If Duration is equal to zero, there is no Inhibit<0> signal.

Inhibit<1>

- **\$9A:** Inhibit<1> delay in number of clock cycles

Read and Write word access.

D11 to D0
Delay

- **\$9C:** Inhibit<1> duration in number of clock cycles

Read and write byte access.

D7 to D0
Duration

If Duration is equal to zero, there is no Inhibit<1> signal.

Inhibit<2>

- **\$A2:** Inhibit<2> delay in number of clock cycles

Read and Write word access.

D11 to D0
Delay

- **\$A4:** Inhibit<2> duration in number of clock cycles

Read and write byte access.

D7 to D0
Duration

If Duration is equal to zero, there is no Inhibit<2> signal.

Inhibit<3>

- **\$AA:** Inhibit<3> delay in number of clock cycles

Read and Write word access.

D11 to D0
Delay

- **\$AC**: Inhibit<3> duration in number of clock cycles
Read and write byte access.

D7 to D0
Duration

If Duration is equal to zero, there is no Inhibit<3> signal.

B-Go<0>

- **\$90**: mode selection for B-Go<0>
Read and write byte access.

D3	D2	D1	D0
Fifo	Single	Sync	Enable

Single	0	Single mode
	1	Repetitive mode
Sync	0	Synchronous cycle
	1	Asynchronous cycle
Enable	0	Front panel input enable
	1	Front panel input disable
Fifo	0	Start cycle as soon as FIFO0 is not empty
	1	Don't look at FIFO status

- **\$96**: a write byte access at this address generates a B-Go<0> signal (if Enable is equal to 1).

B-Go<1>

- **\$98**: mode selection for B-Go<1>

Read and write byte access.

D3	D2	D1	D0
Fifo	Single	Sync	Enable

Single	0	Single mode
	1	Repetitive mode
Sync	0	Synchronous cycle
	1	Asynchronous cycle
Enable	0	Front panel input enable
	1	Front panel input disable
Fifo	0	Start cycle as soon as FIFO1 is not empty
	1	Don't look at FIFO status

- **\$9E**: a write byte access at this address generates a B-Go<1> signal (if Enable is equal to 1).

B-Go<2>

- **\$A0**: mode selection for B-Go<2>

Read and write byte access.

D3	D2	D1	D0
Fifo	Single	Sync	Enable

Single	0	Single mode
	1	Repetitive mode
Sync	0	Synchronous cycle
	1	Asynchronous cycle
Enable	0	Front panel input enable
	1	Front panel input disable
Fifo	0	Start cycle as soon as FIFO2 is not empty
	1	Don't look at FIFO status

- **\$A6**: a write byte access at this address generates a B-Go<2> signal (if Enable is equal to 1).

B-Go<3>

- **\$A8**: mode selection for B-Go<3>

Read and write byte access.

D3	D2	D1	D0
Fifo	Single	Sync	Enable

Single	0	Single mode
	1	Repetitive mode
Sync	0	Synchronous cycle
	1	Asynchronous cycle
Enable	0	Front panel input enable
	1	Front panel input disable
Fifo	0	Start cycle as soon as FIFO3 is not empty
	1	Don't look at FIFO status

- **\$AE**: a write byte access at this address generates a B-Go<3> signal (if Enable is equal to 1).

L1A Number

- **\$88 / \$8A**: L1A number

Read and Write word access or long word access at address \$88.

Address \$88

D7 to D0
L1A# bit 23 to 16

Address \$86

D15 to D0
L1A# bit 15 to 0

B Channel Data for B-Go<0>

- **\$B0:** B Channel data associated to B-Go<0>

If a long-format cycle is used, 32 bits are necessary with the following mapping:

Address \$B0

D31	D30 to D17	D16	D15 to D8	D7 to D0
1	14b TTCrx ADDR	E	8b SUBADDR	8b DATA

If a short-format cycle is used, 9 bits are necessary with the following mapping:

Address \$B0

D31	D30 to D23	D22 to D0
0	8b COMMAND	X

These registers are FIFOs (256 depth), which may be pre-loaded with sequences of B Channel cycles.

B Channel Data for B-Go<1>

- **\$B4:** B Channel data associated to B-Go<1>

If a long-format cycle is used, 32 bits are necessary with the following mapping:

Address \$B4

D31	D30 to D17	D16	D15 to D8	D7 to D0
1	14b TTCrx ADDR	E	8b SUBADDR	8b DATA

If a short-format cycle is used, 9 bits are necessary with the following mapping:

Address \$B4

D31	D30 to D23	D22 to D0
0	8b COMMAND	X

These registers are FIFOs (256 depth), which may be pre-loaded with sequences of B Channel cycles.

B Channel Data for B-Go<2>

- **\$B8**: B Channel data associated to B-Go<2>

If a long-format cycle is used, 32 bits are necessary with the following mapping:

Address \$B8

D31	D30 to D17	D16	D15 to D8	D7 to D0
1	14b TTCrx ADDR	E	8b SUBADDR	8b DATA

If a short-format cycle is used, 9 bits are necessary with the following mapping:

Address \$B8

D31	D30 to D23	D22 to D0
0	8b COMMAND	X

These registers are FIFOs (256 depth), which may be pre-loaded with sequences of B Channel cycles.

B Channel Data for B-Go<3>

- **\$BC**: B Channel data associated to B-Go<3>

If a long-format cycle is used, 32 bits are necessary with the following mapping:

Address \$BC

D31	D30 to D17	D16	D15 to D8	D7 to D0
1	14b TTCrx ADDR	E	8b SUBADDR	8b DATA

If a short-format cycle is used, 9 bits are necessary with the following mapping:

Address \$BC

D31	D30 to D23	D22 to D0
0	8b COMMAND	X

These registers are FIFOs (256 depth), which may be pre-loaded with sequences of B Channel cycles.

Module Identifier

- **\$00**: A read only 8 bit word. Format to be defined.

VME ADDRESS MAP SUMMARY

Addr. Offset	Register	R/W	Access	Remarks
CE				
CC				
CA				
C8				
C6				
C4	Short VMEcycle	W	W 8	DATA<7..0>
C2	Long VMEcycle LSW	W	LW/W	
C0	Long VMEcycle MSW	W	LW/W	
BE	Bgo<3> Param. LSW	W	LW/W	Bgo FIFO <3>
BC	Bgo<3> Param. MSW	W	LW/W	Bgo FIFO <3>
BA	Bgo<2> Param. LSW	W	LW/W	Bgo FIFO <2>
B8	Bgo<2> Param. MSW	W	LW/W	Bgo FIFO <2>
B6	Bgo<1> Param. LSW	W	LW/W	Bgo FIFO <1>
B4	Bgo<1> Param. MSW	W	LW/W	Bgo FIFO <1>
B2	Bgo<0> Param. LSW	W	LW/W	Bgo FIFO <0>
B0	Bgo<0> Param. MSW	W	LW/W	Bgo FIFO <0>
AE	Bgo<3> SW-Go	W	W	data-less function
AC	Inh<3> Duration	R/W	W 8	DATA<7..0>
AA	Inh<3> Delay	R/W	W 12	DATA<11..0>
A8	Bgo<3> Mode	R/W	W 4	DATA<3..0> see bit map
A6	Bgo<2> SW-Go	W	W -	data-less function
A4	Inh<2> Duration	R/W	W 8	DATA<7..0>
A2	Inh<2> Delay	R/W	W 12	DATA<11..0>
A0	Bgo<2> Mode	R/W	W 4	DATA<3..0> see bit map
9E	Bgo<1> SW-Go	W	W -	data-less function
9C	Inh<1> Duration	R/W	W 8	DATA<7..0>
9A	Inh<1> Delay	R/W	W 12	DATA<11..0>
98	Bgo<1> Mode	R/W	W 4	DATA<3..0> see bit map
96	Bgo<0> SW-Go	W	W -	data-less function
94	Inh<0> Duration	R/W	W 8	DATA<7..0>
92	Inh<0> Delay	R/W	W 12	DATA<11..0>
90	Bgo<0> Mode	R/W	W 4	DATA<3..0> see bit map
8E				
8C				
8A	Event-Count LSW	R/W	W 16	
88	Event-Count MSW	R/W	W 16	
86	SW-L1A	W	W -	data-less function
84	SW-RST	W	W -	data-less function
82	CSR2	R/W	W 16	see bit map
80	CSR1	R/W	W 16	see bit map
00	Conf. EEPROM	R/(W)	W 8	LSBytes in every Long Word. See specs.

9. Front panel signals

The following signals are available on the front panel:

Name	Description	Standard
L1A In 0	L1A input from CTP	ECL active low
L1A In 1	User L1A Input	NIM
L1A In 2	User L1A Input	NIM
L1A In 3	User L1A Input	NIM
Trigger Out	Selected L1A output	NIM
Clock In 0	Input clock	ECL
Clock Out N	Selected Clock Output	NIM
Clock Out D	Delayed Selected Clock Output	NIM
Orbit In	Orbit Input	ECL
Orbit Out	Selected Orbit Output	NIM
B-Go 0	B-Go 0 Input	NIM
B-Go 1	B-Go 1 Input	NIM
B-Go 2	B-Go 2 Input	NIM
B-Go 3	B-Go 3 Input	NIM
Inhibit 0	Inhibit 0 Output	NIM
Inhibit 1	Inhibit 1 Output	NIM
Inhibit 2	Inhibit 2 Output	NIM
Inhibit 3	Inhibit 3 Output	NIM
A-Ch	A-Ch Output	ECL
B-Ch	B-Ch Outtput	ECL
Trigger Type	Trigger Type Input	Differential ECL

10. Power supplies

This module requires +5V, -5.2V and -2V. The last 2 power supplies are used by the ECL part of the module. Due to lack of space, it has not been possible to implement either a DC-DC converter or a voltage regulator.

These extra power lines are taken from the Jaux connector.

11. TTCvi front panel

