TTC-VMEbus INTERFACE

TTCvi

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RD12 Project

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TTC-VMEbus INTERFACE

(TTCvi)

This note describes the RD12 TTC-VMEbus interface (TTCvi) module, which interfaces the TTC system to the Central Trigger Processor (Global Trigger) and to the control processors or development workstations which generate commands and data to be transmitted to the front-end electronics controllers. The note is updated at intervals.

Introduction

The TTCvi module is a key component of the RD12 TTC system described in **http://www.cern.ch/TTC/intro.html**. It delivers the A Channel and B Channel signals to the TTC transmitter crate for multiplexing, encoding, optical conversion and distribution to the TTCrx ASICs associated with the front-end electronics controllers. To minimise the possibility of configuration errors, the characteristics of the module and the signal routing which it controls are fully programmable from the VMEbus.

The TTC **A Channel** is used to transmit the Level-1 Accept (L1A) signal. The TTCvi incorporates a programmable L1A source selector and an internal trigger emulator for test purposes.

The TTC **B Channel** is used to transmit framed and formatted commands and data. These can be either:

- Short-format synchronous or asynchronous broadcast command/data cycles. If synchronous, the timing of these cycles relative to the LHC orbit is controlled precisely. They are used for the broadcasting of the bunch counter reset signals which control the phases of the TTCrx bunch counters, and for the transmission of other fast synchronous broadcast controls and test commands or data. These commands are deskewed in the TTCrx ASICs to compensate for individual differences in fibre propagation delay, electronics and detector delays and particle times-of-flight.

- Long-format asynchronous individually-addressed or broadcast command/data cycles. The timing of these cycles with respect to the LHC orbit is indeterminate and they are not individually deskewed in TTCrx ASICs. They are used for the transmission of parameters, test data, calibration data and non time-critical commands, such as channel masks, to the front-end electronics.

Clock Inputs

The TTCvi module is normally driven by a 40.08 MHz clock signal which it receives from the TTC transmitter crate, and which is phase-locked to the LHC clock (or to a local clock generator when that signal is not available). In order to allow compensation for different cable lengths between the TTCvi and the TTC encoder, the phase of the input clock can be adjusted by means of a rotary switch on the TTCvi. The delay value can be read through the TTCvi status register CSR1. This adjustment is made on installation of the module such that the A and B Channel data output signals from the TTCvi are delivered to the TTC encoder within the appropriate phase window. Once set up, it should not be altered unless the cable lengths between the TTCvi and the TTC transmitter crate are changed.

If the external TTC clock source is removed from the front panel input of the TTCvi an internal 40.00 MHz clock is automatically selected in order to keep all the module internal logic working. A front panel indicator (**BC-EXT**) show which clock is running. The external clock input is marked **CLOCK IN bc/ecl** on the front panel and is 50Ω AC coupled and expecting ECL levels.

Trigger Inputs

Although in normal running the trigger input to the module is the L1A signal provided by the Central Trigger Processor, the TTCvi allows three other trigger sources to be selected for test or calibration purposes without modifying the cabling. These sources are synchronised with the TTC transmitter 40.08 MHz clock in the TTCvi.

The latency introduced by the module on the L1A coming from the CTP is minimised. In particular no resynchronisation with the clock is done.

Four front panel external inputs (including the one for the standard L1A input) are provided (**L1A IN<0..3>**), with programmable selection of the one in use. In addition, it is possible to generate a trigger by a VME access to a key address and an internal random trigger generator is provided for test purposes. An internal generator provides a L1A signal; the number of L1A per unit of time follows a Poisson distribution with a mean rate programmable from about 1 Hz to 100 kHz. The selected trigger is made available as two front panel NIM outputs (**TRIGGER OUT<0..1>**) for monitoring purposes. The trigger output pulse duration is 25 ns.
An internal 24-bit event counter (which can be read and written through VME) counts the number of triggers sent.
The trigger source is selected by setting bits in the control register CSR1. The selection is shown on the front panel indicators **L1A-SEL(0..2)**.

Test Trigger Random Generation

The internal random signal generator has a period of 2.15 10^9 allowing L1A sequences to be generated for test purposes. A 16-bit “rate” register is used to define the average rate of trigger accepts generated. The average rate can be selected in the following values: 1 Hz, 100 Hz, 1 kHz, 5kHz, 10 kHz, 25 kHz, 50 kHz and 100 kHz. The rate is selected by setting a value in CSR1. Internal logic further limits the effective L1A rate by forcing a minimum dead time of 2 clock cycles between trigger accepts and by limiting to 16 the number of L1A sent within any interval of 16 µs.

Orbit Input

The orbit signal is a square wave of period 88.924 µs which is received from the LHC machine and distributed to the TTCvi and other components for the generation of signals which are synchronised to the LHC orbit. Adjustment of the phase of the orbit signal permits a global control of the timing of the entire TTC system relative to the LHC bunch structure. The LHC orbit signal is received as a 50Ω AC coupled ECL signal on the front panel connector marked **ORBIT in/ecl**.

To allow tests to be performed when the LHC orbit signal is not available, the TTCvi incorporates an internal pseudo orbit signal source obtained by dividing the 40.08 MHz clock by 3564. Selection between the front panel input of the LHC orbit signal and the internal source is made by setting a bit in the CSR1 register and the selected signal is made available as a front panel NIM output marked **ORBIT out/nim**. The presence of the external orbit signal may also be monitored on the front panel indicator **ORBIT**.

Inhibit<3..0> Signals

Four independently programmable timing signals called Inhibit<3..0> are generated within the TTCvi module for use in sending synchronous commands at controllable times relative to the LHC orbit.

At each Orbit signal all four inhibit timing generators are started. The orbit to the inhibit delay is set by a 0 - 100 µs programmable timer (12-bits) and the inhibit duration by a 0 - 6.4 µs timer (8-bits). The timers are controlled by the selected clock, which means timing may be adjusted in steps of approximately 25 ns. Transmission of the associated synchronous command commences at the end of the Inhibit signal duration.

Each Inhibit signal is assigned a different priority level, such that Inhibit<0> has higher priority than Inhibit<1>, etc. When an Inhibit signal becomes active, the transmission of any command associated with a lower priority Inhibit is allowed to complete, but further such commands are held off until the higher priority one has been sent. Since the Inhibit signals are always programmed to have a duration exceeding that required for the transmission of even a long-format cycle (about 1.05 μs), the higher priority signal is always transmitted at a determinate time relative to the LHC orbit.

The highest priority Inhibit <0> is used to trigger the transmission, during the LHC extractor gap, of a broadcast command containing the bunch counter reset. This signal, after deskewing in the individual receiver ASICs, is used to control the phase of the TTCrx bunch counters. The three other Inhibit signals are available for the generation of other synchronous commands including those required for triggering test pulse generators. All four Inhibit signals are made available as front panel NIM level outputs for monitoring purposes.(**INHIBIT OUT/nim<0..3>**)

Through appropriate preprogramming, one can ensure that synchronous commands at all priority levels are always sent at well defined times.

For asynchronous cycles, the highest priority is given to the broadcast of L1A number and trigger type, then VME mapped cycles and then B-Go<0> to B-Go<3>.

Generation of B Channel cycles

The TTCvi permits synchronous and asynchronous short- and long-format B Channel command/data cycles to be generated in a number of different ways:

Short- and long-format asynchronous cycles

Asynchronous cycles may be initiated by writing the required data (a single byte for short-format or two 16-bit words for long-format) to specified TTCvi VME addresses. Normally short-format cycles are used for broadcast commands or data while long-format cycles are used for individually-addressed commands or data. However, a broadcast of 16 bits of data can be made with long-format cycles if TTCrx address 0 is chosen. The timing of these cycles is not synchronised with the LHC orbit.

Pre-loaded synchronous or asynchronous cycles

Four VME-addressable FIFO's are provided which may be pre-loaded with commands and data to be transmitted by B Channel cycles. For each of the four channels, the actual transmission of the pre-loaded information is initiated by a signal called B-Go<3..0> which can be generated either by a VME write to a key address or by an external signal applied to one of four front panel inputs. It is also possible to start the cycle transmission as soon as the FIFO is not empty. This last mode will facilitate the use of several TTCvi's in a single crate by reducing the VME access time: one can fill the

FIFO in DMA mode (VME block transfers) and start the transmission as soon as the FIFO is not empty. The register CSR2 is used to monitor the status of the FIFO's. Sequences of B Channel cycles can be generated by loading the FIFO's with several parameters. In addition, a mode allows to load the FIFO once and to transmit always the same cycle(s) by resetting the read pointer of the FIFO as soon as it is empty. This is used for instance to transmit repetitive commands such as Bunch Counter Reset. The VME access to the FIFO is D32 only and supports block transfer mode.

A VME-addressable B-Go mode register associated with each of the four channels allows the selection of synchronous or asynchronous mode of either VME or front panel initiated B-Go cycles.

If synchronous mode is selected, the B-channel cycle is generated at the end of the Inhibit<i> signal. The cycle can be programmed to be either single or repetitive. In single mode, only one cycle is generated if a B-Go<i> has occurred before Inhibit<i>. In repetitive mode, the cycle is generated at the end of each Inhibit<i> signal (i.e. once per LHC orbit) and does not require a B-Go<i> to occur. The bunch counter reset command, for example, is sent with this repetitive mode.

If asynchronous mode is selected, the B Channel cycle is generated only once each time the B-Go<i> signal occurs.

Event Number and Trigger Type cycle

After each L1A is transmitted, the contents of the 24-bit event counter in the TTCvi is broadcast together with an 8-bit trigger type parameter, which is received from the Central Trigger Processor via a front panel connection. This broadcast, which is intended for check purposes, is made asynchronously and takes about 4.4 µs if the B Channel is free. The following sub-addresses of the long B-Channel cycle are used:

- 0 Trigger type on the 8 data bits.
- 1 Event Number <23..16> on the 8 data bits.
- 2 Event Number <15..8> on the 8 data bits.
- 3 Event Number <7..0> on the 8 data bits.

Internally, the event number and the trigger type are stored in FIFO's to avoid any losses due to the random time of arrival of L1A. The status of these FIFO's are available in the CSR1 register. The TTC address of this transfer is set provisionally to *external* 0007, but may be altered by reprogramming the firmware.

TTCvi Registers and VME Address Map

Address Modifiers

The TTCvi module is A24, A16 / D32, D16 and responds to the following Address Modifiers:

Standard:	39, 3A, 3D, 3E	
Short:	29, 2D	
Block:	0F, 0B, 3B, 3F	
Extended:	09, 0A, 0D, 0E	(in order to respond to some CPU's)

Four rotary switches are used to set the base address (A23 to A8).

Short-format asynchronous cycles

• **$C4**: B Channel short-format asynchronous broadcast access.

D7 to D0
8b COMMAND

Long-format asynchronous cycles

• **$C2/ $C0**: B Channel long-format individually-addressed (or broadcast with TTCrx = 0) access.
E=0 accesses TTCrx internal registers. E=1 is for access to external subaddresses in the associated front-end electronics.

Address $C0

D15	D14 to D1	D0
1	14b TTCrx ADDR	E

Address $C2

D15 to D8	D7 to D0
8b SUBADDR	8b DATA

Transmission starts after the second address ($C2) has been loaded from VME if one uses D16 transfer. It is not necessary to reload the first address in order to access additional subaddresses associated with the same TTCrx.

CSR1. Input selection and timing.

• **$80**: Clock, Trigger and Orbit signal selection.
Read and Write word access.

bit	R/W	Function	Comments
15	-	Spare	
14	R/W	Random Trigger Rate MSB	‘7’ = 100k, ‘6’ = 50k, ‘5’ = 25k
13	R/W	Random Trigger Rate	‘4’ = 10k, ‘3’ = 5k, ‘2’ = 1k
12	R/W	Random Trigger Rate LSB	‘1’ = 100Hz, ‘0’ = 1Hz
11	R	BC delay MSB	Read BC delay switch value
10	R	BC delay	2 ns/step
09	R	BC delay	***(NB bits <11..08> must inverted to***
08	R	BC delay LSB	***reflect correct switch setting)***
07	R	VME transfer pending	if “1” a VME request is still pending
06	W	L1A FIFO reset	if set to “1”
05	R	L1A FIFO empty	if “1”
04	R	L1A FIFO full	if “1”
03	R/W	Orbit signal select	external ORBIT if set to “0”
02	R/W	L1A trigger select MSB	VME function if 4, Random if 5
01	R/W	L1A trigger select	L1A<2> if 2, L1A<3> if 3
00	R/W	L1A trigger select LSB	L1A<0> if 0, L1A<1> if 1

CSR2. FIFO's status.

• **$82**: FIFO's flags and use
Read and Write word access.

bit	R/W	Function	Comments
15	W	Reset B-Go FIFO 3	if set to “1”
14	W	Reset B-Go FIFO 2	if set to “1”
13	W	Reset B-Go FIFO 1	if set to “1”
12	W	Reset B-Go FIFO 0	if set to “1”
11	R/W	Retransmit B-Go FIFO 3	if set to “0” when EMPTY
10	R/W	Retransmit B-Go FIFO 2	if set to “0” when EMPTY
09	R/W	Retransmit B-Go FIFO 1	if set to “0” when EMPTY
08	R/W	Retransmit B-Go FIFO 0	if set to “0” when EMPTY
07	R	B-Go FIFO 3 FULL	if “1”
06	R	B-Go FIFO 3 EMPTY	if “1”
05	R	B-Go FIFO 2 FULL	if “1”
04	R	B-Go FIFO 2 EMPTY	if “1”
03	R	B-Go FIFO 1 FULL	if “1”
02	R	B-Go FIFO 1 EMPTY	if “1”
01	R	B-Go FIFO 0 FULL	if “1”
00	R	B-Go FIFO 0 EMPTY	if “1”

Software module reset generation

• **$84**: a write word access to this address generates module reset. (data less function)

Software L1A generation

• **$86**: a write word access to this address generates a L1A test trigger if bits <2..0> = $4 in CSR1. (data less function)

Inhibit<0>

• **$92**: Inhibit<0> delay in number of clock cycles
Read and Write word access.

D11 to D0
Delay

• **$94**: Inhibit<0> duration in number of clock cycles
Read and Write word access.

D7 to D0
Duration

If Duration is equal to zero, there is no Inhibit<0> signal.

Inhibit<1>

• **$9A**: Inhibit<1> delay in number of clock cycles
Read and Write word access.

D11 to D0
Delay

• **$9C**: Inhibit<1> duration in number of clock cycles
Read and Write word access.

D7 to D0
Duration

If Duration is equal to zero, there is no Inhibit<1> signal.

Inhibit<2>

• **$A2**: Inhibit<2> delay in number of clock cycles
Read and Write word access.

D11 to D0
Delay

• **$A4**: Inhibit<2> duration in number of clock cycles
Read and Write word access.

D7 to D0
Duration

If Duration is equal to zero, there is no Inhibit<2> signal.

Inhibit<3>

• **$AA**: Inhibit<3> delay in number of clock cycles
Read and Write word access.

D11 to D0
Delay

• **$AC**: Inhibit<3> duration in number of clock cycles
Read and Write word access.

D7 to D0
Duration

If Duration is equal to zero, there is no Inhibit<3> signal.

B-Go<0>

• **$90**: mode selection for B-Go<0>
Read and Write word access.

D3	D2	D1	D0
FIFO	Single	Sync	Enable

Single	0	Single mode
	1	Repetitive mode
Sync	0	Synchronous cycle
	1	Asynchronous cycle
Enable	0	Front panel input enable
	1	Front panel input disable
FIFO	0	Start cycle as soon as FIFO<0> is not empty
	1	Don't look at FIFO status

• **$96**: a Write word access to this address generates a B-Go<0> signal (if Enable is equal to 1).

B-Go<1>

• **$98**: mode selection for B-Go<1>
Read and Write word access.

D3	D2	D1	D0
FIFO	Single	Sync	Enable

Single	0	Single mode
	1	Repetitive mode
Sync	0	Synchronous cycle
	1	Asynchronous cycle
Enable	0	Front panel input enable
	1	Front panel input disable
FIFO	0	Start cycle as soon as FIFO<1> is not empty
	1	Don't look at FIFO status

• **$9E**: a Write word access to this address generates a B-Go<1> signal (if Enable is equal to 1).

B-Go<2>

• **$A0**: mode selection for B-Go<2>
Read and Write word access.

D3	D2	D1	D0
FIFO	Single	Sync	Enable

Single	0	Single mode
	1	Repetitive mode
Sync	0	Synchronous cycle
	1	Asynchronous cycle
Enable	0	Front panel input enable
	1	Front panel input disable
FIFO	0	Start cycle as soon as FIFO<2> is not empty
	1	Don't look at FIFO status

• **$A6**: a Write word access to this address generates a B-Go<2> signal (if Enable is equal to 1).

B-Go<3>

• **$A8**: mode selection for B-Go<3>
Read and Write word access.

D3	D2	D1	D0
FIFO	Single	Sync	Enable

Single	0	Single mode
	1	Repetitive mode
Sync	0	Synchronous cycle
	1	Asynchronous cycle
Enable	0	Front panel input enable
	1	Front panel input disable
FIFO	0	Start cycle as soon as FIFO<3> is not empty
	1	Don't look at FIFO status

• **$AE**: a Write word access to this address generates a B-Go<3> signal (if Enable is equal to 1).

L1A Event Number Counter

- **$88 / $8A**: L1A Event Number Counter. Read and Write word access.

Address $88

D7 to D0
L1A# bit 23 to 16

Address $8A

D15 to D0
L1A# bit 15 to 0

B Channel Data for B-Go<0>

• **$B0**: B Channel data associated to B-Go<0>. VME Write LONGWORD access.

If a long-format TTC cycle is used, 32 bits are necessary with the following mapping:

Address $B0

D31	D30 to D17	D16	D15 to D8	D7 to D0
1	14b TTCrx ADDR	E	8b SUBADDR	8b DATA

If a short-format cycle is used, 9 bits are necessary with the following mapping:

Address $B0

D31	D30 to D23	D22 to D0
0	8b COMMAND	X

These registers are FIFO's (256 depth), which may be pre-loaded with mixed format sequences of B Channel cycles.

B Channel Data for B-Go<1>

• **$B4**: B Channel data associated to B-Go<1>. VME Write LONGWORD access.

If a long-format TTC cycle is used, 32 bits are necessary with the following mapping:

Address $B4

D31	D30 to D17	D16	D15 to D8	D7 to D0
1	14b TTCrx ADDR	E	8b SUBADDR	8b DATA

If a short-format cycle is used, 9 bits are necessary with the following mapping:

Address $B4

D31	D30 to D23	D22 to D0
0	8b COMMAND	X

These registers are FIFO's (256 depth), which may be pre-loaded with mixed format sequences of B Channel cycles.

B Channel Data for B-Go<2>

• **$B8**: B Channel data associated to B-Go<2>. VME Write LONGWORD access.

If a long-format TTC cycle is used, 32 bits are necessary with the following mapping:

Address $B8

D31	D30 to D17	D16	D15 to D8	D7 to D0
1	14b TTCrx ADDR	E	8b SUBADDR	8b DATA

If a short-format cycle is used, 9 bits are necessary with the following mapping:

Address $B8

D31	D30 to D23	D22 to D0
0	8b COMMAND	X

These registers are FIFO’s (256 depth), which may be pre-loaded with mixed format sequences of B Channel cycles.

B Channel Data for B-Go<3>

• **$BC**: B Channel data associated to B-Go<3>. VME Write LONGWORD access.

If a long-format TTC cycle is used, 32 bits are necessary with the following mapping:

Address $BC

D31	D30 to D17	D16	D15 to D8	D7 to D0
1	14b TTCrx ADDR	E	8b SUBADDR	8b DATA

If a short-format cycle is used, 9 bits are necessary with the following mapping:

Address $BC

D31	D30 to D23	D22 to D0
0	8b COMMAND	X

These registers are FIFO’s (256 depth), which may be pre-loaded with mixed format sequences of B Channel cycles.

Configuration - Identification EEPROM Mapping

• **$00**: Read Only 16 bit words, from address $26 to $4E. Write access if strap ST500 is fitted. Successive write cycles should be >5ms apart to allow for EEPROM write access time.

VME Address Offsets of 32 bit words					
MSBYTE			LSBYTE		
31 24	23 16	15 8	7 0		
20	21	22	23		
24	25	26	27	Manufacturer ID (CERN)	MSBYTE
28	29	2A	2B	Manufacturer ID (CERN)	
2C	2D	2E	2F	Manufacturer ID (CERN)	LSBYTE
30	31	32	33	Board ID / Serial No.	MSBYTE
34	35	36	37	Board ID / Serial No.	
38	39	3A	3B	Board ID / Serial No.	
3C	3D	3E	3F	Board ID / Serial No.	
40	41	42	43	Board Revision No.	MSBYTE
44	45	46	47	Board Revision No.	
48	49	4A	4B	Board Revision No.	
4C	4D	4E	4F	Board Revision No.	LSBYTE

The Manufacturer's Board Identification is on request supplied by IEEE (See ANSI/VITA 1-1994 VMEbus Specs. Appendix C)

VME Address Map Summary

Addr. Offset	Register	R/W	Access	Remarks
C4	Short VMEcycle	W	W 8	DATA<7..0>
C2	Long VMEcycle LSW	W	LW/W	
C0	Long VMEcycle MSW	W	LW/W	
BE	B-Go<3> Param. LSW	W	LW/W	B-Go FIFO <3>
BC	B-Go<3> Param. MSW	W	LW/W	B-Go FIFO <3>
BA	B-Go<2> Param. LSW	W	LW/W	B-Go FIFO <2>
B8	B-Go<2> Param. MSW	W	LW/W	B-Go FIFO <2>
B6	B-Go<1> Param. LSW	W	LW/W	B-Go FIFO <1>
B4	B-Go<1> Param. MSW	W	LW/W	B-Go FIFO <1>
B2	B-Go<0> Param. LSW	W	LW/W	B-Go FIFO <0>
B0	B-Go<0> Param. MSW	W	LW/W	B-Go FIFO <0>
AE	B-Go<3> SW-Go	W	W	data-less function
AC	Inh<3> Duration	R/W	W 8	DATA<7..0>
AA	Inh<3> Delay	R/W	W 12	DATA<11..0>
A8	B-Go<3> Mode	R/W	W 4	DATA<3..0> see bit map
A6	B-Go<2> SW-Go	W	W -	data-less function
A4	Inh<2> Duration	R/W	W 8	DATA<7..0>
A2	Inh<2> Delay	R/W	W 12	DATA<11..0>
A0	B-Go<2> Mode	R/W	W 4	DATA<3..0> see bit map
9E	B-Go<1> SW-Go	W	W -	data-less function
9C	Inh<1> Duration	R/W	W 8	DATA<7..0>
9A	Inh<1> Delay	R/W	W 12	DATA<11..0>
98	B-Go<1> Mode	R/W	W 4	DATA<3..0> see bit map
96	B-Go<0> SW-Go	W	W -	data-less function
94	Inh<0> Duration	R/W	W 8	DATA<7..0>
92	Inh<0> Delay	R/W	W 12	DATA<11..0>
90	B-Go<0> Mode	R/W	W 4	DATA<3..0> see bit map
8E				
8C				
8A	Event-Count LSW	R/W	W 16	
88	Event-Count MSW	R/W	W 8	
86	SW-L1A	W	W -	data-less function
84	SW-RST	W	W -	data-less function
82	CSR2	R/W	W 16	see bit map
80	CSR1	R/W	W 16	see bit map
00	Configuration EEPROM	R/(W)	W 8	LSBytes in every Long Word. See specs.

TTCvi Front Panel

Front Panel Coaxial signals

The following signals are available on the front panel:

Name	Description	Standard
L1A IN 0/ecl	L1A input from CTP	ECL active low
L1A IN 1/nim	User L1A Input	NIM
L1A IN 2/nim	User L1A Input	NIM
L1A IN 3/nim	User L1A Input	NIM
TRIGGER OUT/nim 0	Selected L1A Output	NIM
TRIGGER OUT/nim 1	Selected L1A Output	NIM
CLOCK IN bc/ecl	Input clock / Bunch Crossings	ECL
spare i/o	Configurable spare i/o	NIM
CLOCK OUT/nim direct	Selected Clock Output	NIM
CLOCK OUT/nim delayed	Delayed Selected Clock Output	NIM
ORBIT in/ecl	Orbit Input	ECL
ORBIT out/nim	Selected Orbit Output	NIM
B-Go IN/nim 0	B-Go 0 Input	NIM
B-Go IN/nim 1	B-Go 1 Input	NIM
B-Go IN/nim 2	B-Go 2 Input	NIM
B-Go IN/nim 3	B-Go 3 Input	NIM
INHIBIT OUT/nim 0	Inhibit 0 Output	NIM
INHIBIT OUT/nim 1	Inhibit 1 Output	NIM
INHIBIT OUT/nim 2	Inhibit 2 Output	NIM
INHIBIT OUT/nim 3	Inhibit 3 Output	NIM
CHANNEL OUT A/ecl	A-Channel Output	ECL active high
CHANNEL OUT B/ecl	B-Channel Output	ECL active high

Trigger Type Connector Pin-Out

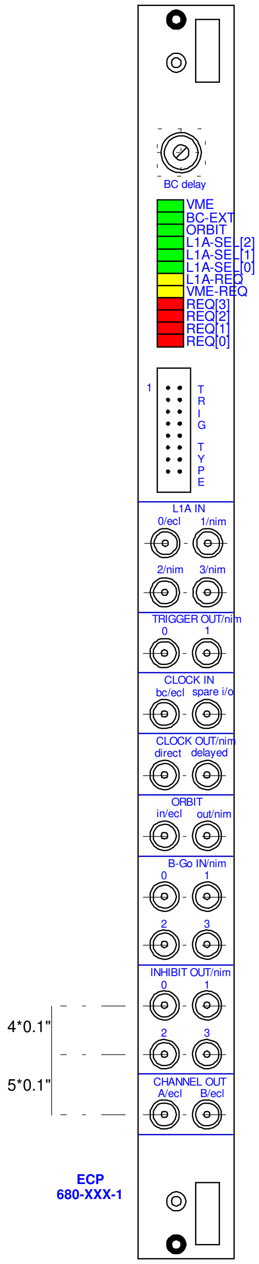
This male connector have 2 x 8 pins mounted with the pin 1 at the top left corner. A mating female plug would be 3M/3452-6600 (SCEM 09.55.03.316.4). The signal levels are of differential ECL type, where the odd pins are true high and even pins true low. Each signal pair is terminated with a 120 Ω resistor.

SIGNAL	PIN	PIN	SIGNAL
D<0> positive	1	2	D<0> negative
D<1> positive	3	4	D<1> negative
D<2> positive	5	6	D<2> negative
D<3> positive	7	8	D<3> negative
D<4> positive	9	10	D<4> negative
D<5> positive	11	12	D<5> negative
D<6> positive	13	14	D<6> negative
D<7> positive	15	16	D<7> negative

Front Panel Indicators

LED	Colour	Show Function
VME	green	Successful VME access
BC-EXT	green	External clock connected and running
ORBIT	green	External Orbit input selected
L1A-SEL(2)	green	L1A trigger source selection
L1A-SEL(1)	green	*L1A<0> if 0, L1A<1> if 1, L1A<2> if 2,*
L1A-SEL(0)	green	*L1A<3> if 3, VME function if 4, Random if 5*
L1A-REQ	yellow	request to send Event Count & Trigger Type
VME-REQ	yellow	request to send long or short asynchronous cycle
REQ(3)	red	request to send B-Go<3> associated cycle
REQ(2)	red	request to send B-Go<2> associated cycle
REQ(1)	red	request to send B-Go<1> associated cycle
REQ(0)	red	request to send B-Go<0> associated cycle

Front Panel Lay-out

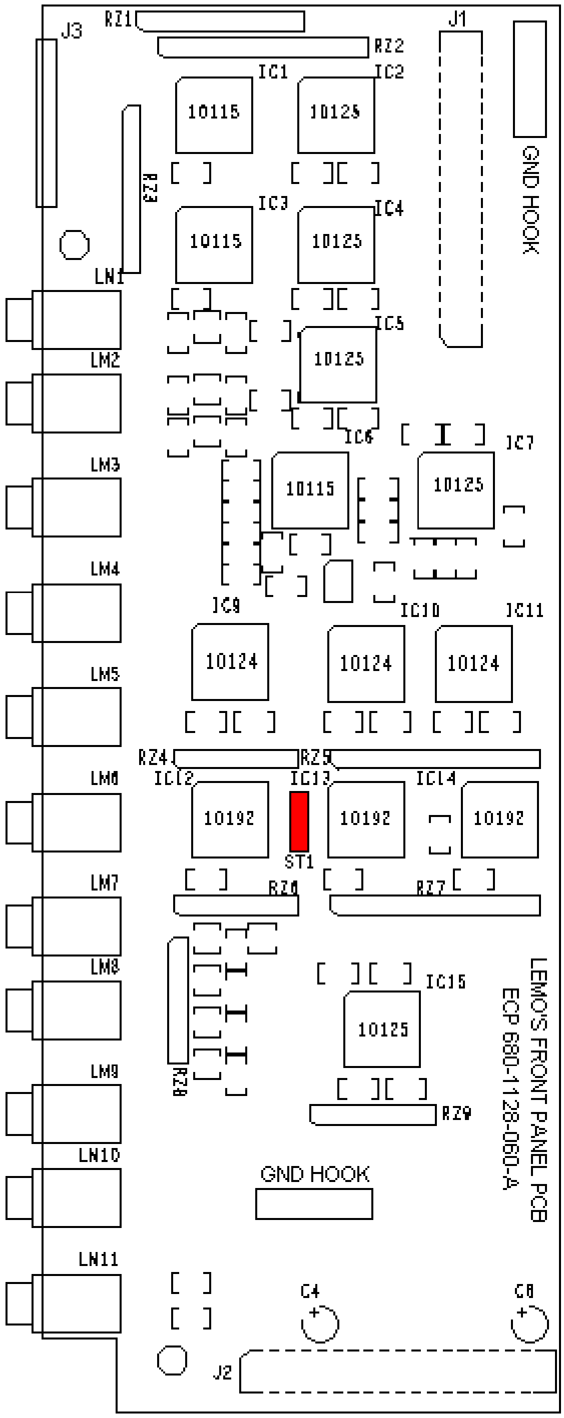


Module Power Requirements

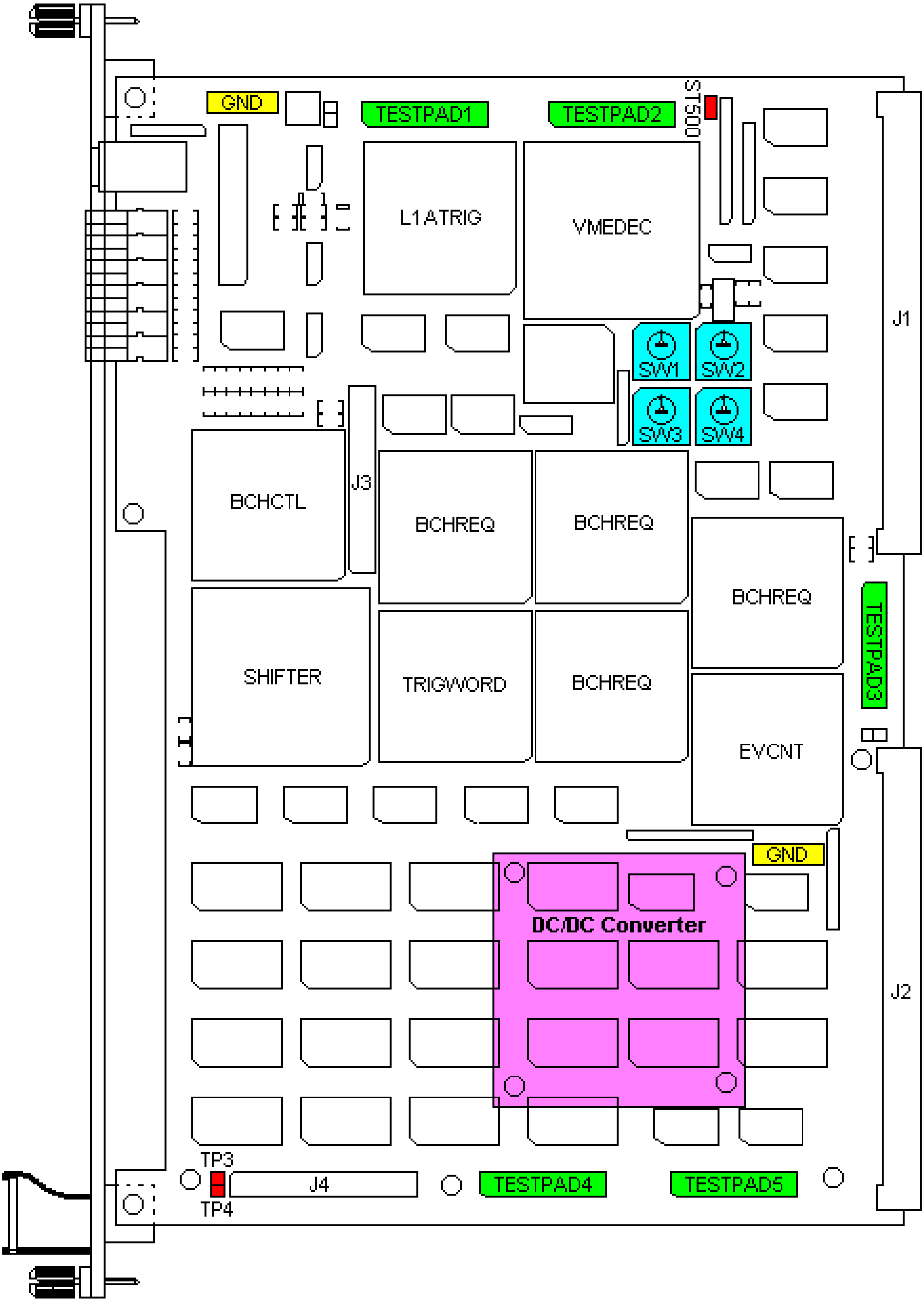
This module requires only a +5 V supply, with a consumption of about 5 A. An on-board DC-DC converter supplies the necessary -5 V for the NIM and ECL logic.

Module Board Lay-out and Configuration

Daughter Board Lay-out



Mother Board Lay-out



Adjusting Module Base Address

This is done by setting the hexa-decimal switches SW[1..4]:

SW1:	VME Address bits <23..20>
SW2:	VME Address bits <19..16>
SW3:	VME Address bits <15..12>
SW4:	VME Address bits <11..08>

Modifying Module Identification/Revision EEPROM

In principle this is done once before shipping the module to the user. If however a modification is needed the following procedure should be respected:

1. Insert a mini-jumper across the strap ST500 on the mother board.
2. Write16 bit words, from address $26 to $4E where the byte D<7..0> should contain the desired information. See table on page 15
3. Consecutive write cycles to this EEPROM should be spaced > 5 ms apart, in order to respect the memory write access time.
4. Read back data and check.
5. Remove the mini-jumper.

Adjusting the clock delay

The phase between the TTC transmitter clock (**CLOCK IN bc/ecl**) and the outgoing A and B Channel Out, (with the exception; if the A channel is derived from the **L1A<0>** input), may be adjusted with the front panel **BC DELAY** switch. Each of the 15 positions (> 0) of the switch corresponds to an additional delay of 2 ns. The switch setting may be read by the VME from CSR1. (N.B. invert CSR1 data bits <8..11> for correct reading!)

TUNING PROCEDURE:

1. Connect the TTCvi **A/ecl** and **B/ecl CHANNEL OUT** outputs to the transmitter crate corresponding encoder inputs with the <u>same</u> lengths of cables.
2. Connect the transmitter clock generator output (ECL) to the TTCvi **CLOCK IN bc/ecl** input. Check that the TTCvi **BC_EXT** indicator is lit, if not check the clock generation in the transmitter crate.
3. Start a VME loop process sending L1A triggers from the TTCvi. This should light up the yellow TTCvi indicator: **L1A-REQ** and the **A/ecl** and **B/ecl CHANNEL OUT** outputs should now carry valid signals. (A: Trigger and B: Trigger Type and Event Count)
4. With an oscilloscope; look at the Channel A and B inputs of the transmitter encoder in respect to the transmitter clock output.
5. Adjust the TTCvi **BC DELAY** switch such as the transition edges of the A and B channel fall in the middle of any clock half cycle, i.e. ≅ 12.5 ns from a clock transition.

Use of the spare NIM front panel input/output

It is possible to use this spare *LEMO* socket to either getting external access to a TTCvi internal signal or having an external signal for internal control or monitoring purposes.

INPUT:

1. Put a mini-jumper in the lower position of strap ST1 on the daughter board.
2. On the mother board: connect a wire from the test point TP4 to the destination signal point. This could, for example, be the CSR1 spare bit 15, which will then become a status bit. (N.B. The VME side of the CSR1 needs also to be connected to D<15>)

OUTPUT:

1. Put a mini-jumper in the upper position of strap ST1 on the daughter board.
2. On the mother board: connect a wire from the test point TP3 to desired source signal. This could, for example, be the CSR1 spare bit 15, which will then become a control bit. (N.B. The VME side of the CSR1 needs also to be connected to D<15>)

Test Headers

There are five Test Headers (TESTPAD[1..5] mounted on the TTCvi mother board to be used for test and debugging purposes. The test headers fit the Hewlett Packard 100 kΩ Termination Adapter (part no. 01650-90920). A suitable Logic State Analyser is the HP 16500 series, for which a number of acquisition set-ups already exists.

TESTPAD 1

L1A, Event Number FIFO related signals.

SIGNAL-NAME	*PIN*	*POD*
NC	1	
NC	2	
BCD2	3	CLK
BCD2	4	D15
from tp2 (spare pin)	5	D14
from tp1 (spare pin)	6	D13
RDFIFO<3>	7	D12
RDFIFO<2>	8	D11
RDFIFO<1>	9	D10
RDFIFO<0>	10	D09
FIFO_L1A_EMPTY_L	11	D08
FIFO_EMPTY_L2	12	D07
FIFO_EMPTY_L1	13	D06
FIFO_EMPTY_L0	14	D05
WR_FIFO_L	15	D04
L1A_GRANT_L	16	D03
L1A_REQ_L	17	D02
L1A_OUT_L	18	D01
ORBIT_L	19	D00
GND	20	GND

TESTPAD 2

VME associated signals.

SIGNAL-NAME	*PIN*	*POD*
NC	1	
NC	2	
BCD2	3	CLK
BCD2	4	D15
STATEVAR_C	5	D14
STATEVAR_B	6	D13
STATEVAR_A	7	D12
WR_FIFO_L0	8	D11
VME_GRANT_L	9	D10
VME_PEND_L	10	D09
VME_LONGL_CLK_H	11	D08
VME_LONGH_CLK_H	12	D07
DTACK_L	13	D06
WRITE_L	14	D05
LONGWORD_L	15	D04
LOADR_L	16	D03
HIADR_L	17	D02
AS_L	18	D01
DS0_L	19	D00
GND	20	GND

TESTPAD 3

B-Go<0>, Inhibit<0>, B-channel related signals.

SIGNAL-NAME	*PIN*	*POD*
NC	1	
NC	2	
BCD3	3	CLK
BCD3	4	D15
from tp5 (spare pin)	5	D14
from tp6 (spare pin)	6	D13
B_GO_L<0>	7	D12
GRANT_L<0>	8	D11
BGO_REQ_L<1>	9	D10
BGO_REQ_L<0>	10	D09
INHIBIT_L<0>	11	D08
RESTRANSM_L<0>	12	D07
RD_FIFO_L<0>	13	D06
FIFO_EMPTY_L<0>	14	D05
SHIFT_L	15	D04
LOAD_L	16	D03
B_CHANNEL	17	D02
VME_LONG_OE_L	18	D01
L1A_GRANT_L	19	D00
GND	20	GND

TESTPAD 4

B-Channel Parallel Data Bus bits <31..16>

SIGNAL-NAME	PIN	POD
NC	1	
NC	2	
NC	3	CLK
B_CH DATA<16>	4	D15
B_CH DATA<17>	5	D14
B_CH DATA<18>	6	D13
B_CH DATA<19>	7	D12
B_CH DATA<20>	8	D11
B_CH DATA<21>	9	D10
B_CH DATA<22>	10	D09
B_CH DATA<23>	11	D08
B_CH DATA<24>	12	D07
B_CH DATA<25>	13	D06
B_CH DATA<26>	14	D05
B_CH DATA<27>	15	D04
B_CH DATA<28>	16	D03
B_CH DATA<29>	17	D02
B_CH DATA<30>	18	D01
B_CH DATA<31>	19	D00
GND	20	GND

TESTPAD 5

B-Channel Parallel Data Bus bits <15..0>

SIGNAL-NAME	PIN	POD
NC	1	
NC	2	
NC	3	CLK
B_CH DATA<0>	4	D15
B_CH DATA<1>	5	D14
B_CH DATA<2>	6	D13
B_CH DATA<3>	7	D12
B_CH DATA<4>	8	D11
B_CH DATA<5>	9	D10
B_CH DATA<6>	10	D09
B_CH DATA<7>	11	D08
B_CH DATA<8>	12	D07
B_CH DATA<9>	13	D06
B_CH DATA<10>	14	D05
B_CH DATA<11>	15	D04
B_CH DATA<12>	16	D03
B_CH DATA<13>	17	D02
B_CH DATA<14>	18	D01
B_CH DATA<15>	19	D00
GND	20	GND