TTCvx
Technical description and users manual.

A VME-sized multiplexer, encoder and fiber-optics transmitter module for the Timing, Trigger and Control Systems of the LHC detectors.

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Per G lln CERN/EP/ATE/dq
per.gallno@cern.ch
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SPECIFICATIONS

- Mechanical Standard

  Europe chassis 6U / 4TE with two 96 pin connectors (DIN 41612) connecting to the backplane

- VME Capabilities

  None. Only the power supply busses of the backplane are used

- Signal levels (coaxial 50 W connectors)

  Inputs and outputs are ECL levels. A/B channel inputs are DC-coupled, whereas clock in/outputs and encoder output are AC-coupled. Internal 50 W terminations on all inputs.

- Signal levels (differential outputs)

  LVDS (Low Voltage Differential Signaling standard)

- Fiber-Optics Connectors

  ST style

- Optical output wavelenght

  1330 nm

- Internal clock generator frequency

  40.00 MHz, 100 ppm

- External clock generator frequency range

  25 - 50 MHz

- Power consumption

  1.6 A @ +5V
  75 mA @ -12V

GENERAL DESCRIPTION

INTRODUCTION

The Trigger, Timing and Control System (TTC) of the LHC experiments comprises the following components:

- The VMEbus interface, TTCvi
- The Laser Transmitter Crate or the Mini-Crate
- The timing receiver ASIC, TTCrx
- System specific modules carrying the TTCrx chip

A VME-size module, TTCvx, featuring the main functions of the Mini-Crate have been designed. The TTCvx is foreseen to be an alternative to be used in TTC test and evaluation systems, where a compact and economical solution is desired.

BASIC OPERATION

TTC

The TTC system distributes the timing signal (BC) from the LHC machine together with trigger and control information (L1A, BCR, ECR etc.) from the Central Trigger Processor to the sub-detector Read-Out Buffers and Front End systems.

The two communications channels: A, carrying the L1A trigger, and B, carrying the control address/data or command packets, are generated by the TTCvi module.

The A and B channels are time division multiplexed (TDM) and bi-phase mark encoded before fed to the optical transmitter, which in turn drives the fiber distribution network. These functions are performed by either the Laser Transmitter Crate, the Mini-Crate or the TTCvx module.

The TTCrx ASIC converts the signal from the photo-detector into user information (address/data/strobes, Clock signals, L1A, BCR,...) available on the output busses of the chip. The TTCrx have other functions as: clock recovery, de-skewing, bunch/event counting, generating resets etc.

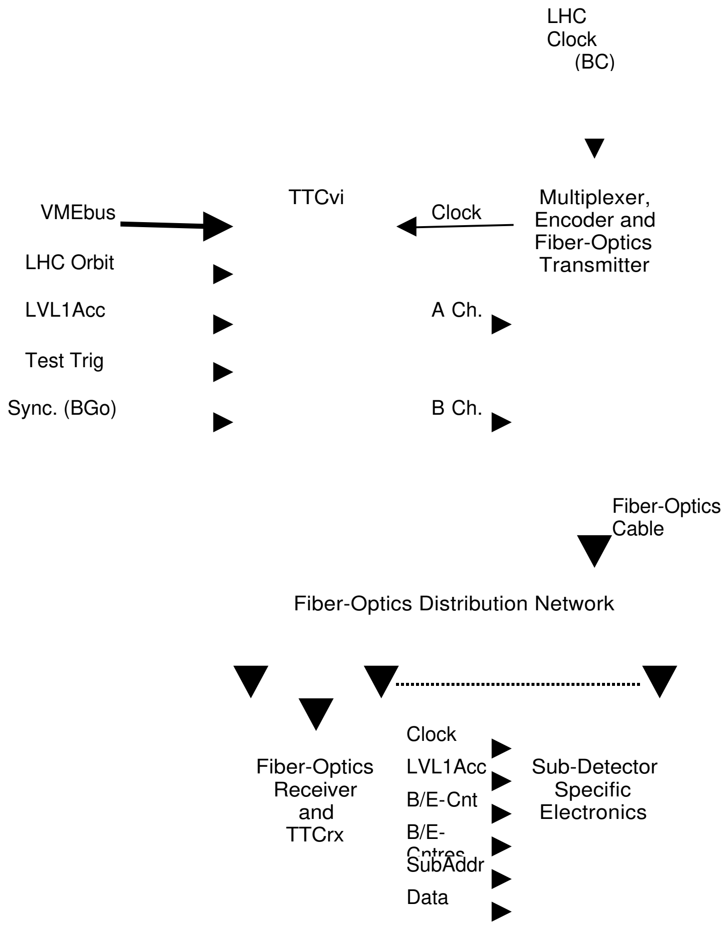


Figure 1. The TTC System

TTCvx

The TTCvx module function is, as described above, to multiplex and encode the A and B channels generated by the TTCvi. The TTCvx has an internal clock, as well as an input for an external one. The switching between the two clock sources is automatic by the means of an external clock detection circuit. The, for the encoding, necessary clock multiplication is handled by a phase locked loop (PLL) frequency synthesizer circuit. The basic clock frequency from the PLL is available on the module front panel in both LVDS and ECL levels and is used for synchronization with the TTCvi. Up to four light emitting devices can be fitted to drive fiber optic cables. The encoded signal is also available on the front panel in both ECL and LVDS levels.

DESIGN DESCRIPTION

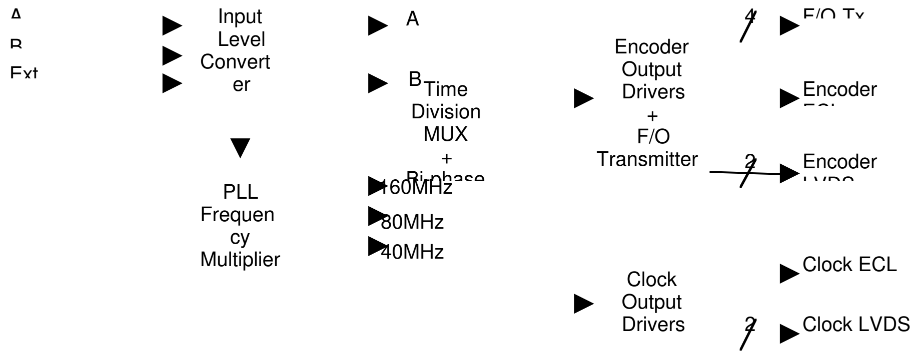


Figure 2. The TTCvx Block Diagram

The TTCvx design can be divided into blocks namely:

- Input signal level converter and clock selection/generation
- PLL frequency multiplier
- Time division multiplexer and bi-phase mark encoder
- Encoder output drivers
- Clock output drivers
- Supply voltage regulators

The function of each block will be described briefly:

Input signal level converter and clock selection/generation

The A and B inputs are DC-coupled and terminated by Thevenin networks, having a resulting impedance of 50 W. The External Clock input is AC-coupled and then terminated by 50 W. All inputs are biased to ECL "0" level when no input signal is applied. The ECL input signals are in this block shifted to PECL levels as all the remaining logic is designed using PECL technology.

An 80.00 MHz quartz ECL oscillator, which output is divided by two, acts as the internal clock generator. A simple diode detector circuit senses when an external frequency source is connected and causes the clock selector to switch over to external clock. A LED is lit when an external clock signal is present.

PLL frequency multiplier

A PLL Clock synthesizer circuit is used to generate the different clock multiples (*1, *2 and *4) required by the TDM and encoder circuits. The PLL operation range can be selected and is, in the TTCvx, preset to operate in the 25 - 50 MHz range. A reset button is implemented in the case the PLL circuit should fails to lock to the input frequency.

Time division multiplexer and bi-phase mark encoder

A 2:1 multiplexer selects the A and B channels in turn at the rate of the basic clock frequency. The resulting time division multiplexed signal feeds the bi-phase mark encoder, which in turn produces an output according to *Figure 3*.

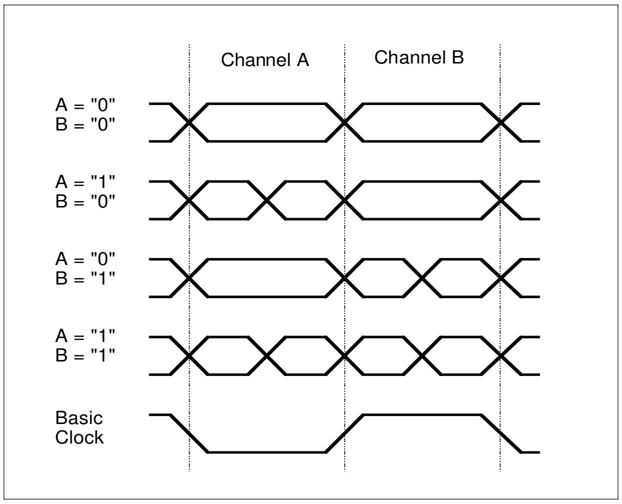


Figure 3. Encoder Output Wave forms

Encoder output drivers

The encoded signal is available on the module front panel as one AC-coupled ECL output, two LVDS outputs and four fiber optics transmitter outputs.

Clock output drivers

The PLL basic frequency (40 MHz) is available on the module front panel as two AC-coupled ECL outputs and two LVDS outputs.

Supply voltage regulators and backplane connections

All ECL integrated circuits are referenced to the +5 V (VCC) rail (PECL). The PLL circuit has a maximum supply voltage of 3.3 V between VCC and GND, hence a 1.7 V current sinking regulator is implemented. Another voltage regulator is used to supply the -5 V for the ECL/PECL level shifter chip from the -12 V rail.

No VMEbus protocol related signals are used by the TTCvx module. Daisy-chained signals as IACK in/out and BGO in/out are bypassed in the module.

REFERENCE LITERATURE

- All relevant TTC information may be found at the URL: *http://www.cern.ch/TTC/intro.html*
- Motorola Application Note: Designing with PECL (AN1406)
- National Application Note: An Overview of LVDS Technology (AN971)

USER'S GUIDE

FRONT PANEL FUNCTIONS

The front panel lay-out can be seen in *Figure 4*

Channel A/B In

ECL level inputs to connect the A and B channel from the TTCvi module. These inputs are DC-coupled and internally terminated with 50 W. Both inputs are biased to an ECL "0" level when not connected.

Clock In

Input for connecting an external ECL level clock source. The commutation is automatic and the indicator lights up when an external clock signal is present. This input is AC-coupled and internally terminated with 50 W. The practical input frequency range corresponds well with the selected PLL locking range, actually set to 25 - 50 MHz.

Clock Out

Two AC-coupled ECL level outputs and two LVDS clock outputs used for synchronization of external equipment, i.e. the TTCvi (ECL). These outputs carry the basic frequency of the PLL circuit.

Encoder Out

One AC-coupled ECL level output and two LVDS outputs carrying the signal generated by the encoder. The LVDS signal can be used for connecting to the TTCrx end in systems without optical transmission.

Fiber Optics Out

Four fiber optics transmitters of LED type (1330 nm). The standard TTCvx version is delivered with two transmitters. On special request (and to a higher price) all four transmitters can be fitted.

PLL Reset

Push button to reset the PLL circuit if phase locking is lost.

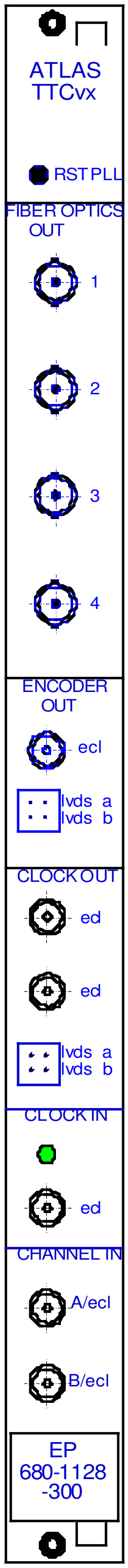


Figure 4. TTCvx Front Panel

INSTALLATION PROCEDURE

IMPORTANT WARNINGS

1. *The VME crate must be powered down before inserting or extracting the TTCvx module.*
2. *The module must be thoroughly pushed into the VME crate and secured with the top and bottom fixing screws, in order to assure proper operation.*
3. *Optical fiber and emitter connectors should be handled and cleaned according to prescribed procedures.*
4. *Some components on the TTCvx board are sensitive to electro-static discharges. To avoid damage, minimize handling and take appropriate precautions against static discharges.*
5. *Any modification to the pre-set adjustments of the module must only be carried out by a specialist in a laboratory environment.*

PLL operation mode verification

The solder straps ST2 to ST9 should be bridged according to following table in order to insure stable operation in the 25 - 50 MHz range. The lay-out of the TTCvx board can be seen in *Figure 5*.

FS0	FS1	FS2	VCO	FE0	FE1	FE2	FE3
fselFB-0	fselFB-1	fselFB-2	VCO-sel	fsel-0	fsel-1	fsel-2	fsel-3
done	done	open	done	open	done	done	open

Clock selection

An external clock source with ECL levels should be connected to the Clock In input if a different frequency is desired as the one generated by the internal oscillator (40.00 MHz).

TTCvx/TTCvi interconnecting cables

The following cables need to be connected in order to operate the TTCvi/TTCvx module pair:

- A 0.5 ns cable between the TTCvi: CHANNEL OUT A/ecl and the TTCvx: CHANNEL IN A/ecl
- A 0.5 ns cable between the TTCvi: CHANNEL OUT B/ecl and the TTCvx: CHANNEL IN B/ecl
- A 0.5 ns cable between the TTCvi: CLOCK IN bc/ecl and the TTCvx: CLOCK OUT ecl (top)

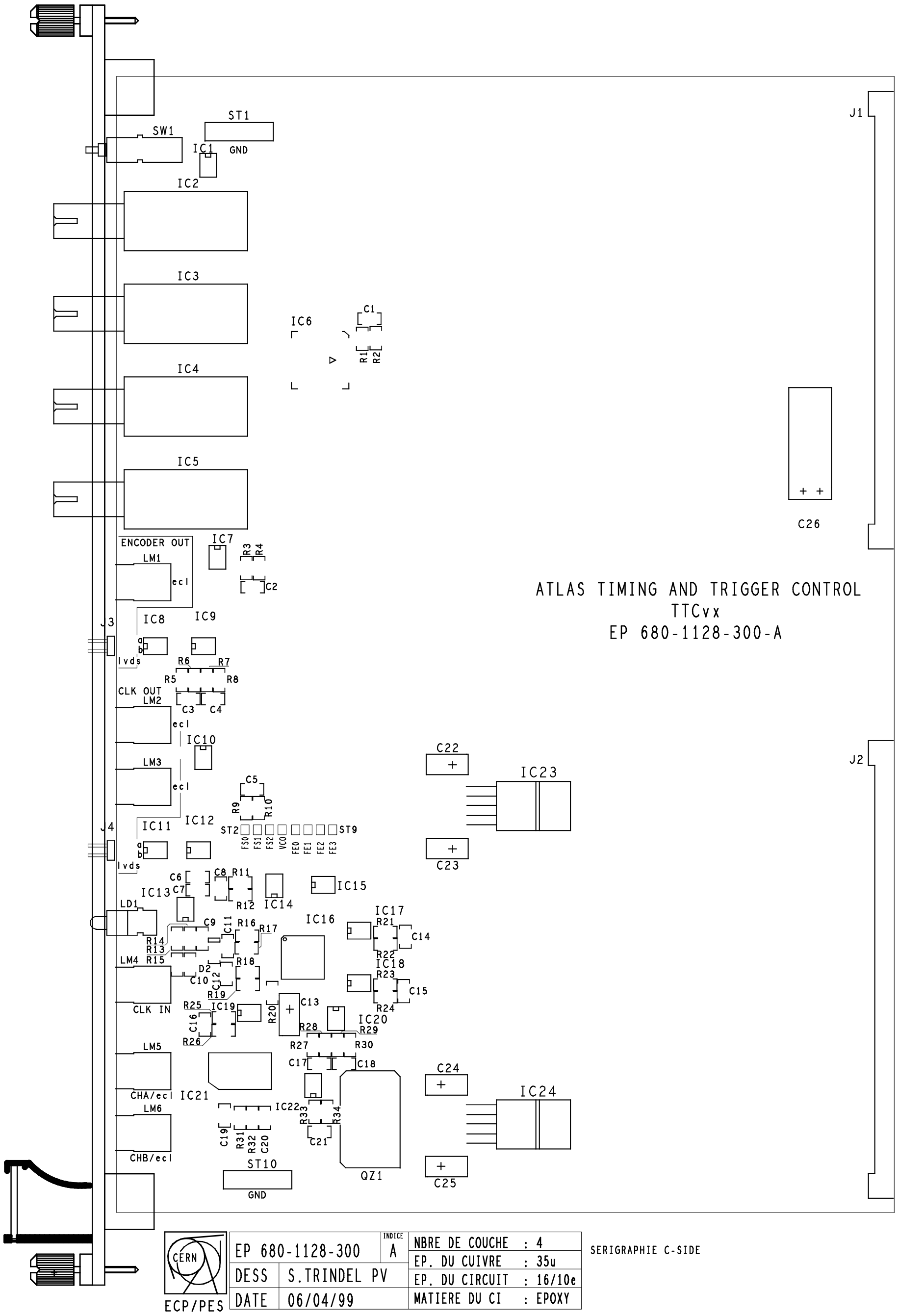


Figure 5. TTCvx Board Lay-Out

TEST PROCEDURES

In order to test the basic functions of the TTCvx one needs the following additional equipment:

- A relatively fast oscilloscope (BW ‡ 500 MHz)
- A TTCvi module

Setting up the test bench for static inputs

The A and B channel inputs of the TTCvx may be connected in different ways to the inactive A and B channel outputs of the TTCvi. The A output carries an ECL "0" and the B output a "1". The TTVx channel A/B inputs take the value of "0" when not connected. The ECL Encoder Out of the TTCvx should show the following waveforms in relation to the TTXvx Clock Out. The oscilloscope should be set to trigger on the rising edge of the clock signal.

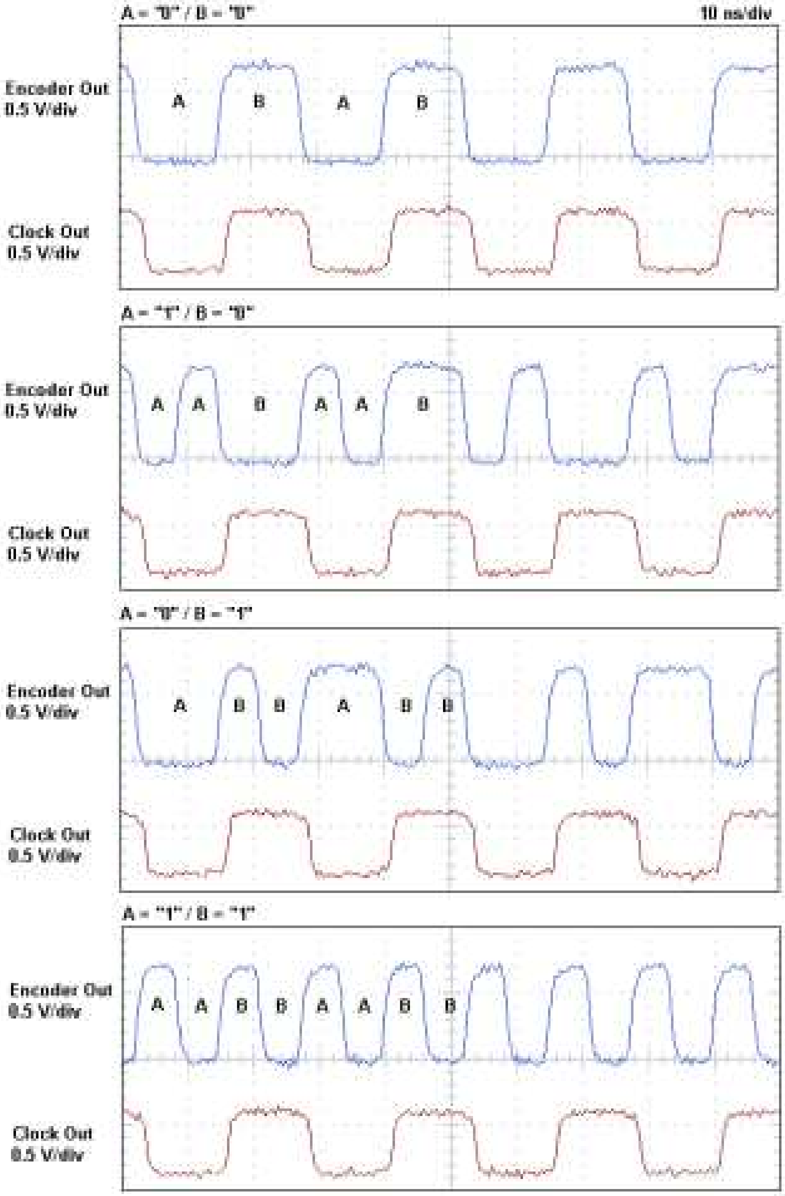


Figure 6. Encoder Output Wave forms

TTCvx latency verification

The L1A latency may be verified by having the TTCvi running in the random trigger mode and then measure the time between the TTCvi/TRIGGER OUT/nim/0 and the TTCvx/ENCODER-OUT/ecl. The oscilloscope should be set to trigger on the falling edge of the trigger pulse. N.B. The Trigger/nim output is active low, whereas the A channel output is active high.

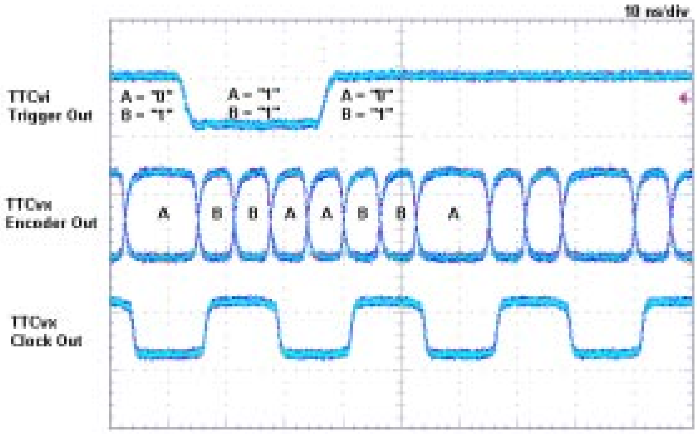


Figure 7. TTCvx L1A latency measurement

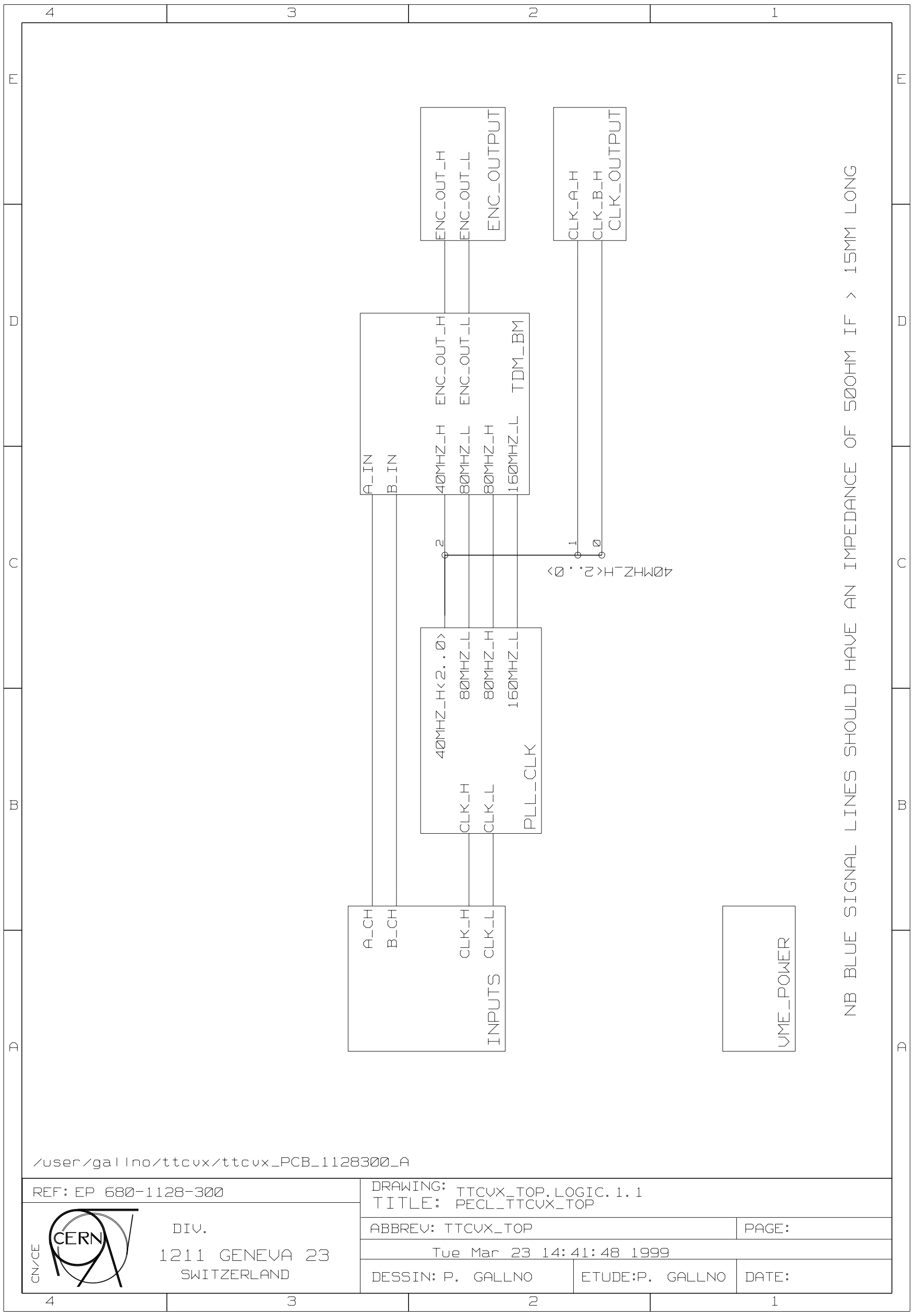
HARDWARE MANUAL

PARTS LIST

PART	TYPE, VALUE, TOLERANCE	SCEM	Qty	REFERENCE
Diode	Silicon HP 5082-2900	08.51.11.760.3	1	D2
Diode LED	Yellow MENTOR 8033	07.88.10.730.8	1	LD1
Fiber Optic Transmitter	LED 1330 nm 200Mb/s AMP 269049		2	IC2-IC5
Integrated Circuit	ECLinPS 100EL90		1	IC21
Integrated Circuit	ECLinPS Lite 10E111	08.57.18.111.6	1	IC6
Integrated Circuit	ECLinPS Lite 10EL04	08.57.21.004.1	1	IC17
Integrated Circuit	ECLinPS Lite 10EL12	08.57.21.012.1	3	IC7,IC10,IC14
Integrated Circuit	ECLinPS Lite 10EL31	08.57.21.031.8	3	IC1,IC18,IC22
Integrated Circuit	ECLinPS Lite 10EL35	08.57.21.035.4	1	IC15
Integrated Circuit	ECLinPS Lite 10EL58	08.57.21.058.7	2	IC19,IC20
Integrated Circuit	ECLinPS Lite 10ELT21		3	IC9,IC12,IC13
Integrated Circuit	DS90C401 (LVDS driver)		2	IC8,IC11
Integrated Circuit	LM2991 TO220 Neg. Voltage Regulator		2	IC23,IC24
Integrated Circuit	MPC991 PLL Clock Driver		1	IC16
Integrated Circuit	Quartz Oscillator 80MHz ECL		1	QZ1
Capacitor	Ceramic Class 2, SMD 1206 100nF/50V	10.03.04.500.2	85	Decoupling
Capacitor	Ceramic Class 2, SMD 1206 22nF/50V	10.03.04.422.9	1	C9
Capacitor	Tantalum axial, 200uF/10V	10.81.01.240.1	1	C26
Capacitor	Tantalum SMD, 15uF/25V		1	C24
Capacitor	Tantalum SMD, 22uF/16V	10.82.01.380.4	4	C13,C22,C23,C25
Resistor	Metal film 1/4W, SMD 1206, 10ohm, 1%	11.24.05.110.0	1	R20
Resistor	Metal film 1/4W, SMD 1206, 56ohm, 1%	11.24.05.156.6	2	R70,R73
Resistor	Metal film 1/4W, SMD 1206, 62ohm, 1%	11.24.05.162.8	1	R32
Resistor	Metal film 1/4W, SMD 1206, 82ohm, 1%	11.24.05.182.4	41	Terminations
Resistor	Metal film 1/4W, SMD 1206, 120ohm, 1%	11.24.05.212.5	41	Terminations
Resistor	Metal film 1/4W, SMD 1206, 130ohm, 1%	11.24.05.213.4	1	R71
Resistor	Metal film 1/4W, SMD 1206, 240ohm, 1%	11.24.05.224.1	4	R31,R69,R96,R98
Resistor	Metal film 1/4W, SMD 1206, 390ohm, 1%	11.24.05.239.4	1	R72,R97
Resistor	Metal film 1/4W, SMD 1206, 750ohm, 1%	11.24.05.275.0	1	R36,R99
Resistor	Metal film 1/4W, SMD 1206, 2,2kohm, 1%	11.24.05.322.0	2	R14,R15
Resistor	Metal film 1/4W, SMD 1206, 3,3kohm, 1%	11.24.05.333.7	2	R13,R35
Switch	MENTOR 1840.6131 Push-Button	07.88.10.300.6	1	SW1
Jumper	JUMPER-1016 (for scope probe GND clip)	07.88.24.516.1	2	ST1,ST10
Connector	2mm 2x2 male for LVDS		2	J3,J4
Connector	Europa DIN41612 VME 3X32 male	09.61.33.315.7	2	J1,J2
Connector	Coaxial LEMO #00 90 degr	09.46.11.180.6	6	LM1-LM6
Front Panel Hardware	VME 6U/4TE	06.61.64.704.3	1	
Screws	M3x6 cheese head	47.62.32.306.6	2	
Screws	M2.5x10 cheese head	47.62.32.257.8	4	
Nuts	M3	47.44.77.330.8	2	
Nuts	M2.5	47.44.77.325.5	4	

CIRCUIT DIAGRAMS

The circuit diagrams are presented in a hierarchical fashion, with an explanatory block diagram at the top level followed by the detailed design drawings or sub-blocks.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CLK_B_H
CLK_OUTPUT
A_IN
B_IN
40MHZ_H
80MHZ_L
80MHZ_H
160MHZ_L
ENC_OUT_H
ENC_OUT_L
TDM_BM
40MHZ_H<2..0>
40MHZ_H<2..0>
80MHZ_L
80MHZ_H
160MHZ_L
CLK_H
CLK_L
PLL_CLK
A_CH
B_CH
CLK_H
CLK_L
INPUTS
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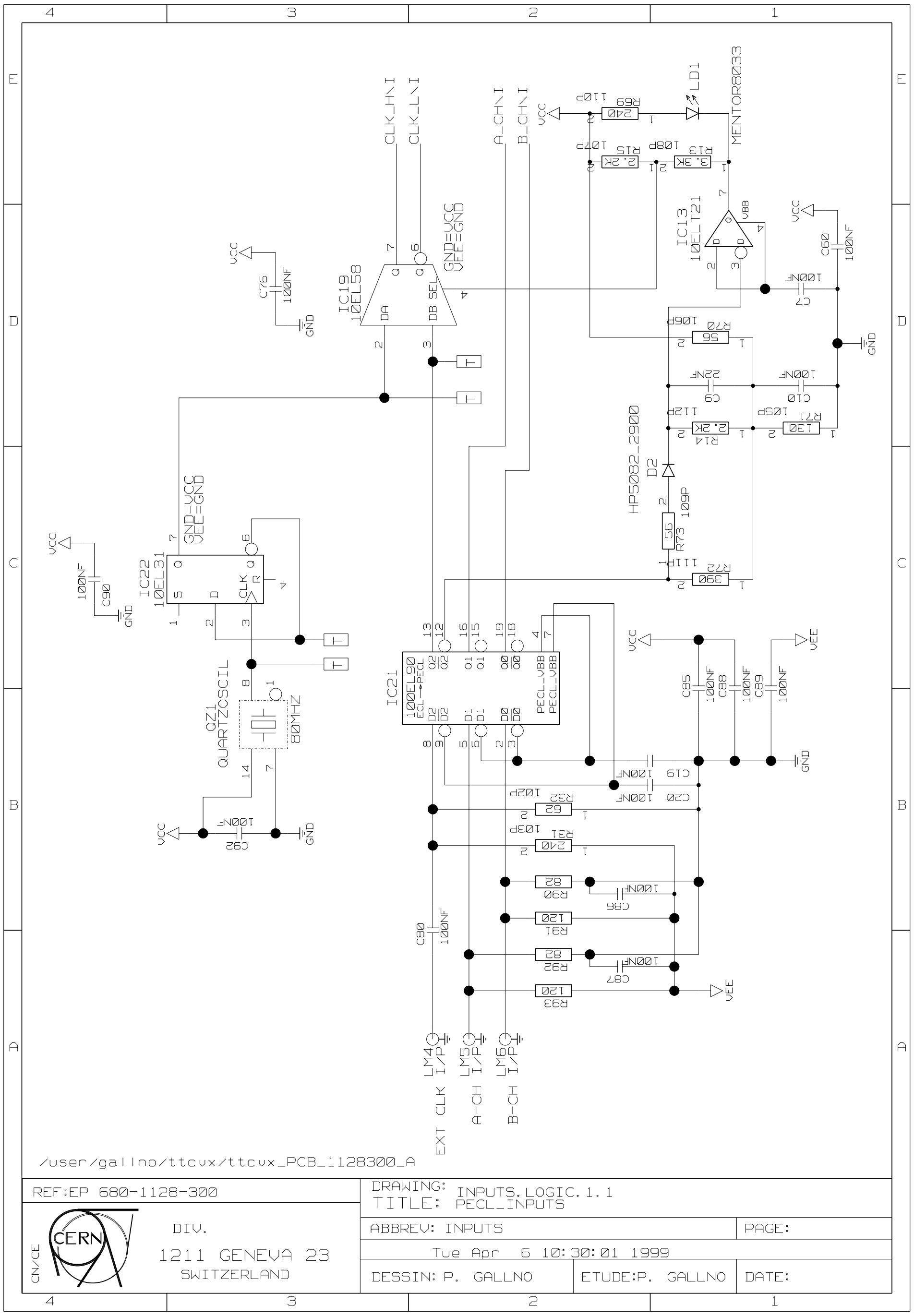
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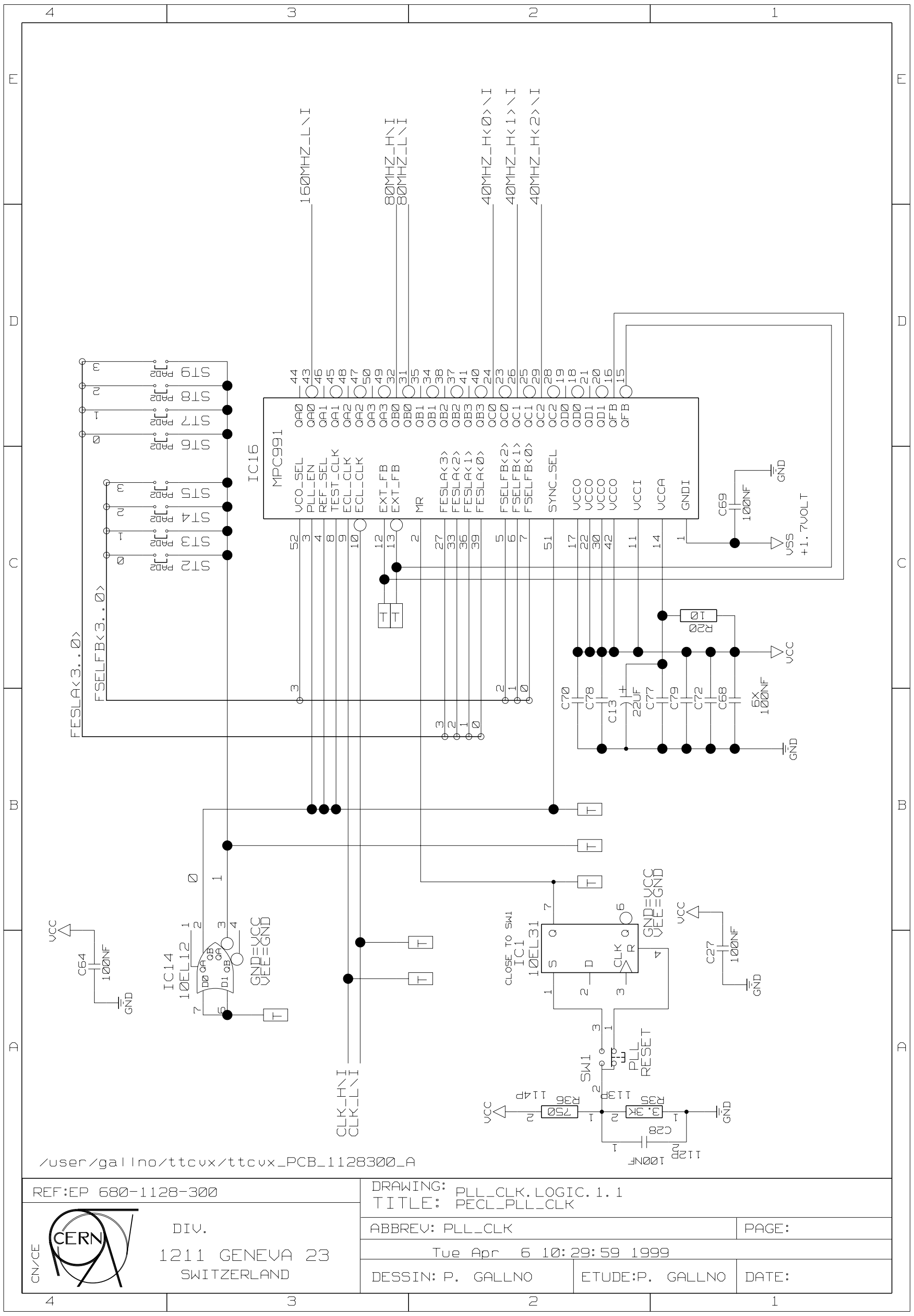
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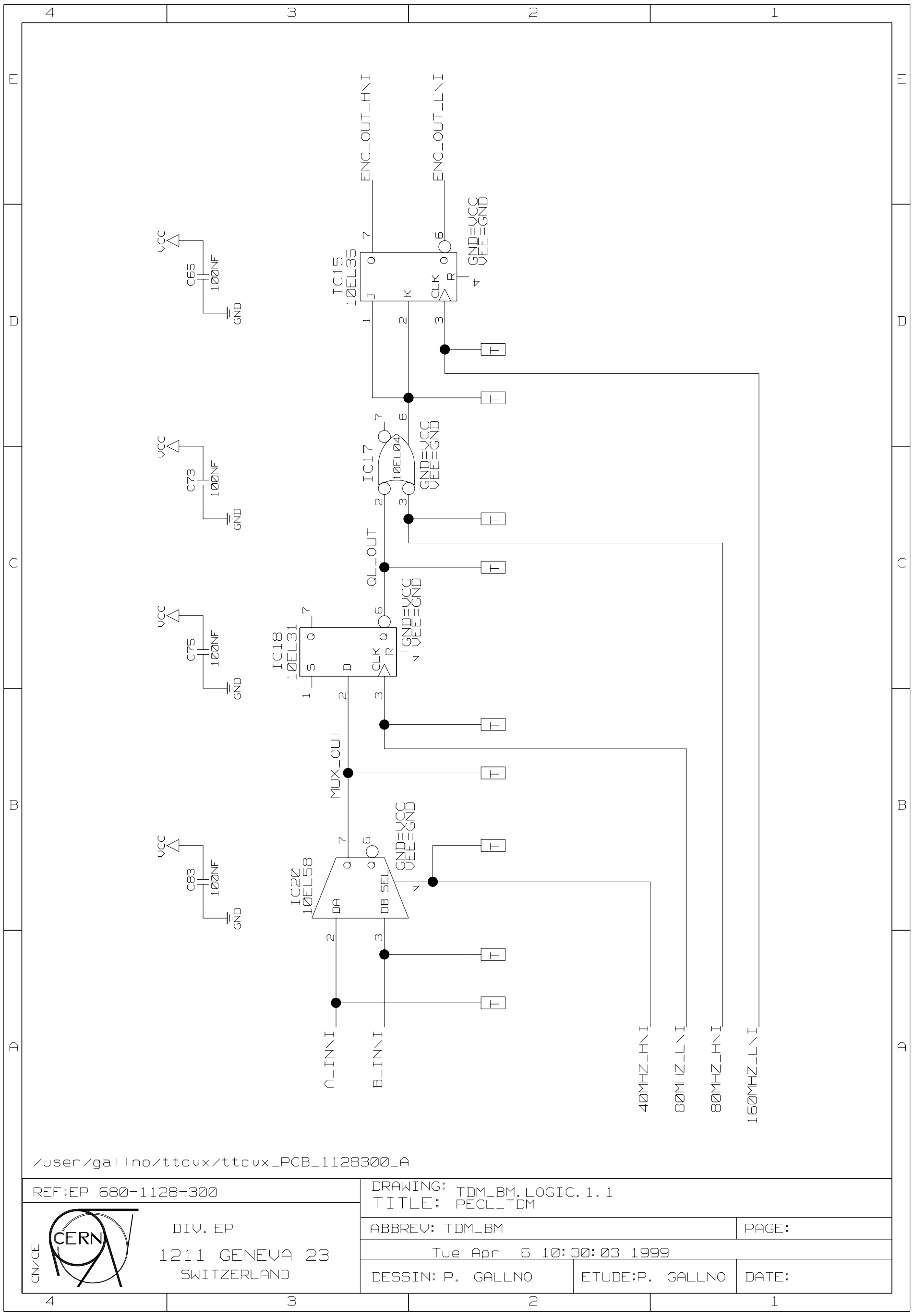
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ENC_OUT_L\I
IC15
10EL35
IC17
10EL04
IC18
10EL31
IC20
10EL58
QL_OUT
MUX_OUT
GND=VCC
VEE=GND
C65
C73
C75
C83
100NF
VCC
GND
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B_IN\I
40MHZ_H\I
80MHZ_L\I
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160MHZ_L\I
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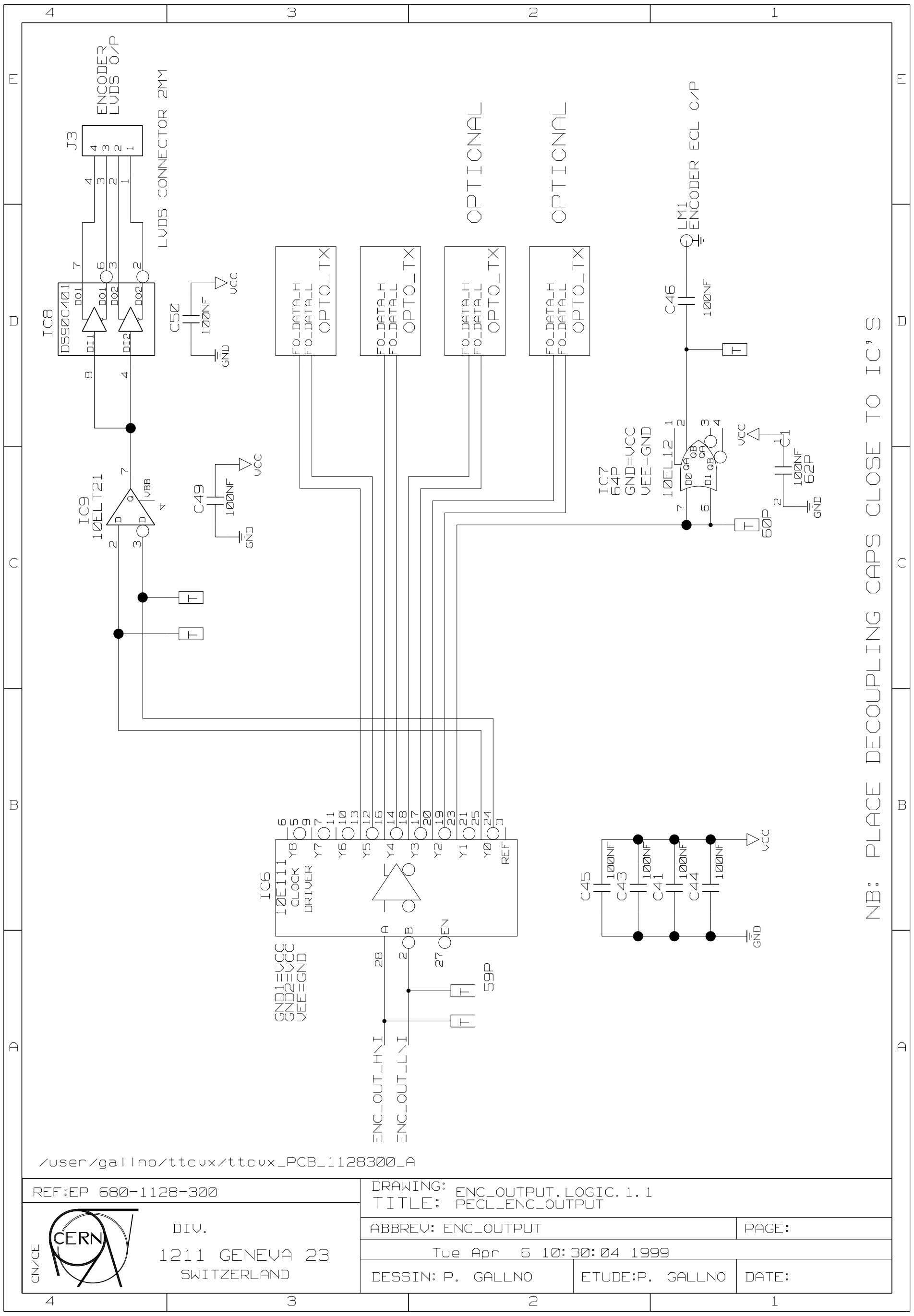
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IC8
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OPTIONAL
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FO_DATA_L
OPTO_TX
LM1
ENCODER ECL O/P
C46
100NF
IC7
64P
GND=VCC
VEE=GND
10EL12_1
C1
100NF
62P
60P
IC9
10ELT21
C49
100NF
NB: PLACE DECOUPLING CAPS CLOSE TO IC'S
IC6
10E111
CLOCK
DRIVER
GND1=VCC
GND2=VCC
VEE=GND
59P
ENC_OUT_H_I
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C43
C41
C44
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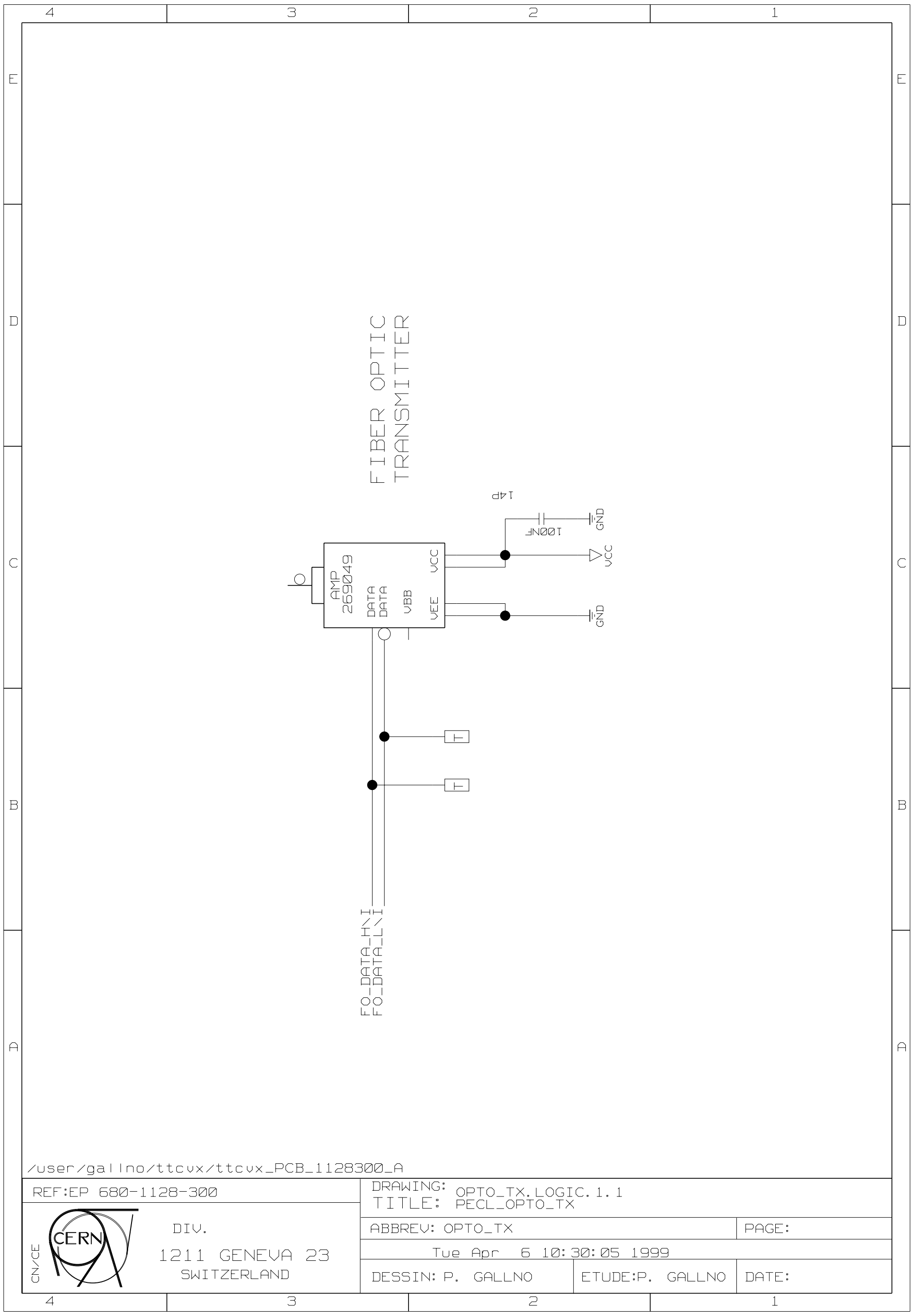
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AMP
269049
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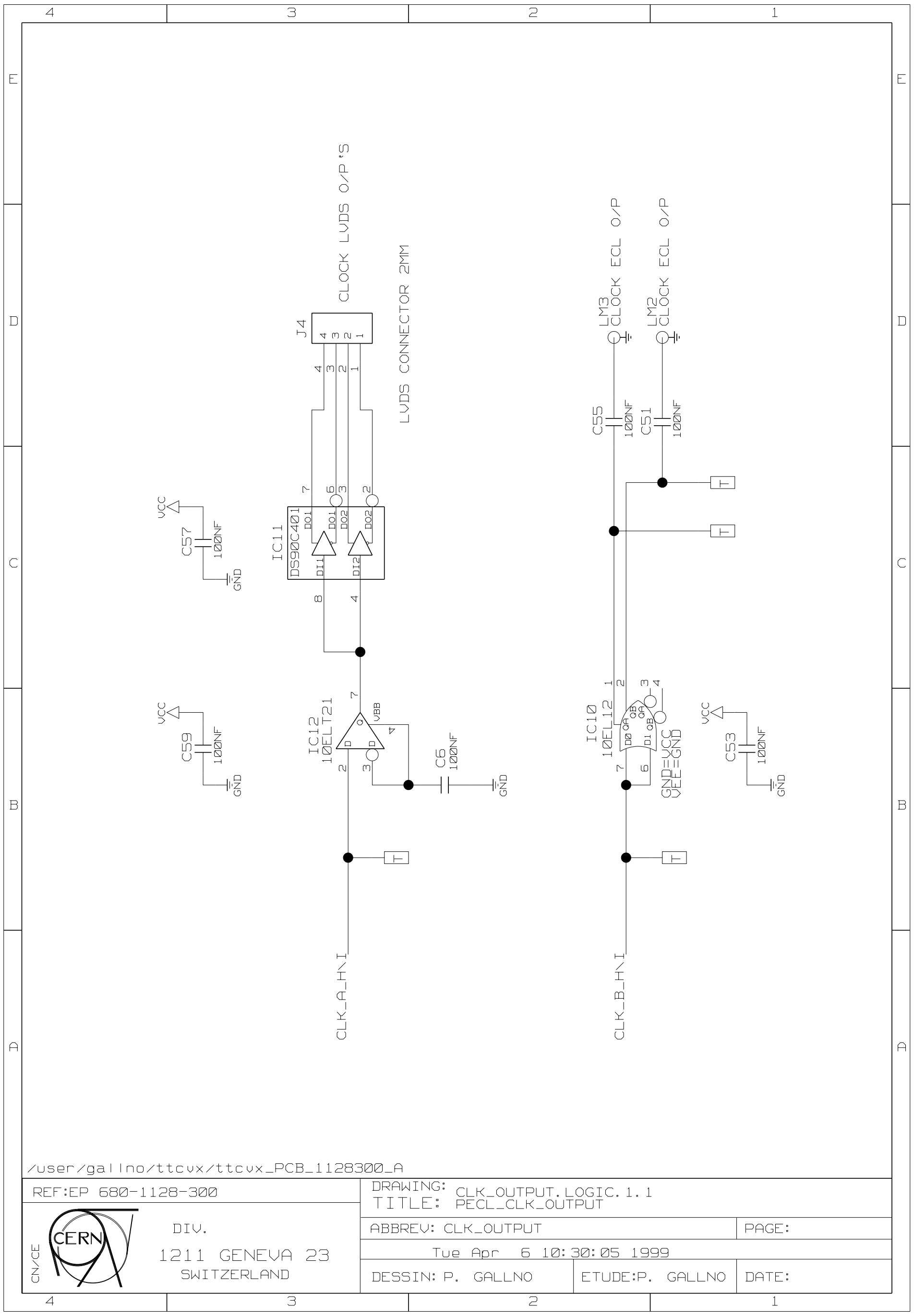
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100NF
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100NF
C59
100NF
VCC
GND
CLK_A_H\I
CLOCK ECL O/P
LM3
LM2
C55
100NF
C51
100NF
IC10
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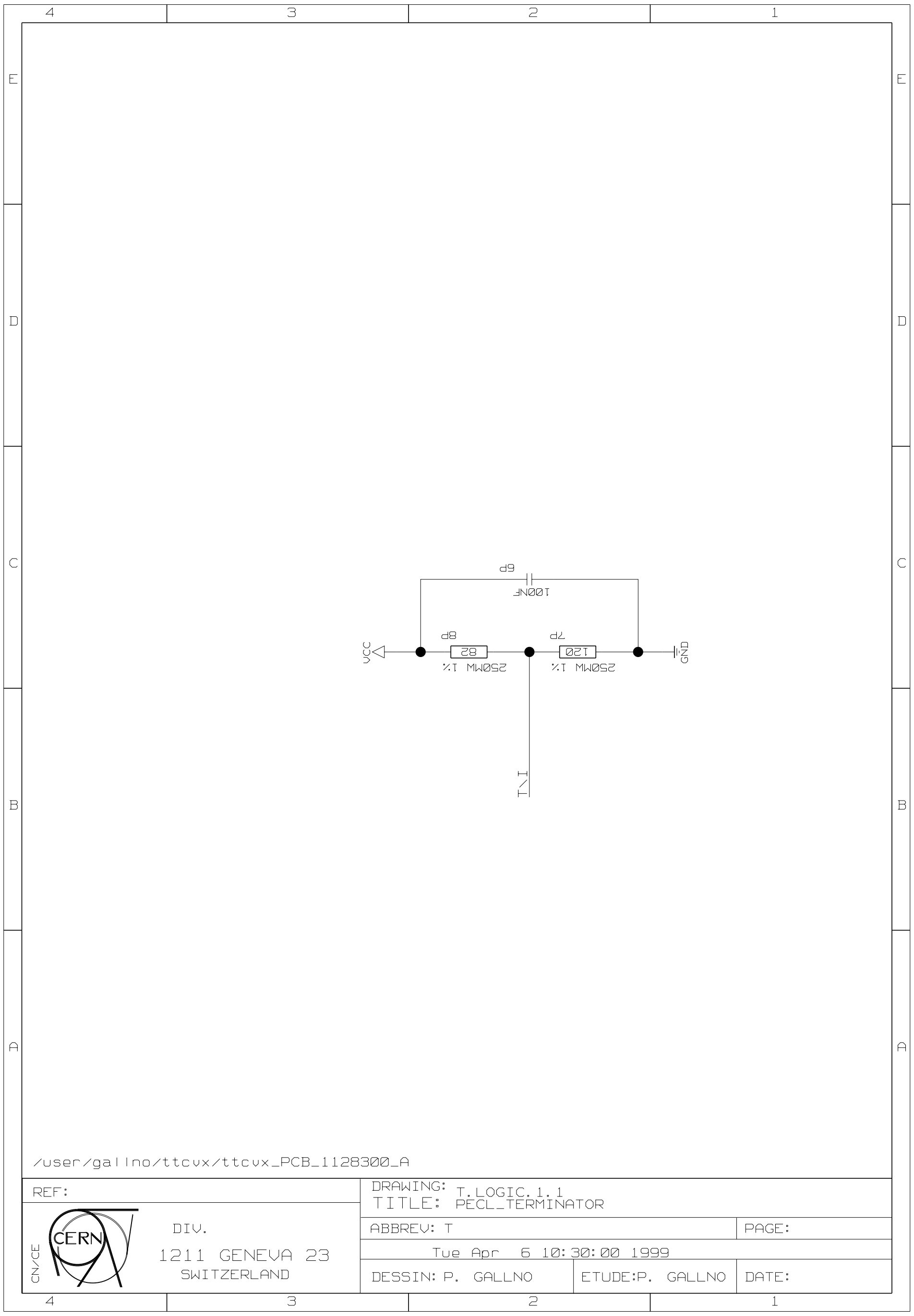
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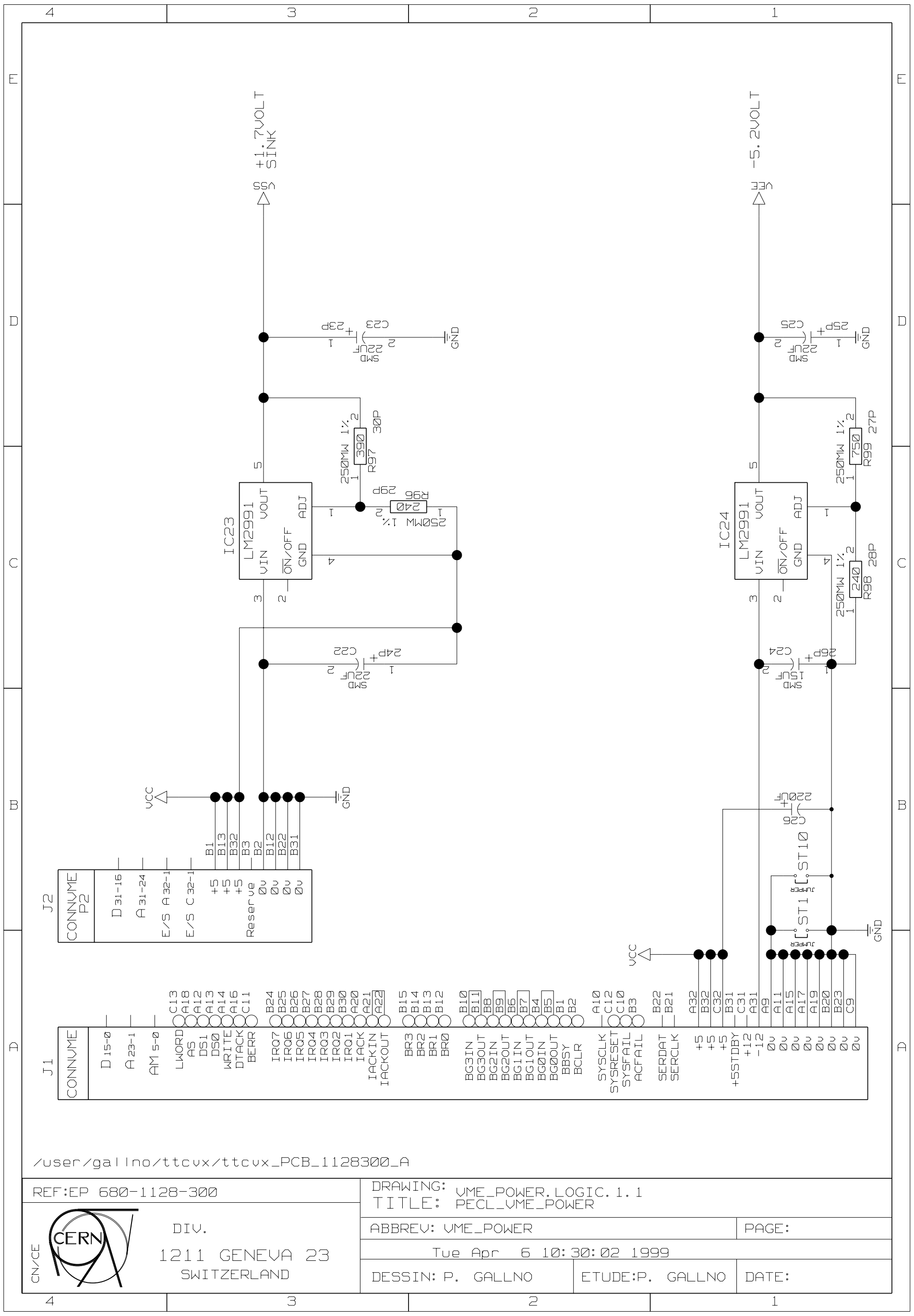
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SINK
-5.2VOLT
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LM2991
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LM2991
J1
CONNVME
J2
CONNVME
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DRAWING: VME_POWER.LOGIC.1.1
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ANNEX A

COMPONENT DATA SHEETS

AMP 269049-1 Optronic Data Transmitter

Features

- Design utilizing advanced molded optical lens technology
- ST style optical interface
- 16 pin multi-sourced packages
- Products compatible with Fast Ethernet, FDDI, ATM and fiber Channel chip sets
- ECL compatible
- Full optical power budget
- Data rates of 125 Mb/s (FDDI), 156, 200 Mb/s (ATM), and 270 Mb/s (FC)
- Single +5 volts power supply
- Process compatible (i.e. wave soldering)
- Robust zinc die-cast housing
- Wide 25 to 75% duty cycle operation

Applications/ Equipment

- Fast Ethernet
- FDDI
- ATM
- Fiber Channel
- Channel Extenders
- Backbone
- Concentrators
- Adapters
- Workstations

Description

The AMP Molded-Optronic 16 Pin Data Links offer full functionality for FDDI and ATM applications. These technologically advanced products incorporate the AMP state-of-the-art designs for high quality data link products at a new low cost. Advancements in the resin circuit board technologies have made precision chip and wire processes a sourceable commodity. Also, optical polycarbonate molding technologies can now provide low cost, high quality camera lenses for 1300 nm fiber optics. Due to these technological breakthroughs, high cost subassemblies can now be eliminated from data link designs without a performance penalty. The AMP offering of 156 Mb/s and 200 Mb/s modules allows for use of 4B / 5B encoding or scrambled Sonet transmission formats.
Units are supplied with process caps which seal the connector interface during soldering and cleaning processes.

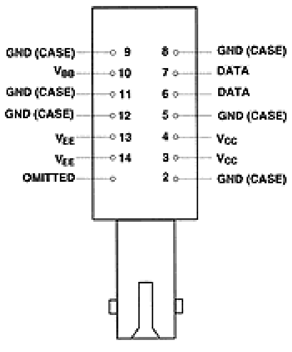
Absolute Maximum Ratings:

Parameter	Symbol	Min.	Typical	Max.	Units
Storage temperature	—	-40	—	100	°C
Lead soldering limits	—	—	—	240/10	°C/s
Supply voltage	V_{CC}-V_{EE}	-.2	—	7.00	V

Transmitter Performance Specifications:
(TA = 0 to 70°C, V_{CC}-V_{EE} = 4.75 to 5.25V DC)

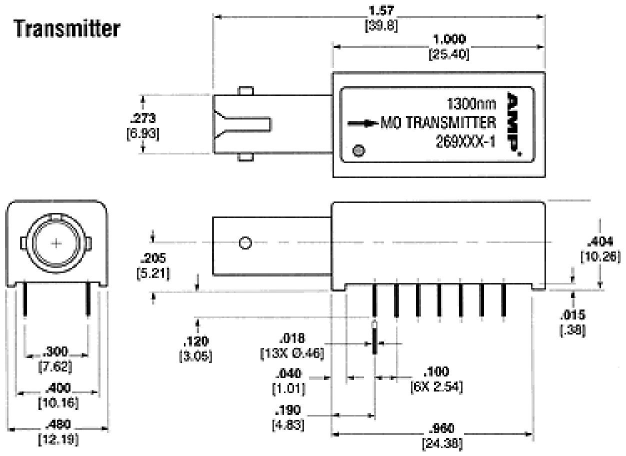
		200 Mb/s			270 Mb/s			
Parameter	Symbol	Min.	Typical	Max.	Min.	Typical	Max.	Units
Data rate (NRZ)	B	0	—	200	0	—	270	Mb/s
Optical output (avg.)(5)	P_{OH}	-19	—	-14	-19	—	-14	dBm
Extinction ratio (P_{OL}/P_{OH}) x 100%		—	—	10	—	—	10	%
Optical wavelength (2)	λout	1270	—	1380	1280	1330	1380	nm
Spectral width (2)	Δλ	—	—	200	—	130	—	nm
Duty cycle	—	0	—	100	0	—	100	%
Output risetime (2)	t_{TLH}	.6	1.2	2.5	.6	—	2.0	ns
Output falltime (2)	t_{THL}	.6	1.2	2.5	.6	—	2.0	ns
Pulse width distortion (1)	—	—	—	0.5	—	—	0.5	ns
Data dependent jitter (1)	t_{DDJ}	—	—	0.3	—	—	0.3	ns
Random jitter (1)	t_{RJ}	—	—	0.5	—	—	0.5	ns
Data (3)(4)	V_{IL}				V_{CC}-1.81	—	V_{CC}-1.475	V
Inputs	V_{IH}	V_{CC}-1.165	—	V_{CC}-.88	V_{CC}-1.165	—	V_{CC}-.88	µA
	I_{IL}	-2	—	—	-2	—	—	µA
	I_{IH}	—	—	400	—	—	400	µA
Reference voltage (output)	V_{BB}	V_{CC}-1.396	—	V_{CC}-1.24	V_{CC}-1.396	—	V_{CC}-1.24	V
Power supply voltage	V_{CC}-V_{EE}	4.75	5.0	5.25	4.75	5.0	5.25	V
Supply current	I_{CC} or I_{EE}	—	—	140	—	—	140	mA
Operating temperature	T_A	0	—	70	0	—	70	°C

(1) Driven with a differential signal.
(2) Limits on optical wavelength, spectral width, output risetime, and output falltime are controlled by figures below.
(3) When V_{BB} is used as the reference voltage.
(4) Voltage levels listed are compatible with 100K Series ECL logic levels. The parts are 100% compatible with 10K and 10KH Series logic when driven with differential signals.
(5) .275NA 62.5/125 µm fiber.
(6) LED emitters comply with IEC 825-1 and -2 requirements for eye safety.



PINOUT WHEN VIEWED FROM TOP

Transmitter



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SEMICONDUCTOR TECHNICAL DATA

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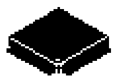
Low Voltage PLL Clock Driver

MPC990
MPC991

LOW VOLTAGE
PLL CLOCK DRIVER



FA SUFFIX
52–LEAD TQFP PACKAGE
CASE 848D–03

The MPC990/991 is a 3.3V compatible, PLL based ECL/PECL clock driver. The fully differential design ensures optimum skew and PLL jitter performance. The performance of the MPC990/991 makes the device ideal for Workstation, Mainframe Computer and Telecommunication applications. The MPC990 and MPC991 devices are identical except in the interface to the reference clock for the PLL. The MPC990 offers an on–board crystal oscillator as the PLL reference while the MPC991 offers a differential ECL/PECL input for applications which need to lock to an existing clock signal. Both designs offer a secondary single–ended ECL clock for system test capabilities.

- Fully Integrated PLL
- Output Frequency Up to 400MHz
- ECL/PECL Inputs and Outputs
- Operates from a 3.3V Supply
- Output Frequency Configurable
- TQFP Packaging
- ±50ps Cycle–to–Cycle Jitter

The MPC990/991 offers three banks of outputs which can each be programmed via the the four fsel pins of the device. There are 16 different output frequency configurations available in the device. The configurations include output ratios of 1:1, 2:1, 3:1, 3:2, 4:1, 4:3, 4:3:1 and 4:3:2. The programming table in this data sheet illustrates the various programming options. The SYNC output monitors the relationship between the Qa and Qc output banks. The output pulses per the timing diagrams in this data sheet signal the coincident edges of the two output banks. This feature is useful for non binary relationships between output frequencies (i.e., 3:2 or 4:3 relationships). The Sync_Sel input toggles the Qd outputs between sync signals and extensions to the Qc bank of outputs.

The MPC990/991 provides a separate output for the feedback to the PLL. This allows for the feedback frequency to be programmed independently of the other outputs allowing for unique input vs output frequency relationships. The fselFB inputs provide 6 different feedback frequencies from the QFB differential output pair.

The MPC990/991 features an external differential ECL/PECL feedback to the PLL. This external feedback feature allows for the MPC991's use as a "zero" delay buffer. The propagation delay between the input reference and the output is dependent on the input reference frequency. The selection of higher reference frequencies will provide near zero delay through the device.

The PLL_En, Ref_Sel and the Test_Clk input pins provide a means of bypassing the PLL and driving the output buffers directly. This allows the user to single step a design during system debug. Note that the Test_Clk input is routed through the dividers so that depending on the programming several edges on the Test_Clk input will be needed to get corresponding edge transitions on the outputs. The VCO_Sel input provides a means of recentering the VCO to provide a broader range of VCO frequencies for stable PLL operation.

If the frequency select or the VCO_Sel pins are changed during operation, a master reset signal must be applied to ensure output synchronization and phase–lock. If the VCO is driven beyond its maximum frequency, the VCO can outrun the internal dividers when the VCO_Sel pin is low. This will also prevent the PLL from achieving lock. Again, a master reset signal will need to be applied to allow for phase–lock. The device employs a power–on reset circuit which will ensure output synchronization and PLL lock on initial power–up.

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REV 3

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MPC990 MPC991

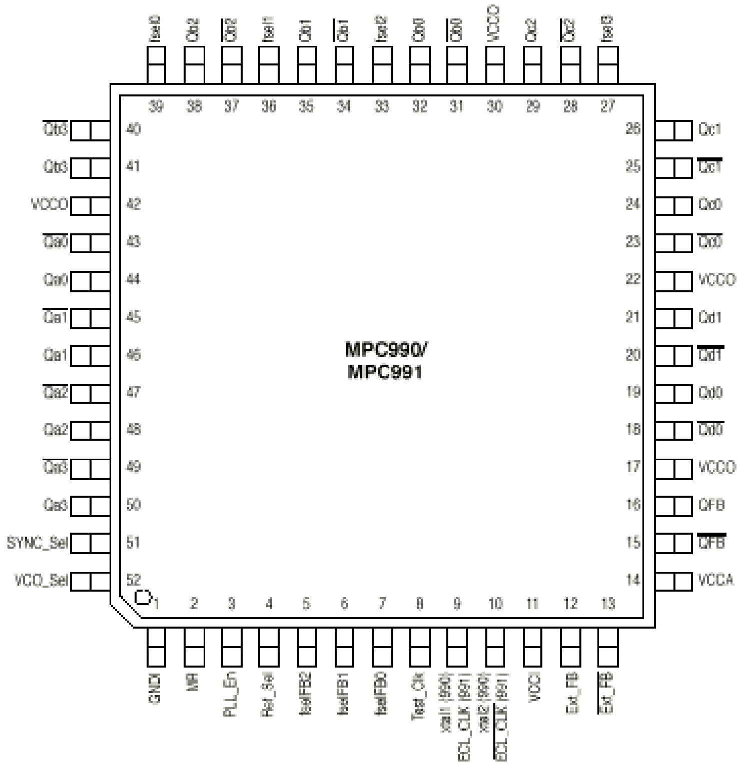


Figure 1. 52–Lead Pinout (Top View)

FUNCTION TABLE 1

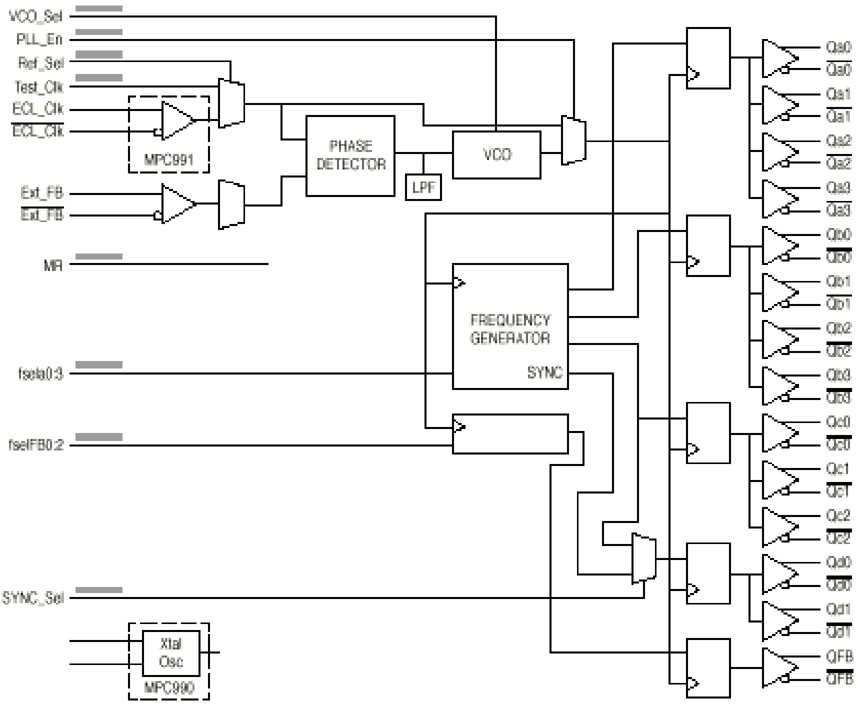
INPUTS				OUTPUTS		
fsel3	fsel2	fsel1	fsel0	Qa	Qb	Qc
0	0	0	0	÷2	÷2	÷2
0	0	0	1	÷2	÷2	÷4
0	0	1	0	÷2	÷4	÷4
0	0	1	1	÷2	÷2	÷6
0	1	0	0	÷2	÷6	÷6
0	1	0	1	÷2	÷4	÷6
0	1	1	0	÷2	÷4	÷8
0	1	1	1	÷2	÷6	÷8
1	0	0	0	÷2	÷2	÷8
1	0	0	1	÷2	÷8	÷8
1	0	1	0	÷4	÷4	÷6
1	0	1	1	÷4	÷6	÷6
1	1	0	0	÷4	÷6	÷8
1	1	0	1	÷6	÷6	÷8
1	1	1	0	÷6	÷8	÷8
1	1	1	1	÷8	÷8	÷8

FUNCTION TABLE 2

fselFB2	fselFB1	fselFB0	QFB
0	0	0	÷2
0	0	1	÷4
0	1	0	÷6
0	1	1	÷8
1	0	0	÷8
1	0	1	÷16
1	1	0	÷24
1	1	1	÷32

FUNCTION TABLE 3

Control Pin	Logic '0'	Logic '1'
PLL_En	Enable PLL	Bypass PLL
VCO_Sel	fVCO	fVCO/2
Ref_Sel	xtal or ECL/PECL	Test_Clk
MR	—	Reset Outputs
SYNC_Sel	SYNC Outputs	Match Qc Outputs



NOTE: ECL_Clk, Ext_FB have internal pulldowns, while $\overline{\text{ECL\_Clk}}$, $\overline{\text{Ext\_FB}}$ have external pullups to ensure stability under open input conditions.

Figure 2. MPC990/991 Logic Diagram

MPC990 MPC991

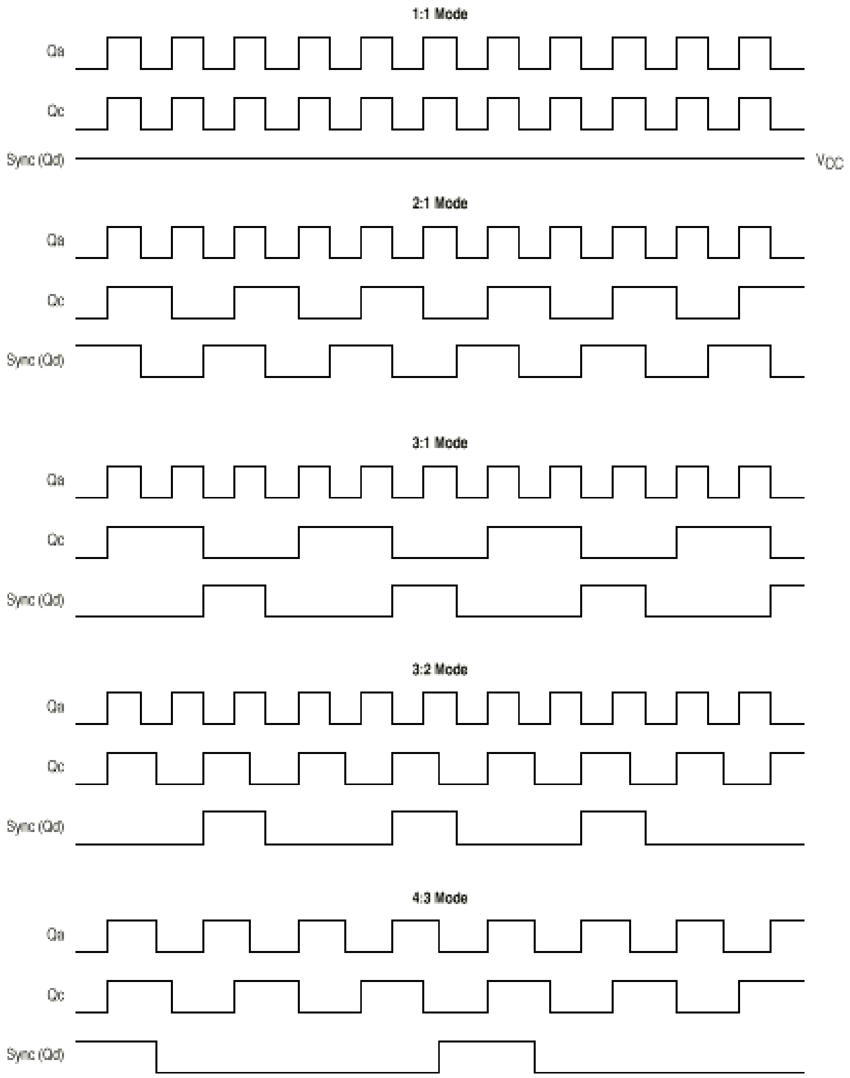


Figure 3. Timing Diagrams

ECL DC CHARACTERISTICS (T_A = 0° to 70°C, $V_{CCA} = V_{CCI} = V_{CCO}$ = 0V, GNDI = –3.3V ±5%, Note 1.)

		0°C			25°C			70°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
V_{OH}	Output HIGH Voltage	–1.3		–0.7	–1.3	–1.0	–0.7	–1.3		–0.7	V
V_{OL}	Output LOW Voltage	–2.0		–1.4	–2.0	–1.7	–1.4	–2.0		–1.4	V
V_{IH}	Input HIGH Voltage	–1.1		–0.9	–1.1		–0.9	–1.1		–0.9	V
V_{IL}	Input LOW Voltage	–1.8		–1.5	–1.8		–1.5	–1.8		–1.5	V
V_{PP}	Minimum Input Swing	500			500			500			mV
V_{CMR}	Common Mode Range	V_{CC} –1.3V		V_{CC} –0.5V	V_{CC} –1.3V		V_{CC} –0.5V	V_{CC} –1.3V		V_{CC} –0.5V	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{GNDI}	Power Supply Current		200	240		200	240		200	240	mA

1. Refer to Motorola Application Note AN1545/D "*Thermal Data for MPC Clock Drivers*" for thermal management guidelines.

PECL DC CHARACTERISTICS (T_A = 0° to 70°C, $V_{CCA} = V_{CCI} = V_{CCO}$ = 3.3V ±5%, GNDI = 0V, Note 2.)

		0°C			25°C			70°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
V_{OH}	Output HIGH Voltage (Note 3.)	2.0		2.6	2.0	2.3	2.6	2.3		2.6	V
V_{OL}	Output LOW Voltage (Note 3.)	1.3		1.9	1.3	1.6	1.9	1.3		1.9	V
V_{IH}	Input HIGH Voltage (Note 3.)	2.2		2.4	2.2		2.4	2.2		2.4	V
V_{IL}	Input LOW Voltage (Note 3.)	1.5		1.8	1.5		1.8	1.5		1.8	V
V_{PP}	Minimum Input Swing	500			500			500			mV
V_{CMR}	Common Mode Range	V_{CC} –1.3V		V_{CC} –0.5V	V_{CC} –1.3V		V_{CC} –0.5V	V_{CC} –1.3V		V_{CC} –0.5V	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{GNDI}	Power Supply Current		200	240		200	240		200	240	mA

2. Refer to Motorola Application Note AN1545/D "*Thermal Data for MPC Clock Drivers*" for thermal management guidelines.
3. These values are for V_{CC} = 3.3V. Level Specifications will vary 1:1 with V_{CC}.

AC CHARACTERISTICS (T_A = 0° to 70°C, $V_{CCA} = V_{CCI} = V_{CCO}$ = 3.3V ±5%, Termination of 50Ω to V_{CC} – 2.0V)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
f_{xtal}	Crystal Oscillator Frequency	10		25	MHz	
t_r, t_f	Output Rise/Fall Time	0.2		1.0	ns	20% to 80%
t_{pw}	Output Duty Cycle	47.5	50	52.5	%	
t_{os}	Output-to-Output Skew Same Frequency Different Frequencies		150 250	250 350	ps	
f_{VCO}	PLL VCO Lock Range VCO_Sel = '0' VCO_Sel = '1'	400 200		800 400	MHz	FB ÷8 to ÷32 (Note 4.) FB ÷4 to ÷32
t_{pd}	Ref to Feedback Offset	75	250	425	ps	f_{ref} = 50MHz (Note 5.)
f_{max}	Maximum Output Frequency Qa,Qb,Qc (÷2) Qa,Qb,Qc (÷4) Qa,Qb,Qc (÷6) Qa,Qb,Qc (÷8)			400 200 133 100	MHz	
t_{jitter}	Cycle–to–Cycle Jitter (Peak–to–Peak)		±50		ps	
t_{lock}	Maximum PLL Lock Time			10	ms	

4. With VCO_Sel = '0', the PLL will be unstable with a ÷2, ÷4 and some ÷6 feedback configurations. With VCO_Sel = '1', the PLL will be unstable with a ÷2 feedback ratio.
5. t_{pd} is specified for 50MHz input reference FB ÷8. The window will shrink/grow proportionally from the minimum limit with shorter/longer input reference periods. The t_{pd} does not include jitter.

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PLL INPUT REFERENCE CHARACTERISTICS (T_A=0 to 70°C)

Symbol	Characteristic		Min	Max	Unit	Condition
t_r, t_f	TCLK Input Rise/Falls			3.0	ns	
f_{ref}	Reference Input Frequency VCO_SEL='0'	Feedback divide 6 Feedback divide 8 Feedback divide 16 Feedback divide 24 Feedback divide 32	100 50 25 16.67 12.5	125 100 50 33.33 25	MHz	
	VCO_SEL='1'	Feedback divide 4 Feedback divide 6 Feedback divide 8 Feedback divide 16 Feedback divide 24 Feedback divide 32	50 33.3 25 12.5 8.33 6.25	100 66.67 50 25 16.67 12.5		
f_{refDC}	Reference Input Duty Cycle		25	75	%	

APPLICATIONS INFORMATION

Using the On–Board Crystal Oscillator

The MPC990 features an on–board crystal oscillator to allow for seed clock generation as well as final distribution. The on–board oscillator is completely self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MPC990 as possible to avoid any board level parasitics. To facilitate co–location surface mount crystals are recommended, but not required.

The oscillator circuit is a series resonant circuit as opposed to the more common parallel resonant circuit, this eliminates the need for large on–board capacitors. Because the design is a series resonant design for the optimum frequency accuracy a series resonant crystal should be used (see specification table below). Unfortunately most of the shelf crystals are characterized in a parallel resonant mode. However a parallel resonant crystal is physically no different than a series resonant crystal, a parallel resonant crystal is simply a crystal which has been characterized in its parallel resonant mode. Therefore in the majority of cases a parallel specified crystal can be used with the MPC990 with just a minor frequency error due to the actual series resonant frequency of the parallel resonant specified crystal. Typically a parallel specified crystal used in a series resonant mode will exhibit an oscillatory frequency a few hundred ppm lower than the specified value. For most processor implementations a few hundred ppm translates into kHz inaccuracies, a level which does not represent a major issue.

The MPC990 is a clock driver which was designed to generate outputs with programmable frequency relationships and not a synthesizer with a fixed input frequency. As a result the crystal input frequency is a function of the desired output frequency. For a design which utilizes the external feedback to the PLL the selection of the crystal frequency is straight forward; simply chose a crystal which is equal in frequency to the fed back signal.

Table 1. Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental at Cut
Resonance	Series Resonance*
Frequency Tolerance	±75ppm at 25°C
Frequency/Temperature Stability	±150pm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5–7pF
Equivalent Series Resistance (ESR)	50 to 80Ω Max
Correlation Drive Level	100μW
Aging	5ppm/Yr (First 3 Years)

* See accompanying text for series versus parallel resonant discussion.

Power Supply Filtering

The MPC990/991 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC990/991 provides separate power supplies for the output buffers (V_{CCO}) and the internal PLL (VCCA) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the VCCA pin for the MPC990/991.

Figure 4 illustrates a typical power supply filter scheme. The MPC990/991 is most susceptible to noise with spectral content in the 1KHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the VCCA pin of the MPC990/991. From the data sheet the I_{VCCA} current (the current sourced through the VCCA pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the VCCA pin very little DC voltage drop can be tolerated when a 3.3V V_{CC} supply is used. The resistor shown in Figure 4 must have a resistance of 5–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

Although the MPC990/991 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

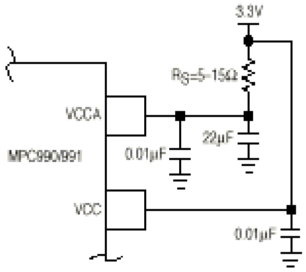

Figure 4. Power Supply Filter

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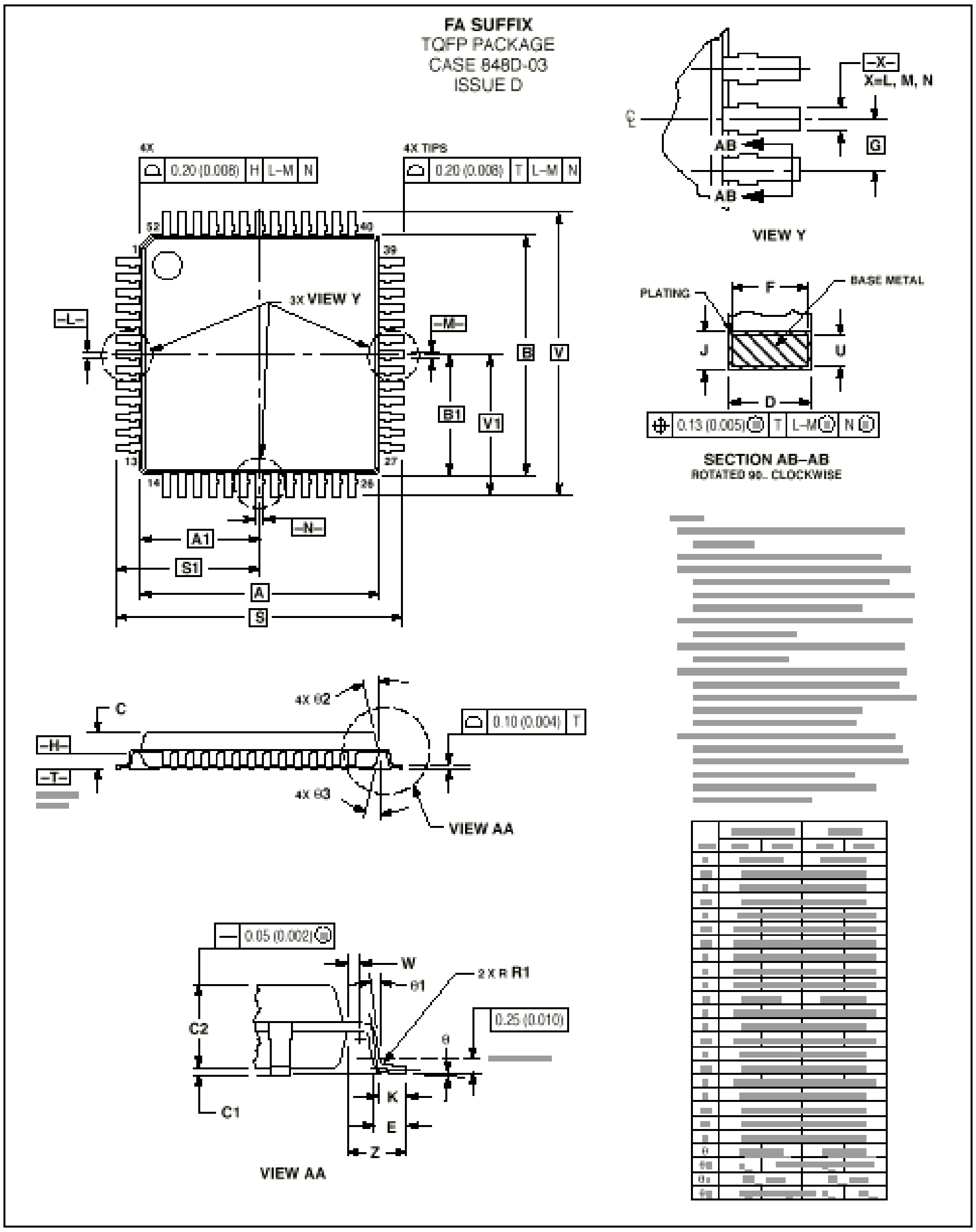
OUTLINE DIMENSIONS



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