Not yet Certified as ATLAS Documentation

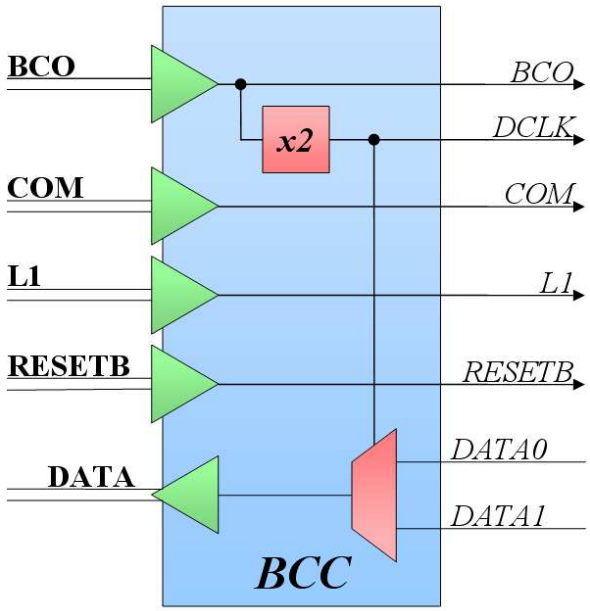
BufferControlChip

Introduction

The BCC ASIC interfaces ABCNs on a hybrid to stave signal distribution. Born out of an opportunity to use ‘spare’ silicon on the edge of a wafer for a run of a larger chips (KPIX) and availability of expertise from SLAC. Manufacture by TSMC, through MOSIS. 0.25um process. Submission March 30, 2009, expecting a 3 month turn-around

Supposed to be a very simple chip LVDS stave to ABCN single-ended

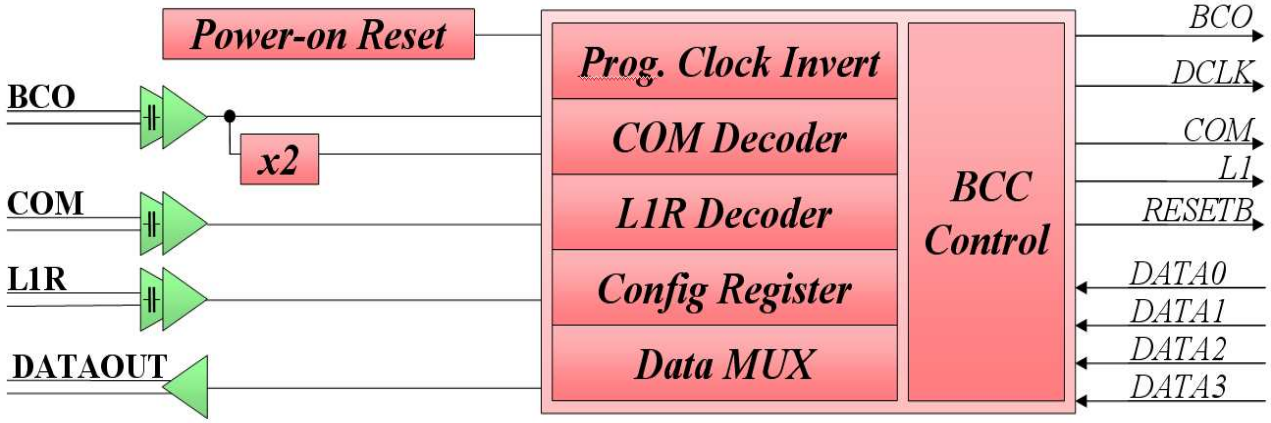
- Clock multiplier for 80MHz readout
- MUX to combine 2 columns of data



The functionality has been increased.

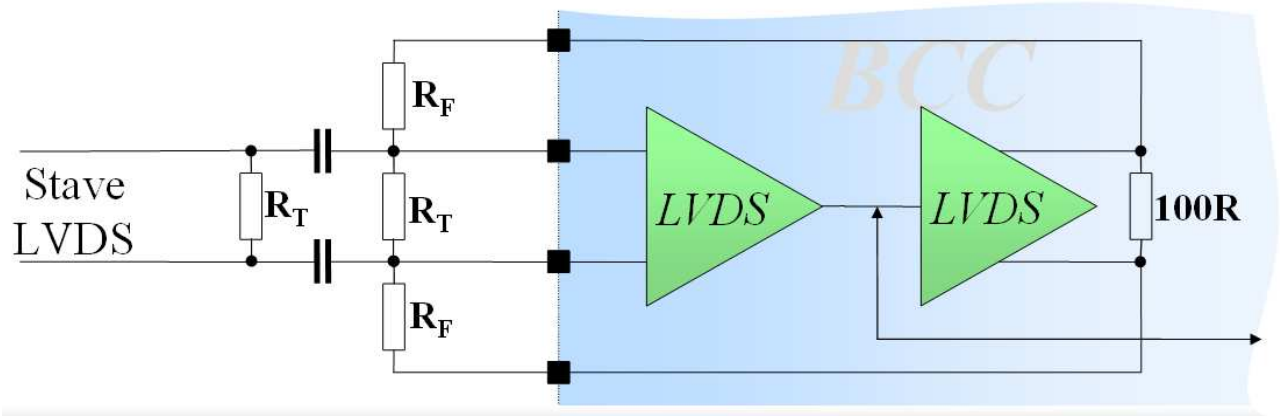
BCC Features

- Special LVDS buffering – DC signalling, AC coupled, DC out
- 40MHz BCO multiply to 80MHz clock
- Config register, with read-back
- ABCN data clock (DCLK) selectable as 40 or 80MHz
- Multiplex 2 ABCN streams onto 80/160MHz data line
- L1 line multiplexed with RESETB (L1R) – separate decoder, provides BCC-RESET
- Programmable Clocks inversion
- ABCN data sync (“sample and hold”) (invertible)
- ABCN signals synchronised to BCO (invertible)
- No-MUX mode – single channel readout select
- Redundant ABCN data lines selectable
- Power-on Reset
- Quad-mode – mux all 4 data lines (low priority feature)



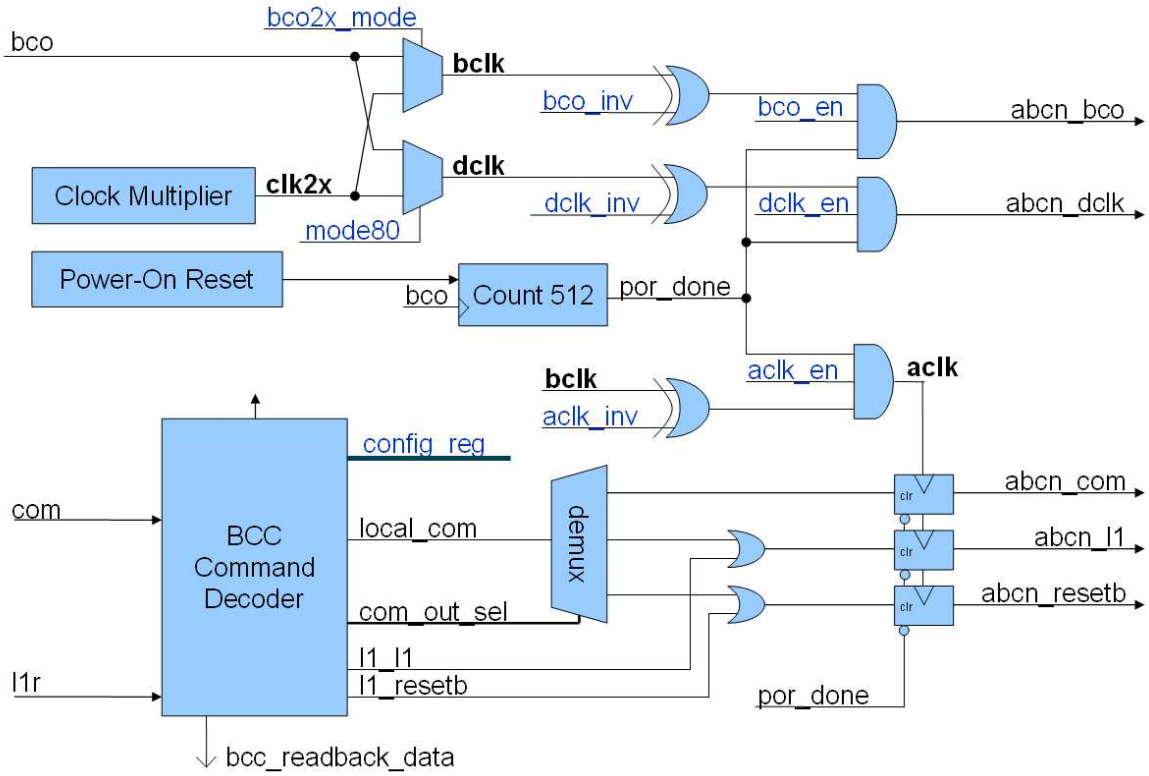
Special LVDS DC-AC-DC Buffer

DC Signals are AC coupled(!). Feedback is used to 'hold' the level beyond the RC constant Passives are external to BCC for tuning. Feedback resistors are set by two requirements: 1) The LVDS receiver needs >100mV on input in the static condition. This value set to 150mV to guarantee proper operation. It could be reduced by 2 with MLVDS. 2) Total input impedance as high as possible for parallel operation (driving several hybrids) The capacitors as set as small as possible to reduce stored energy. The data rate is limited by having two LVDS circuits in series in a feedback mode



Operation I: Clock and Control (Ext-In, Local-Out)

The BCC receives BCO (40MHz Beam Crossing Clock), COM (Command) and ~~L1R~~ (combined L1 and Reset) signals from the outside world. These are enabled/inverted/decoded/doubled as required, resulting in ABCN signals ABCN_BCO, COM, L1, RESETB and DCLK.



Functions can be broken into blocks:

Clock Multiplier

The BCO input clock is multiplied by 2, providing *clk2x*, which can be used for ABCN_DCLK (or ABCN_BCO!)

Power On Reset

And internal circuit provides a power-on reset signal. This feeds a counters that disables chip outputs for 512 BCOs.

Clock Enables and Inversion

The chip makes use of multiple clocks, all derived from the input BCO. *dclk* can be either BCO or *clk2x* depending of a configuration change. ABCN_BCO and ABCN_DCLK can be enabled and inverted as needed. All ABCN signals (COM, L1, RESETB) are clocked out of the chip using the internal *aclk*. *aclk* is This can be inverted and disabled.

Command Decoder

Using a BCC leader (header for a header) the BCC ID can be read, and its configuration can be read, written. payload data can be directed out of the ABCN_COM, L1 or RESEB ports as required Classic ABCD style broadcast signals (L1, BCR, ECR) are decoded correctly (and forwarded to the ABCNs) but incure a 4 clk (??? check) delay in the BCC.

Operation II: Data (Local-In -> Ext-Out)

Sample Clock

DATA from the ABCNs in sampled/synchronised using the flip-flops on the BCC. These are driven by the *sclk* which is an optionally invertable DCLK (which can be either BCO or _clk2x).

Four channels of data channels from the ABCN token rings are selectively multiplexed onto a single DATAOUT line for transfer across a stave. The hybrid is organised into 2 *columns* of ABCN chips. Each column has a 'bottom' and a 'top' data output for redundancy. Either the bottom, or the top DATA can be selected for readout. Each column's data is sampled/synchronised to the *sclk* - an optinally invertable version of the *dclk*. The pair of signal is then multiplexed onto the DATAOUT line. The selector for this MUX is configurable between sclk, /sclk, 0, 1. A special quadmode is also provided. Here all 4 data input are MUXed onto the single data-out. The selection is provided by [bco:clk2x] with no configurable options.