



Engineering Change request

ATLAS Read Out Drivers: Endianness

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ATLAS-Project

BCID and LVL1ID after a Reset

Abstract

The aim of this ECR is to clarify what is the starting value after a Reset of the Bunch Crossing Identifier (BCID) and of the Level 1 Identifier (LVL1ID)

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1 BCID after a Reset

The BCR will be issued at the end of each LHC cycle in order to reset the bunch-crossing counters in the TTCrx. BCID 0 will be allocated to the last BC of the 3.17 μ s gap at the end of the LHC cycle so that the LHC cycle starts with BCID 1.

Ref. The Level-1 Trigger TDR: BCID synchronization section 16.5.2.2 (page 441)

<http://atlas.web.cern.ch/Atlas/GROUPS/DAQTRIG/TDR/tdr.html>

2 LVL1ID after a Reset

After an Event Counter Reset (ECR) the TTCrx sets its internal counter to 0xffff (24 bit), so that the first L1A following the ECR will result in a L1ID 0. This convention shall be used by all RODs (even those who do not directly use the TTCrx).

The above is at first only true for the 24-bit L1ID. The 8-bit ECR counter shall be set to 0 at start of a run by a VMEbus command, and shall be incremented at every ECR. Therefore the value of the 32-bit extended L1ID, following the first L1A in a run, is "0x00000000".

Following L1As get consecutive numbers until an ECR is issued. After an ECR the following event will have the lower 24 bit at "0x000000" and the higher 8-bit incremented by one.

Ref. TTCrx Reference Manual (Page 26)

http://ttc.web.cern.ch/TTC/TTCrx_manual3.8.pdf