

From Cambridge Meeting on 6th May 2010

Martin Postranecky, Matt Warren and Maurice Goodrick met to plan the form and realization of the “Dave VME Module”.

This is brief attempt to summarise the discussions.

Preliminary:

- MP and MW had produced a functional block diagram.
- MP had also produced an initial listing of front panel components
- MG had produced a first draught of a drawing showing these components and how much panel space they would occupy.

Decisions:

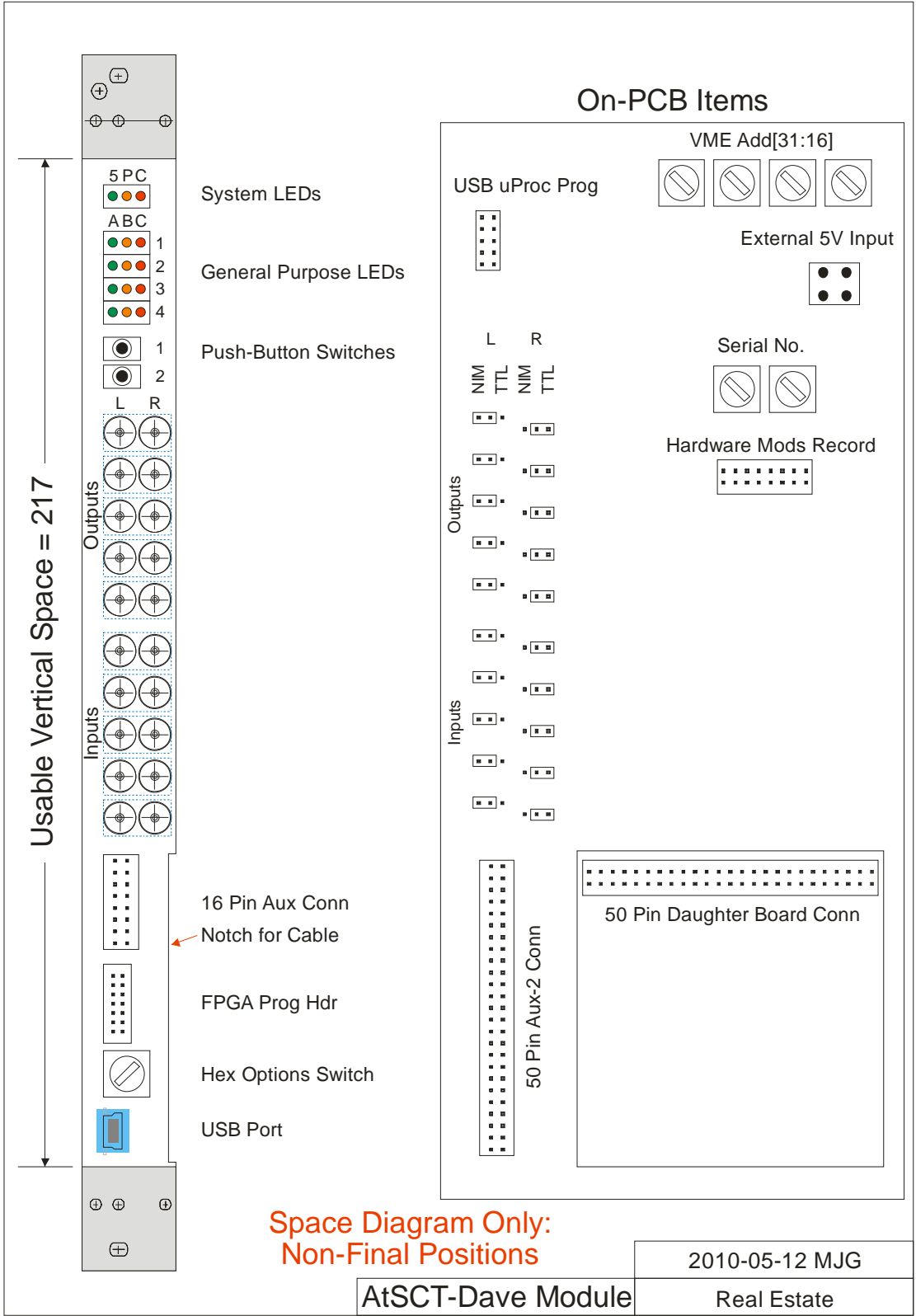
- LVDS input termination: probably on FPGA, but add pads for discrete R terminators
- Front Panel Auxiliary Connector: 0.1in Header as big as will fit (looks like 16 pin)
- on PCB Aux-2 connector with notch in panel for cable (looks like 34-pin) – this to include +5V and Gnd, with the +5V fused. **Other supplies?? 2nd connector for power?**
- Fuses to be thermal, auto resetting.
- Primary Power: 5V - either from VME or on-PCB power connector, the latter to allow out-of-crate operation.
- Other power rails: generated on board as needed (-5V, 1V8, 2V5, 3V3).
- System LEDs: LED for 5V OK, LED for all other rails OK, LED with “Health Heartbeat”
- 6U VME: check that normal, 160 mm depth is OK (Dave?).
- Ideally with eject handles, but does this make it VME64 dependent?
- No J-Aux, just J1 and J2
- A32D16 interface implemented in the FPGA with electrical buffering (**NOT A24 and No Geographical Addressing???**)
- FPGA choice: Xilinx preferred because of experience base and re-use. Probably Spartan 3E. Latest thinking from MW is the Spartan 3E 500K, with and FG320 pinout (XC3S500E-FG320). We should check that parts with more logic are pin-compatible (Rick).
- Lemo00 Inputs and Outputs: 10 of each with flexible choice between NIM and TTL standards. At least 1 of the TTL inputs should have a pull-up (optional or not) for wired-OR functionality. The NIM inputs will not have internal termination.
- ECL requirement? ECL or PECL??
- Implementing Delays:
 - baseline is to use conventional tapped delay lines
 - where possible use FPGA delays
 - Could look at CERN Delay25 ASIC
 - MG will check on TI-Dallas offerings
- Large SRAM for recording Trigger sequences: 32Mb (2M x 18) device identified.
- **Break-Out Header for Daughter Boards – PCI sized?.**
- **Discriminator Inputs???** NO

Division of work:

- Circuit design: MP/ MW/ MG with help from others
- Schematics and Layout: Cambridge (Rick Shaw and/or Saevar Sigurdsson)
- Parts procurement: CB plus others?
- Prototype Assembly: CB
- Production: CB or external? – depends on numbers
- Firmware: MW
- USB Interface and uProc firmware: MG
- Testing: UCL

Later Issues: QPLL/ PLL ? VME buffers? USB- FPGA by SPI or parallel? QuickSwitches?

Price and Schedule?? Need answers soon.



...ooOoo...