

Delay chips

Manuf	Chip	Description	Bits	Step (ps)	Range (ns)	Logic	I/Face	Min Delay	Errors				Pkg	Comments
									Step (ps)	Range (ps)	Non-Lin (ps)	Monotonic?		
AD	AD9501	Dig Prog Delay Gen	8	10	2.5ns-10us	TTL/CMOS	Parallel							Trig-Reset Operation
CERN	Delay 25	4+1 Channel ½ ns Prog. Delay Line	6	500		CMOS/LVDS	I2C			24.5 ns	44 ps	Y	TQFP32	Vcc=2v5, Jitter 19ps, Needs 32,40,64, or 80 MHzClk
Dallas	DS1020/21	Prg 8-bit Silicon Delay Line	8	150,250,500,1000,2000	50 - 500	TTL/CMOS	Par or SPI	10ns			+/- 4ns		SOIC 8	
Data Delay Devices	PDU16F-0.5	6-BIT Prog Delay Line	6	500				8-9ns	+/-300	+/-1600			DIP 24	
Micrel-Synergy	SY89296U	Dual Programmable Delay	10	11	6.2-17.8 ns								TQFP 32, MLF-32	
Micrel-Synergy	SY89297U	CML Dual Programmable Delay	10	11	6.2-17.8 ns								TQFP 32, MLF-32	
ON Semi	MC10EP195	3.3 V ECL Prog. Delay Chip	10	10	2.2-12.2	ECL	Parallel	2.2ns					QFN32, LQFP	
ON Semi	NB6L295M	Dual Programmable Delay	10	11	6.2-17.8 ns									
ON Semi	NB6L297M	CML Dual Programmable Delay	10	11	6.2-17.8 ns									