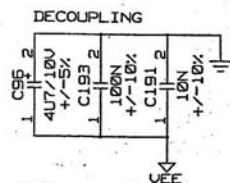


- 1 Polarity: could this be done in the FPGA?
- 2 AC coupling: shouldn't this bias to -400mV, not +200mV ?
- 3 Should the 50R be link-optional ? Could act on TTL i/p
- 4 Should this be LVC running on 3v3 for our design ?
- 5 -

AtSCT-Dave Module
2010-07-13 MJG
Inputs



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