ATLAS PROTOTYPING: FINANCIAL REQUEST 1995/96

I.P. Brawn, R.E. Carney, D.G. Charlton, I. Dawson, J.D. Dowell, J. Garvey, R.J. Homer, P. Jovanovic, I.R. Kenyon, T. McMahon, S.W. O'Neale, S. Oglesby, D. Rees, H.R. Shaylor, R. Staley, A. Watson, J.A. Wilson

University of Birmingham

J.R. Batley, J.R. Carter, M.J. Goodrick, J.C. Hill, D.J. Munday, M.A. Parker, D. Robinson, K.H. Wyllie

University of Cambridge

S. D'Auria, A.T. Doyle, A.J. Flavell, J.G. Lynch, D.J. Martin, V. O'Shea, C. Raine, D.H. Saxon, I.O. Skillicorn, K.M. Smith.

University of Glasgow

T.J. Brodbeck, A. Chilingarov, G. Hughes, T. Komorowski, R.C.W. Henderson, P.N. Ratoff, T. Sloan

University of Lancaster

P.P. Allport, P.S.L. Booth, T.J.V. Bowcock, P.A. Cooke, A. Greenall, C. Green, M.A. Houlden, J.N. Jackson, T.J. Jones, B.T. King, A. Moreton, J.D. Richardson, N.A. Smith, P. Sutcliffe, P.R. Turner, S.E. Tzamarias, M. Wormald

University of Liverpool

I. P. Duerdoth, P.W. Dunne, P.F. Finnegan, J.M. Foster, J. Freestone, S.D. Gilbert, R.E. Hughes-Jones, M. Ibbotson, S.D. Kolya, F. Loebinger, N. Lumb, R.Marshall, D.Mercer, S. Snow, R. J. Thompson

University of Manchester

J.H. Bibby, C.B. Brooks, F.J. Harris, D. Howell, A. Fox Murphy, A. Grewal, B.M. Hawes, A. Holmes, S.J. Hunt, N. Kundu, J.G. Loken, R.B. Nickerson, A. Reichold, P.B. Renton, A.M. Segar, R.L. Wastie, A.R. Weidberg

University of Oxford

G.A. Beck, A.A. Carter, E. Eisenhandler, P. Kyberd, M. Landon, S.L. Lloyd, J.M. Pentney, T.W. Pritchard

Queen Mary and Westfield College, University of London

R.J. Apsimon, J. T. Baines, D.R. Botterill, D.A. Campbell, R.W. Clifft, J.G. Dowdell, T. R. Edgecock, J. Edwards, M. Edwards, R. L. English, E. Evans, S.M. Fisher, C.N.P. Gee, M.D. Gibson, A.R. Gillman, J.R. Gorbold, R. Hatley, S.J. Haywood, D.L. Hill, L.L. Jones, J.L. Leake, D.J. McPhail, R.P. Middleton, M. Morrisey, P. Murray, W. Murray, A.Nichols, P.R. Norton, B.T. Payne, V.J. Perera, P.W. Phillips, B.J. Saunders, P. Seller, T.P. Shah, G.J.R. Tappern, M. Tyndel, D.J. White, F.J. Wickens

Rutherford Appleton Laboratory

A. Belias, B.J. Green, I. Hegerty, Ll-M. Mir, J.A. Strong

Royal Holloway and Bedford New College, London

B. E. Anderson, A. Charalambous, P.E.L. Clarke, R. Cranfield, G.J. Crone, M. J. Esten, T. W. Jones, M. Postranecky, P. Sherwood, N. Wooley

University College London

C.N. Booth, C.M. Buttar, F.H. Combley, M.H. Lehto, S. Manolopoulos, P.J. Sellin, S. Walsh

University of Sheffield

1 Introduction

This document requests the resources needed during 1995-96 for ATLAS prototype work. This must be finished in time, so that the UK groups will be ready to contribute to the construction of the ATLAS detector [1]. Building on the experience and expertise in the LEP and HERA detectors, the UK interest in ATLAS has been focussed on precision tracking and level-1 and level-2 triggers. The UK groups have played a leading role in all of these areas.

In the precision tracking for ATLAS, the UK groups have been prominent both in the overall design and optimisation, and in the R&D for the technologies. The overall production schedule for the ATLAS Inner Detector requires that final decisions on the remaining options must be made in the next year to allow for large-scale prototyping to be be done before module construction starts in the end of 1997. Whilst silicon detectors are a relatively mature technology, considerable R&D is still required to maximise the detector radiation tolerance, develop the electronic readout and develop a low-mass stable structure and cooling system. The GaAs programme will concentrate on producing realistic detector prototypes.

MSGCs are a relatively new technology which is expected to be well suited to the ATLAS requirements in the forward region. Work is required to verify the lifetime of the detector and to minimise the material. Silicon is being considered as an option in the forward region. The decision will depend on a comparison of performance, material cost, integration issues as well as risk assessment. We therefore propose a small extension to the SCT programme to study the use of silicon in the forward region, which will enable us to make an informed decision on which technology to use.

The level-1 calorimeter trigger work in ATLAS originated in the UK and our concept has been adopted as the baseline design. The proposed programme will enable prototyping of key elements needed to decide on solutions for the final design. These are concerned with high-speed data transmission from the experiment to the trigger system using compact fibre-optics, and the required high-speed fan-out of the signals into processing elements that perform pattern recognition in overlapping windows.

The UK level-2 groups have pursued the idea of an asynchronous level-2 trigger and have made the tests necessary for this concept to have been adopted as the ATLAS baseline. Further prototyping work is required to prove connectivity to all sub-detectors and to measure system performance in the laboratory at the full LHC rate.

The detailed programmes are laid out in sections 2 to 5. In addition a minimal funding for the straw tube electronics is requested in order to complete the evaluation of the circuits produced thus far with RD6 funding. A brief statement of the software activity and plans is given in section 7. A summary of the request is given in section 8. Resources required for ATLAS superconducting magnets are not included in this request.

2 SCT

We wish to construct a significant fraction of the SCT [2] in the UK and we therefore request support to continue to play a leading role in the prototyping of the key technologies: Si and GaAs detectors, front-end electronics, optical links, engineering/structures, cooling and alignment. The inner detector construction schedule implies that we need to complete the prototyping work to enable all major options to be chosen within one year. We would then start construction of a section of the detector, the Barrel Sector Prototype (BSP) in 1996 enabling it to be evaluated in 1997 and hence we would be able to ask for tenders in 1997. Module construction requires 2-3 years. We would expect to pay a 25% share for the components of the BSP: detectors, front-end electronics, modules, opto-links and the mechanical structure etc. A summary of the work we propose to do is given here.

- Detectors. Our R&D on Si detectors has indicated that the detectors will be able to survive 10 years of operation at LHC but with no margin of safety at the minimum radius. We therefore need to use the remaining time to produce more robust detectors. We propose to investigate p-type substrates which would avoid the problem of type inversion. We will also produce final prototypes of n+ strips on n or p substrate detectors which can be operated partially depleted. We need to investigate fan-geometry and non-uniform irradiation for the forward silicon option and this will be done initially at minimum cost with dc detectors. Similarly we need to investigate fan-geometry GaAs detectors. To reduce the material and cost of the GaAs detectors we wish to investigate double-sided GaAs detectors. If the forward silicon option is chosen we would wish to produce final prototypes, adopting the technology used in the barrel.

- Front-end electronics. The UK has led the development of the analogue option for the front-end electronics. We have also been strongly involved in the digital option and we are part of the team that will produce the

ATLAS sparse/digital chip based on the Wilkinson ADC and we will therefore contribute to the rad-soft chip run. We also propose to contribute to a Harris run for the selected final prototype of the ATLAS chip (ATLAS-1).

- Optical links. MQWs are a new, but potentially attractive, technology for optical links. They are radiation hard and consume very little power on the detector. They would be particularly suitable for analogue readout but could also be used for digital data. LEDs are a well understood technology and have recently been demonstrated to have adequate lifetime after irradiation. They have been developed for digital data transmission but could also be use for analogue data. We need to prove the viability of these links and make realistic cost estimates by the end of the year. We therefore need to do a production LED run and produce MQWs for the BSP. We also need to produce the final version of DORIC for the clock & control distribution.

- Off-detector electronics. We need to develop modules firstly to fully test the performance in a test beam and then to equip the BSP for full scale system tests. We wish to continue development of a receiver for analogue data (AROMA) and the VME clock & control module. We will also need to purchase general DAQ VME units for the test beam.

- Modules. In order to make the systematic beam test of the different readout options we need to develop realistic modules. This is essential preparation if the UK wishes to bid for a large share of the production of the ATLAS modules. We need to fabricate hybrids and fan-ins for the barrel, GaAs and forward silicon detectors. We need low-mass cables and assembly jigs, supports etc.

- Engineering structure. We need to continue to prototype the critical components for the stave design and the carbon fibre composite structure. We anticipate paying for a 25% share of the BSP structure and cooling system. We have to develop a control system for the binary ice cooling so that we can test the long term stable operation of binary ice. We will complete the development of frequency scan interferometry (FSI) and make measurements on prototypes as a proof of principle. We will use the electronic speckle pattern interferometry (ESPI) to measure the deflections under mechanical and thermal loads of an aluminium stave prototype which will allow us to check the FEA calculations and hence have confidence in the Beryllium stave design.

The milestones for the SCT are given below.

Item	**Milestone**
Si detectors	Test-beam evaluation of full size prototypes
	HV operation of irradiated detectors
	Choice of substrate
Forward Si	Test of fan-geometry and non-uniform irradiation
GaAs	Test of fan-geometry and double-sided detectors
Front-end	System test of full analogue readout
Electronics	Production of prototype digital chip
Modules	Production of fan-ins, hybrids, low-mass cables
	and assembly of full-size modules
	Full electrical and thermal measurements
Engineering structure	Test stability of prototype stave
	Verify FEA thermal and mechanical calculations
	Understand integration to other sub-detectors
Cooling	Long term stable operation of binary ice
Alignment	Proof of principle for FSI

The financial resources requested for the financial year 1995-96 are given in Table 1 and amount in total to £346K. The estimated cost for construction of the large prototypes in 1996-97 is given in Table 2. The estimated manpower requirements are given in Table 8.

3 MSGC

The schedule for the entire ATLAS experiment is given in the Technical Proposal [1], and in detail for the MSGCs in the Support Document [4]. The milestones for the next 3 years are given below:

Dec 1995	Technology choice for the forward tracker.
	Geometry of the forward tracker finalised.
Jul 1996	Choice of substrate, metallisation, gas and front-end electronics.
Dec 1996	Complete final large scale prototype.
Sep 1997	Complete tests on large scale prototype.

To meet these milestones the UK groups will carry out R&D on:

- The mechanical support structure. This is led by the UK with contributions from the NIKHEF and Canadian groups.
- The modules. The UK groups are concentrating on the R&D of closed modules using S-8900 glass as the substrate material, the gas mix and the effects of neutrons on the operation.
- The front-end electronics. The UK groups are concentrating on evaluating the front-end preamplifier and developing the full analogue scheme.

3.1 Proposed Programme

As detailed in the status report submitted to the PPESP, the ATLAS baseline choice for MSGCs uses 400μm thick S-8900 glass with gold metallisation and an Ar/DME gas mix [1]. While this combination has been shown to have most of the attributes required, it has a short radiation length and is relatively expensive. Our programme of work for the next two years falls into five categories detailed in sections 3.1.1 to 3.1.5.

3.1.1 Laboratory work

Here our R&D programme to mid-1996 is directed towards:

1. **Material reduction.** There are a number of possibilities for doing this:
   - Reduction of the thickness of the S-8900 glass. While we have initial quotes for 200 μm thick S-8900 glass of the required size, it would appear to be expensive. Hence this does not appear to be a promising route, and will not be pursued immediately.
   - Increase the radiation length of S-8900 type glass by replacing the barium oxide in the mix by magnesium oxide. This is underway at three centres.
   - Use of a thin ($< 1\mu$m thick) layer of S-8900 glass sputtered on to a thin, lightweight support. Initial results from this are very promising.
   - Use of a lighter bulk material. There are several possibilities being investigated by the ATLAS MSGC groups; coated or uncoated D263 glass and a Plastic (UPILEX). While the NIKHEF and Moscow groups will take the lead in investigating D263 glass, the UK groups intend to contribute in confirmation of results, particularly ageing. The use of UPILEX will be investigated by the Canadian groups.
2. **Lifetime confirmation.** As detailed in the status report submitted to the PPESP, results from accelerated ageing of gold on S-8900 substrates are very promising. There is, however, further work to be done on ageing:
   - Extend the data we have accumulated so far to the full accumulated charge collection of 100mC/cm.
   - Demonstrate that these results can be relied on by doing less accelerated ageing.
   - Run S-8900 MSGC's in the WA102 experiment. The approved 100 days running will give equivalent ageing , from charged particles, to two years LHC running at design luminosity. It will also provide a further demonstration of rate and efficiency capabilities.
   - Complete the investigation of the effects of the neutron flux on occupancy etc. This work has started using the Neutron Irradiation Facility at ISIS.

- Carry out tests of working plates before and after neutron irradiation to substantiate our claims of radiation hardness.

3. **Gas mix studies.** Although we believe our baseline choice of gas mix is Ar/DME, we need to investigate other mixtures in order to confirm this choice.

3.1.2 Test beam work

During 1995 the UK groups will concentrate on use of the H6 beam at CERN, in collaboration with RD28, where we have installed all the infrastructure needed. We have been allocated two running periods, each of approximately 10 days. Our objectives for these tests are:

- Measurement of the two-track resolution.
- Measurement of the gain uniformity of a full-sized keystone detector.
- Confirmation of our simulation of the BCO tagging algorithms.
- Confirmation of earlier results of efficiency and resolution as a function of track angle.

We expect this programme to complete our stand-alone tests in the H6 beam. We plan to move into the H8 beam in 1996 and integrate into the ATLAS DAQ system tests taking place there. In order to facilitate this move we intend to contribute to the build up of the H8 tests being undertaken by the NIKHEF group this year.

3.1.3 Electronics

We plan to continue the evaluation of preamplifier designs, pipelines, BCO tagging circuits, and data transmission. In order to be ready to make the choice of front-end electronics for the final ATLAS detector, we need this evaluation to include fabrication of custom designed chips in collaboration with the silicon BSP project.

3.1.4 Materials study

We intend to continue our programme of research and prototyping into materials suitable for the modules and supporting structure needed for the final detector.

3.1.5 Full disk prototype

We expect the above generic programme of R&D to be completed in the first half of 1996. We then plan to build a 30 degree sector of an ATLAS full wheel in conjunction with the NIKHEF and Canadian groups, to prove the final design. This prototype, consisting of 15 tiles and approximately 7500 read-out channels, would be completed and tested in the H8 beam before embarking on the build of the final detector. We expect the infrastructure needed for these tests will be provided by other groups: the gas system by Cracow, the low voltage supplies by Moscow, and the high voltage supplies by Prague.

3.1.6 Resources

The requested resources for the period 1995-96 are given in Table 3 and amount to a total of £181K. The estimated costs of completing the forward wheel prototypes in 1996-97 is given in Table 4. The manpower requirements are given in Table 8.

4 Level-1 Trigger

4.1 Prototyping Programme

The level-1 trigger prototype programme for 1995 concentrates on the high-speed signal processing needed for the ATLAS baseline trigger design. The programme is presented in detail in the accompanying level-1 trigger status report. The key items to be tested are:

- Data serialisation and optical transmission at up to 1600 Mbaud.
- Optical-to-electrical conversion using integrated optical techniques.
- Serial-to-parallel data conversion and multiplexing using custom-built MCMs.
- Backplane fan-out of serial data at 160 Mbit/s using single-ended signals.
- Reception of serial bit-streams into CMOS ASICs at 160 Mbit/s.

The trigger prototype will use 36 data channels covering a 6×6 cell area of the e.m. calorimeter, within which a 3×3 area will be fully instrumented. Experience in running earlier prototypes shows that this is the minimum viable area needed to retain access to data as the beam is scanned over the calorimeter surface. Operating a reasonable number of channels in parallel is also essential to enable system aspects to be studied.

Test-beam calorimeter data will be digitised in 40 MHz FADCs, processed through BCID logic, serialised at $\geq$ 800 Mbaud, and transmitted on 18 optical fibres each carrying data from two calorimeter channels. The fibres will be received on 9 cluster-processing modules in high-density integrated optical receivers, where conversion to parallel format and multiplexing to 160 Mbit/s will take place. A single multi-chip module (MCM), of the design planned for use in the final ATLAS trigger processor, will be used per cluster processing module. Separate optical receiver modules with discrete commercial optical receivers will also be built to allow electrical data-transmission tests at up to 1600 Mbaud.

Data will be transferred between cluster-processing modules at 160 Mbit/s over a custom transmission-line backplane. Four of the nine cluster modules will be equipped with the original cluster-processing ASICs to complete the trigger processing chain. The proposal includes the minimum number of modules needed to test all required data transfer functions. The design will allow future expansion to test data transfer to downstream trigger processors and readout controllers.

4.2 Resource Request

4.2.1 Capital

The resources requested for the level-1 trigger programme are given in Table 5 and amount to a total of £125K. The programme requires manufacture of a new dual-mode ASIC (whose design is nearing completion), an integrated optical-to-electrical converter, and an MCM. These have a total NRE cost of £60K. Four new module designs are required, and together with the crate backplane, the total board layout cost will be £8K. The irreducible NRE cost is thus £68K.

4.2.2 Manpower

The RAL electronics division manpower requested is as follows. We estimate that design, manufacturing and testing of the multiplexing ASIC, ASOC and MCM will require two full-time electronics engineers for the duration of the project. Layout and component procurement for four printed circuit board designs will require 6 staff months, and 3 staff months of post design services will be needed for assembly of 22 modules. The engineering manpower is given in Table 8.

4.3 Timescale

The following milestones must be met to ensure first beam tests in summer 1996:

Testing of bare-die ASICs completed	July 1995
Working bare-die ASOCs available	August 1995
Tested optically equipped prototype MCMs available	November 1995
Prototype system tests completed	February 1996
Full set of tested system modules available	June 1996
Full system integration tests completed	August 1996
Beam tests commence	September 1996

5 Level-2 Trigger

The test and development programme of the second level trigger group [3] is based around three activities: laboratory tests, beam tests and modelling. Last year we showed that we had developed the basic components for a system by mounting a small system connected to one sub-detector in a test beam. We intend to build on this work by extending the activity to other sub-detectors and expanding the system which can be demonstrated in the laboratory. The UK effort has been central in nucleating the second level trigger activity and our continued participation is vital for the success of this programme. We will continue to play a major role in the ATLAS modelling activity and we provide two members of the ATLAS Trigger/DAQ steering group.

Our main objectives for the year are:

- Connection to and operation with multiple sub-detectors (exploiting our detector independent architecture).
- Demonstration of RoI guidance.
- Measurement of SCI latency with load (for comparison with ATM and FiberChannel).

5.1 Test beam programme.

The principal objective until October 1995 is to set up and run a system in the test beam which connects to up to four sub-detectors. Until then, laboratory effort will be directed at getting the beam test system operational. In contrast to 1994 when the tests were primarily a UK effort, there is now a large multi-national group working on this enterprise. We believe that testing in a beam line is a significant ingredient in the development programme. It is essential to show the completeness and robustness of the system and this is the only way to show that a system can cope with "live" data. In addition, the close working links which have to be established with the sub-detector groups improve the comprehension of both sides and provide a firm basis for work in future years.

The UK contribution to the test beam run would be the data buffers, part of the local network, the local processor system (RHBNC and UCL), interfaces to the global network and the global network and processors (Manchester and RAL). The UK groups have already developed much of the code to run the buffers, the local network, the SCI interfaces, the system supervisor and the algorithms running on the Alpha processors and would remain responsible for these aspects. In addition we would be responsible for the local DAQ system (RAL and UCL). Some of the responsibilities taken on by other groups are outlined below. Cracow are building a new interface to the RD6 prototype which will send us data from all 5 TRT modules. We are co-operating with NIKHEF on the production of units to allow both DAQ and second level trigger data accesses to the MSGC prototype using their AORTA connection. The same system can be used in the future for DAQ and trigger studies with the NIKHEF muon prototype. For this year data from the RD3 liquid argon calorimeter prototype can be obtained via a VIC link and we are discussing with the Saclay group how to arrange this. The data path is slow, but we feel that the connection to the calorimeter is a vital ingredient in the tests, as the region of interest (RoI) pointers available from the first level trigger are from the RD27 prototype connected to the calorimeter. This provides the only way we can run a system with both first and second level triggers operating on the same data. The FERMI group at Paris VI/VII wish to demonstrate the functionality of their system. We are specifying with them the design of a system which will allow communication with the rest of the second level trigger. To extend the functionality of the local network from the link units used in 1994, we are collaborating with NBI Copenhagen on a C40/DS-link interface so that all or part of the local network can use C104 cross bar switches for the 1995 tests. We would expect to see more extensive tests with this and other switch technologies in the future. A major component missing from the tests in 1994 was RoI guidance from the level-1 trigger. Groups at Argonne and Michigan are working on the provision of a basic level-2 Supervisor and they are liaising closely with us (and our UK colleagues on the level-1 trigger) on its specification.

As in 1994, an SCI ringlet is proposed for the global network although more interfaces will be needed. The groups from Manchester and RAL will continue to work in this area together with a group from Valencia and liaison with CERN. Again this year we plan to use DEC Alpha processors in the global system. In the future, when other suitable processors with SCI interfaces become available they could be included with ease.

5.2 Laboratory test programme

The initial laboratory programme will be to get all systems running in a satisfactory form before installation in the beam line. From October the major work will be to measure the performance of systems in the laboratory using data samples which include those obtained in the beam line.

Test beam operation concentrates on demonstrating connectivity to multiple detectors but at a low rate. Using data sources to simulate LHC-like event rates in the laboratory is the best way to determine the performance limitations of components and systems and we intend to pursue these investigations. Accurate modelling of asynchronous systems containing switches and networks of the type we propose to use this year will be significantly aided by the measurements we can make.

In addition to measurements in home laboratories, we have the opportunity to couple our system to the large transputer array of the GPMIMD and MACRAME collaborations at CERN. This will allow measurements to be made on a system which approaches the size and complexity proposed for ATLAS.

For the longer term, we wish to develop closer links with the UK groups working on tracking (and with silicon, in particular). This will allow us to collaborate with the development of the systems to connect the trackers to the DAQ and Second Level Trigger system and the development of the algorithms for triggering.

For this programme we need to provide the equipment listed below. This involves the purchase of items to supplement our current systems and the construction of items developed as a result of our previous test programmes.

5.3 Modelling

The UK is providing a major contribution to the general ATLAS trigger and data acquisition modelling activity and support for the modelling program SIMDAQ. This will be used as a basis for models of beam and laboratory systems so that we can check and update the device and system models.

5.4 Resources

The resources requested for the Level-2 trigger in the period 1995-96 are given in Table 6 and amount to a total of £128K. The estimated manpower requirements are given in Table 8.

6 Straw Tube Electronics

Resources are requested for 1995-96 to complete the following development programme:

- The development of a test system to allow a complete evaluation of the new TRDA chip in its existing environment (separate TRDS and ROC). This will require some VME equipment (crate and controller etc) as well as control and display facilities, and may require iteration of the current design of daughter board. The estimated cost of this equipment is £8K.
- Investigations into the miniaturisation of electronics and the optimisation of miniature pcb layout. This would use the new TRDS-ROC chip and require development of bonding techniques. The estimated cost of this work is £4K.

The manpower requested from RAL Electronics is 1 staff-year.

7 Software

In addition to the prototyping work described in the preceding sections, there is also activity within the UK on software for ATLAS. This includes Monte Carlo simulation, pattern recognition and reconstruction of events, simulation of the trigger and modelling of data flow. Attention is also being paid to the future software needs of ATLAS. At present, no funds are requested for these activities except for travel.

8 Summary

The first round of funding from the PPESP has allowed the UK groups to establish leading roles in the areas of precision tracking and triggering. The layout and design of the tracker is well advanced and will be finalised this year. Prototype silicon modules equipped with LHC type electronics have been evaluated in the test beam and shown to meet the ATLAS specifications. We have demonstrated an MSGC prototype which satisfies the ATLAS requirements. The problems of low charge collection efficiency in GaAs have been understood and solved. GaAs detectors have been produced commercially. For level-1 and 2 triggering, architectures have been developed, demonstrated and adopted by ATLAS.

In the coming year, all the major technological decisions for the tracking must be taken in order to meet the ATLAS schedule. The trigger system design and component prototyping must also proceed in line with the timetable for the experiment. Our proposed programme will supply the information required to make choices in an informed way. Additionally we must prepare for the large scale system tests in the H8 test beam foreseen for 1996-97.

The financial resources requested are summarised in Table 7 and the engineering manpower available in the Universities and requested from RAL are listed in Table 8. These resources would allow the UK groups to maintain a leading role in the areas of tracking and triggering and are required so that the ATLAS collaboration can maintain its schedule.

References

[1] The ATLAS Technical Proposal (CERN/LHCC/04-43).

[2] Technical Proposal Backup Document for the SemiConductor Tracker (SCT) for the ATLAS detector. ATLAS internal note ATLAS-INDET-85.

[3] Tests of Components for an Asynchronous Level-2 Trigger for ATLAS. ATLAS internal note DAQ-NO-36

[4] The support document for the Micro Strip Gas Counter Sub-system which is part of the inner detector for the ATLAS experiment at CERN (ATLAS Internal Note INDET-NO-076)

Table 1: *SCT resource request for 1995-96. Groups involved: B=Birmingham, C=Cambridge, G=Glasgow, La=Lancaster, Li=Liverpool, O=Oxford, Q=QMW, R=RAL.*

Item	Spend (£K)	Groups
Investigation of p substrates	15	
Single sided n+ - Final prototype	23	
Forward dc prototypes	12	
GaAs prototypes : keystone	16	
GaAs prototypes : double-sided	16	
Detectors sub-total	82	C,G,La,Li,Q,R,S
ATLAS Sparse/digital chip (50% share)	15	
Front-end electronics sub-total	15	Li, O, R
LED production run (50% share)	13	
MQW - 10 links for BSP (8 channels)	27	
Optical links sub-total	40	B, O, R
AROMA (2nd iteration prototype)	15	
Clock & Control prototype VME units	5	
DAQ/VME - System tests for silicon readout	18	
ADCs and power supplies for GaAs	5	
Off-detector electronics sub-total	43	C,O,R,S
Hybrids - Barrel and GaAs	20	
Fan-ins - Barrel, Forward and GaAs	15	
Power supplies H8 + development	10	
Low-mass cables/connectors	7	
Assembly Jigs/Cooling/Supports - Barrel	8	
- Forward	3	
- GaAs	3	
Components	12	
Modules sub-total	78	C,G,Li,Q,R,S
Metal Matrix Rings	25	
Sliding Joints	5	
Al extrusion	2	
Composite prototype cylinder (50% share)	15	
Silicon structure - TRT interlinks (50% share)	7	
- Pixel interlinks (25% share)	3	
- Forward wheels	5	
Rig for radiation tests	1	
Cabling model	3	
Thermal model	5	
Engineering-structure sub-total	71	La,O,Q,R
Cooling control system:	7	
Cooling sub-total	7	Q,R
FSI corner cubes	5	
Camera for ESPI	5	
Alignment sub-total	10	O
Grand Total	**346**	

Table 2: *BSP estimated costs for 1996-97. A * in the cost column indicates commit only after a decision at the end of 1995. There will be additional costs associated with developments for production.*

Item	Spend (£K)
25% share of ATLAS production run 200 detectors	50
Final forward prototypes	23*
Detectors sub-total	73
ATLAS-1 (radhard 65% share MSGC/TRT)	36
ATLAS production run for BSP (25% share)	25
Front-end electronics sub-total	61
MQW hybrid transceivers	10
DORIC final version (50% share)	13*
50 MQW links	40*
Opto-links sub-total	63
DAQ system for BSP	40
Off-detector electronics subtotal	40
Hybrids - Barrel, Forward and GaAs	10*
- barrel pre-production (25% share)	6
Fan-ins - barrel pre-production (25 % share)	4
Power supplies/cables for BSP	25
Modules sub-total	45
Silicon support - Forward wheels	5*
BSP structure (25%)	5
Engineering-structure sub-total	10
Cooling plant for BSP (25% share)	6
Cooling sub-total	6
FSI cavity	10
Alignment sub-total	10
Grand Total	**308**

Table 3: *MSGC resource request for 1995-96. Groups involved: Birmingham, Manchester, RAL and UCL*

Item	Cost (£K)	Groups
Materials R&D, module mechanics, etc.	40	RAL, UCL
Electronics	30	RAL
Substrates	70	Manchester, RAL
Gas studies	15	Birmingham, UCL
Neutron studies	10	UCL, RAL
WA102 Programme (as recommended by the PPESP)	6	Manchester, UCL
Contribution to build up of H8	10	Manchester, RAL
Grand Total	**181**	

Table 4: *MSGC estimated costs for 1996-97*

Item	Cost (£K)
UK contribution to the full size disk prototype	100
Mechanics	20
Electronics	20
Substrates	20
Gas studies	10
Test beam equipment	20
Grand Total	**190**

Table 5: *Level-1 trigger resource request for 1995-96. Groups involved: Birmingham, QMW and RAL*

Item	Comment	Cost (£K)
Dual-mode ASIC (ES2)	NRE	25
	ECL Pads & Simulation	6
	Production chips	9
Integrated optics MCM	NRE	24
	Packaged parts	27
Cluster processing module	NRE + modules	27
Optical receiver module	NRE + modules	12
Transmitter module	NRE + modules	16
Optical fibre links & Test modules		8
Clock modules	NRE + modules	5
Crates & backplanes		14
Computing support		2
Less remaining 1994 allocation		-50
Grand Total		**125**

Table 6: *Level-2 trigger resource request for 1995-96. Groups involved: Manchester, RHBNC, RAL, and UCL*

Item	Number	Cost (£K)	Groups
VIC modules	1	3	
VME processors	1	3	
Memory boards	6	6	
C40 boards	15	15	
LVI boards	7	4	
Fan-out boards	9	3	
C40/DS-link boards	5	2	
VME crates	3	9	
LynxOS	1	4	
C40 TIMs	2	4	
Prototype silicon interface	1	8	
Monitor workstation	1	5	
Local sub-total		66	RHBNC, UCL
Alpha processor boards	2	4	
C40 boards	4	4	
C40/SCI transition boards	4	4	
AXP workstation	1	5	
SCI/PCI interface	5	8	
VxWorks (OS for global)	4	8	
SCI/PCI Accelerator	1	4	
Integrated SCI/C40	1	3	
Cables, spares		6	
Global sub-total		46	Manchester, RAL
LynxOS (OS for DAQ)	1	4	
VIC module	1	3	
VME processor	1	3	
DAQ sub-total		10	All
Test equipment & data sources	2	6	All
Grand Total		**128**	

Table 7: *Summary of financial resources requested for 1995-96.*

Sub-project	Cost (£K)
SCT	346
MSGC	181
Level-1 trigger	125
Level-2 trigger	128
TRT electronics	12
Grand Total	**792**

Table 8: *Estimated engineering effort in staff-years/year available from universities, and effort requested from RAL Engineering and Technology Divisions.*

Activity	University Engineers	University Technicians	RAL Electronics	RAL Technology
SCT			9.0	10.0
Birmingham	0.5	0.5		
Cambridge	1.4	2.5		
Glasgow	5.0	4.5		
Lancaster	1.0	2.0		
Liverpool	3.5	2.5		
Oxford	6.0	4.0		
QMW	1.5	3.0		
Sheffield	-	2.0		
MSGC			2.5	2.0
Birmingham	0.5	1.0		
Manchester	2.0	4.5		
UCL	1.0	1.0		
L1 Trigger			2.75	
Birmingham	1.0	0.5		
QMW	0.5	2.0		
L2 Trigger			1.0	
Manchester	2.0	2.0		
RHBNC	1.0	1.5		
UCL	2.0	1.0		
TRT electronics			1.0	