ATLAS UK PROPOSAL TO STUDY p-p INTERACTIONS AT THE LHC

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Principal area of activity in ATLAS:
(1) Inner Detector, (2) Level-1 Trigger, (3) Level-2 Trigger, (4) Software development and simulation.

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1 Introduction

1.1 Structure of the Proposal

In this proposal the UK ATLAS groups request the necessary support from the PPESP to allow them to play a central role in the construction and commissioning of the ATLAS detector [1] over the coming eight years, leading to its subsequent exploitation. Firstly the physics objectives of the experiment are outlined and then the activities and experience of the UK groups relevant to their proposed programme are reviewed. Following sections contain a more detailed account of the major activities to which UK groups wish to contribute within the ATLAS project, namely the precision tracker and the level-1 and level-2 triggers, and the case for the requested funding. In bidding for a major share of each of these activities the UK groups propose building on their areas of expertise. Their involvement in these crucial areas of the project will enable them to take full advantage of the physics potential of ATLAS from the beginning of physics running at the LHC. A summary of the requested resources, together with the proposed spend and manpower profiles, is given in section 8.

1.2 Physics Motivation

Over the last decade the UK groups have made a significant impact on the physics programmes at the $p\overline{p}$ and e^+e^- colliders at CERN, and the ep collider at DESY. Their contributions to instrumentation have been prominent in the areas of precision tracking and event triggering, particularly fast triggering, and they have exploited this expertise by leading many of the physics analyses that have been dependent on data from these detectors. This work has contributed in a notable way to our present understanding of the nature of elementary particle interactions as summarised in the Standard Model. Within the ATLAS experiment the UK groups wish to build on this experience and extend it to the new regime of interactions in the TeV mass scale.

The ATLAS experiment will provide the opportunity of exploring a wide range of phenomena and the physics reach of the detector is discussed extensively in the ATLAS Technical Proposal [1]. Searches for new particles will range from states to be expected within the Higgs sector to more exotic predictions from, for example, supersymmetry. The experiment will also provide a unique precision test-bed for a continuing programme of quantitative studies both within and beyond the Standard Model.

Although the highest TeV energies and luminosities will be needed to complete the searches programme, the expected initial years at lower luminosity and possibly lower energy will allow important measurements to be made in the heavy quark and lepton sectors, as well as studies of CP-violation and rare decays.

The physics objectives of the ATLAS experiment require high precision tracking around the interaction region with the largest possible coverage in η. This must be coupled with low P_T triggering thresholds, excellent electromagnetic calorimetry for electron and photon identification and good jet and missing E_T calorimetry. The inner detector sits within a 2T axial superconducting solenoid allowing good momentum resolution up to 500GeV/c for enhanced electron identification through E/p matching, independent muon momentum measurement and charged hadron reconstruction. Good impact parameter resolution for heavy flavour physics is also achieved. Stand-alone muon momentum measurements are possible up to the highest LHC luminosity using the large muon spectrometer consisting of the outer superconducting air-core toroids instrumented with precision drift chambers. Two examples of the resulting physics performance are illustrated in figures 1 and 2 [3],[4].

1.3 The UK Contribution to ATLAS

The UK groups propose to make major contributions in specific areas of this extensive project :

- **Event triggering :**
  The very high event rate required for the TeV pp collisions imposes formidable requirements on both the event selection criteria and subsequent processing. The UK groups have taken the intitiative in these areas, building on their already considerable expertise. In the level-1 calorimeter trigger project, initiated by the UK, the design requires high-speed data transmission using compact fibre-optics and signal fan-out and processing techniques. In the level-2 trigger, again a UK ATLAS concept, an asynchronous approach has been adopted. This has already been demonstrated to satisfy the ATLAS specifications and further prototyping work will prove connectivity to all sub-detectors and measure system performance at the full LHC rate.

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Figure 1: Simulated 4-lepton invariant mass distribution for m_H =130, 150 and 170 GeV, showing the expected shape of distribution (dashed line) and result from one experiment after $10^5 pb^{-1}$ integrated luminosity.

- **Precision tracking :**
  Initiatives by the UK groups have been central to optimising this layout design, and in proposing the appropriate instrumentation techniques and their development programmes. In particular the UK work centres on silicon and gallium arsenide (GaAs) semiconductor detectors and on microstrip gas avalanche chambers (MSGCs). The current ATLAS inner tracking scheme is heavily dependent on semiconductor devices in the central barrel region, with GaAs detectors being more appropriate to regions of higher particle fluxes nearer the forward direction. The MSGC instrumentation is proposed for the forward regions where also silicon strip devices offer an alternative approach. Both implementations for this region are under study, with strong UK involvement, and have important milestones of technical achievement to demonstrate in the near future. All the UK personnel from the MSGC activity are committed to contributing to construction of the precision inner tracking, whichever solution is chosen. Although a final decision to adopt an integrated all-semiconductor option would truncate the UK MSGC activities, the groups concerned would become part of the extended UK responsibility that would then cover both barrel and forward semiconductor tracking within a cohesive programme of work for the inner detector. The implications on the requested funding, explained in this proposal, are almost independent of the final choice.

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Figure 2: The ATLAS b-tagging performance

- **Exploiting the data :**
  The successful exploitation of the data from a detector as complex as ATLAS, with data flow rates at the Tb/s level, clearly requires the development of highly efficient, state-of-the-art software tools and management. The UK has traditionally provided a reservoir of extremely competent and far-sighted software engineers and physicists, who have introduced modern data handling techniques into the latest high energy physics activities. ATLAS UK groups plan to continue this tradition, and a specialised team is already working towards defining ATLAS software standards for the next decade.

In the area of TRT electronics, UK groups have played an important part through the RD6 collaboration. RAL electronics expertise has proved invaluable in designing a radiation hard amplifier/shaper/discriminator satisfying the required ATLAS specifications. A second version of the chip, now under test, shows encouraging results, making it a candidate for being chosen for use in the final ATLAS TRT modules.

1.4 ATLAS Management Structures and Decision-making Processes

A large collaboration such as ATLAS, with around 1500 participating physicists, requires substantial structures for its efficient management. ATLAS has established such structures, including a Collaboration Board with representation by each participating group and a democratically-elected Chairperson. The CB is the ultimate decision-making body in ATLAS. A smaller Executive Board has also been set up, to advise the Spokesperson and the Steering Groups managing the various sub-detector projects. Review panels have been created as necessary to consider options for the different sub-detectors and make recommendations to the Collaboration Board. Technical and Resource Co-ordinators have been appointed and are already active in drawing together the requirements of different components of the final detector. The UK is very well-represented in all of these management structures, as indicated in Appendix A.

Within the UK community, similar structures include a UK Collaboration Board with representation from each group and an elected Chairperson and Deputy. A small Steering Group has also been set up to ensure maximum coherence of the UK effort in our various sub-projects.

1.5 The Common Fund

As has been found necessary in previous large experiments at CERN, the ATLAS Collaboration proposes that certain items be purchased collectively through a Common Fund. Such items are either beyond the financial capability of the groups directly involved or are of a highly specialised technology, such as the magnets. The total cost of the proposed Common Fund items has been estimated to be 190 MCHF.

ATLAS proposes that the obligation to the Common Fund should be proportional to the cost of the other (non-Common Fund) pieces of apparatus which the groups provide. Provisions have been made for the possibility of *in kind* contributions in lieu of cash payments in order to overcome some of the contractual difficulties which might arise.

Amongst the main items on the Common Fund list are the end-cap toroidal magnets and associated cryogenic plant. The RAL superconducting magnet team is responsible for the design of these end-cap toroids, at the request of the ATLAS collaboration. Each toroid consists of eight superconducting 'pancake' coils assembled inside a single cryostat and the large radial magnetic forces on the coils are absorbed in the self-supporting cold mass structure linking them. Particular attention has to be paid to conductor stability, quench protection, safe and reliable response to faults, and structural integrity of the design. An extensive R&D programme, supported and monitored by CERN, has been initiated, to include the development of suitable conductor, the winding of a test racetrack coil and studies of conductor stability. The construction and assembly of the toroids will be carried out in industry, with contracts placed according to the rules of the CERN Finance Committee. This creates an excellent opportunity for UK industrial firms to tender competitively for the construction contracts.

2 The Atlas Inner Detector

2.1 Introduction

2.1.1 Overview and UK Objectives

The physics goals of ATLAS at TeV energies span a wide range of topics, from continuing quantitative measurements to test and probe beyond the Standard Model, through to studies of the Higgs sector and, more speculatively, compositeness and supersymmetry. In most cases the experimental signatures for such physics processes can only be extracted from the QCD background by identification of high P_T leptons and heavy quarks. For the leptons, accurate tracking in the central volume is vital for clean electron identification (through E/p matching) and provides an important independent measurement of muon momenta. Furthermore, precision vertexing is needed for reliable τ lepton reconstruction and for high efficiency, low background b and t quark identification. This latter capability is important for low luminosity studies of $B\bar{B}$ mixing, CP violation and top decays, but it is also a requirement for the dominant Higgs decays in the most difficult mass range and for many of the high luminosity searches. In summary, the Inner Detector is vital to the most exciting physics analyses of ATLAS.

From their current and past research, the UK ATLAS groups have particular experience and expertise in physics associated with precision tracking which they wish to extend into the ATLAS experiment. This situation is closely coupled to the established reputation of the same UK groups in the instrumentation needed to carry out heavy flavour physics; namely precise charged particle tracking for both primary and secondary vertex reconstruction, as well as aspects of fast triggering and overall event reconstruction. The specific techniques proposed here are centred on semi-conductor devices, both silicon and gallium arsenide, and microstrip gas chambers.

In the following sections we review briefly the activities of the UK groups in these areas of instrumentation, and explain how the use of these technologies is appropriate to an optimised ATLAS inner tracker. We then discuss the programme of work needed to allow final sub-detector construction to begin in three years time. Finally the UK responsibilities and planning across the subsequent seven to eight years of construction and commissioning are discussed, and the requested PPESP funding and resources are described and tabulated.

2.1.2 The Matching of UK Expertise to Precision Tracking

Throughout the last two years the PPESP has supported the UK ATLAS groups in much of the specific development work they have done towards prototypes of the expected ATLAS final devices. This has allowed the UK groups to initiate many of the detector and electronics studies associated with the ATLAS semiconductor projects and they are now well placed to lead these through to the final decisions on the specific components that will instrument the overall ATLAS inner tracker.

The UK groups have played key rôles across a range of DRDC sponsored projects associated with precision tracking:

- RD2 — Tracking/preshower detectors and electronics
- RD6 — Straw tube transition radiation tracker
- RD8 — GaAs tracking detectors (ATLAS-UK co-spokesman)
- RD20 — High resolution silicon microstrips and electronics
- RD23 — Optoelectronic analogue signal transfer
- RD28 — Gas microstrip detectors (MSGCs)

The groups have also driven much of the transfer of the practical knowledge gained from this work into the context of the ATLAS experiment.

Furthermore, in the field of large–array silicon tracking systems, members of the ATLAS-UK community have led projects for both the DELPHI and OPAL microvertex programmes and many UK silicon experts from these and other projects (*eg* the UA2 silicon detectors) are now actively working on the ATLAS SCT. Some examples of major contributions made by ATLAS-UK personnel to semiconducting tracking systems currently running successfully around the world include:

- The MX series of microplex chips developed at RAL, initially for the DELPHI microvertex detector(MX3, MX6)[8] and also extended with the collaboration of UK physicists for use in both the OPAL(MX5, MX7 and MX7-RH) and ALEPH(MX7-RH) microvertex projects. Both the conventional CMOS and radiation hardened (RH) designs have been extensively used across a range of applications both within and outside HEP and this has helped reinforce the basis for the RAL Technology Division's broad involvement in the electronics for the LHC.
- The high precision beryllium mechanics of the CCD vertex detector (the VXD)[7] in the SLD experiment at the Stanford Linear Collider which is cooled to $-80°C$ while retaining resolutions of $\leq 10\mu$m.
- The silicon microstrip detectors developed and used by OPAL[9], manufactured by Micron Semiconductor (UK) Ltd, which were also subsequently adapted for use in the 4 layer silicon vertex detector (the SVX) of CDF which proved critical for the discovery of the top quark at Fermilab.

As a result of this expertise several UK personnel hold key positions within the ATLAS experiment (Appendix A). There are UK members on the ATLAS Executive Board, including the Inner Detector Steering Group co-ordinator, and on the Steering groups of both the Inner Detector and the SCT. There is also a UK physicist on the Inner Detector review panel.

3 A Description of the ATLAS Inner Detector

Charged particle track reconstruction in the region close to the primary interaction is a demanding task at the LHC. Detailed studies have looked at particle multiplicities and distributions and multiple-event overlaps to set the specifications for a scheme with good track resolution, particle indentification and momentum measurement. A proposed layout has an inner detector 2.3m in diameter, 6.8m in length, and situated inside a superconducting solenoid providing a 2T axial magnetic field. Within a radius of about 1m from the interaction point it has been found that a combination of inner discrete hit measurements followed by more continuous information at larger radii can provide an acceptable solution, satisfying bounds both on overall material represented by the detector and on project cost.

The inner detector will be constructed in three units, consisting of a barrel part extending over ± 80 cm, and two identical forward sections that instrument the remainder of the cylindrical cavity. The general support and services for the detectors are placed around the outer radius.

During high luminosity running the nearest devices to the beam are semiconductor pixels (Table 1). These are followed by precision strip detectors up to a radius of 60cm. Beyond 60cm the straw tube system provides both transition radiation detection and more continuous track measurements with minimal material and cost.

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Figure 3: The ATLAS Technical Proposal Inner Detector Layout

In the barrel, the high-precision detector layers form concentric cylinders around the beam axis, with the exception of the disks of pixel detectors in the forward direction, ($|\ \eta\ | \geq 1.7$) which are arranged perpendicular to the beam, similar to all the elements of the forward sections. The barrel TRT straw tubes are parallel to the beam direction. The silicon microstrip layers provide both $R\phi$ and z co-ordinates from axial and stereo measurements, while the straw tubes use drift-time information to provide radial information only. Both systems contribute to the second level triggering.

For the earlier low luminosity operation, a high precision vertexing layer is installed at a radius of 6cm. This further enhances the $b-$physics (CP–violation, rare decays) potential of the experiment, exploiting the very high production rates of $b-$quarks at the LHC, by providing 70% efficient $b-$tagging for $|\ \eta\ | \leq 2.1$ with rejection factors of ≥ 100 against background processes.

Table 1: Parameters of the Technical Proposal Layout for the Inner Detector. Resolutions correspond to single points (single pixel layers, stereo pairs in silicon and GaAs strips, triplets in MSGCs and single straws), and do not include alignment errors.

System	Position	Area (m^2)	Resolution σ (μm)	Channels (10^6)	η coverage
Vertex silicon	1 barrel layer	0.2	$R\phi = 10, z = 20$	0.03	± 2.1
Pixels	2 barrel layers 4 forward disks on each side	1.4 0.8	$R\phi = 14, z = 87$ $R = 87$	140	± 2.5
Silicon strips	4 barrel layers	41	$R\phi = 15, z = 770$	2.9	± 1.4
GaAs	2 forward disks on each side	3.3	$R\phi = 10, R = 1200$	0.8	2.0–2.5
MSGC	12 forward disks and 1 wheel on each side	51	$R\phi = 35, R = 1800$	1.5	1.4–2.5
TRT	Axial barrel straws Radial forward straws 36 straws per track		170 (per straw)	0.1 0.32	± 2.5

In the forward direction $1. < \eta < 2.5$, the required momentum resolution is provided by large area precision strip detectors. Microstrip gas counters (MSGCs) represent a solution which is expected to provide an economical means of covering this region and coping with the expected radiation levels which will increase by about a factor of two between the barrel ($| z | \leq 80$cm) and the far forward region ($| z | \geq 300$cm). An alternative design for this forward region based on silicon devices is now under consideration. This design calls for a modified barrel and has the advantage of using a single technology for the strip detectors, allowing the use of identical read-out electronics in the barrel and forward regions.

The layout in Fig. 3 shows silicon strip devices in the barrel and microstrip gas counters (MSGCs) as the high-precision detectors in the forward regions, complemented with gallium arsenide (GaAs) microstrip detectors for the highest rapidity range with the most severe radiation levels. Fig. 4 shows the alternative solution, the *Morges* layout, with an integrated semi-conductor tracker covering both the barrel and forward regions complemented as before with outer straw drift-tubes. Such a design benefits from a uniformity of technology, cooling and engineering and provides a coherent detector throughout the range up to $\eta < 2.5$.

The main features of the integrated semi-conductor tracker layout are:

- the barrel instrumentation becomes $\pm$ 76 cm in length
- the four barrel layers have radii 30 cm $< R <$ 52 cm
- 6 discs per side with radii 32 cm $< R <$ 56 cm, 1 per side with 38 cm $< R <$ 56 cm and 2 per side with radii 44 cm $< R <$ 56 cm
- detectors with a fan geometry giving a mean spatial precision of 15 μm at radii of 38 cm with a linear variation from 32 cm to 44 cm radius and similarly a linear variation between radii of 44 cm and 56 cm with 15 μm resolution at a radius of 50 cm.
- three discs have GaAs detectors covering 24 cm $< R <$ 30 cm and one disc has a GaAs detector covering the range 18 cm $< R <$ 30 cm
- GaAs detectors have a fan geometry with a mean pitch of 50 μm at $R = 24$ cm.

The momentum resolution for this layout is shown in Fig. 5 as a function of η and the number of pairs of stereo hits on a track as a function of η (not including the 2 pixel space–points) is shown in Fig. 6. The number of space–points at high values of η has been increased to 5 to improve the pattern recognition in this difficult

Table 2: Parameters of the *Morges* Integrated Semi-conductor Layout for the Inner Detector. (The values for the pixels, TRT and low-luminosity vertexing layer options are unchanged.)

System	Position	Area (m^2)	Resolution σ (μm)	Channels (10^6)	η coverage
Silicon strips	4 barrel layers	31	$R\phi = 15, z = 770$	2.3	± 1.4
Silicon strips	9 forward disks on each side	21	$R\phi = 15, R = 770$	1.6	1.4–2.5
GaAs	5 forward disks on each side	2.5	$R\phi = 10, R = 1200$	0.8	1.5–2.5

region. It can be seen that the resulting performance is uniform over the η range up to 2.0 and shows only a slow deterioration of the momentum resolution between $\eta = 2.0$ and $\eta = 2.5$.

The basic design parameters and hit resolutions summarized in Tables 1 & 2 correspond to designs with full tracking coverage over $\mid \eta \mid < 2.5$ and the capability of providing the required momentum measurements ($\sigma_{P_T}/P_T < 30\%$ at $P_T = 500$GeV, $\mid \eta \mid < 2$) and impact parameter resolution ($\sigma_{i.p.} = 27\mu\text{m} \oplus 220\mu\text{m}/P_T\sqrt{\sin\theta}$ for tagging decays of heavy quarks and τ leptons). Improved measurements of secondary vertices ($\sigma_{i.p.} = 13\mu\text{m} \oplus 62\mu\text{m}/P_T\sqrt{\sin\theta}$) will be possible during the initial lower luminosity running with the additional vertexing layer.

3.1 Precision Tracking

The inner detector must provide powerful track-finding and pattern-recognition performance, a sagitta resolution of ≤ 25 μm, a polar-angle resolution of < 2 mrad, and have good efficiency for tagging heavy quark decays. To cope with situations where straw tube information may be absent, such as in high-P_T jets, the other inner tracking elements must have a stand-alone track-finding efficiency in the region of 90%. The measurement precisions required per stereo hit, including the needs for detector alignment, are ≤ 20 μm in $R\phi$ and < 1 mm in z. These are well matched to the properties of silicon microstrip technology where resolutions of ≤ 10 μm are achieved in current collider experiments.

These detectors will be used to optimise the tracker performance within the basic guidelines of:

- minimizing the amount of material, compatible with providing the necessary number of space–points from devices with appropriate granularity and at a reasonable cost
- maintaining good track–finding ability, both at high luminosity and within jets at lower luminosity.

The design will ensure that over the entire η coverage of the inner detector, there are at least six high precision hits per track. Two of these will be space–points from pixel layers, with the outer four incorporating strip measurements from small-angle stereo devices. In the most forward regions there will be GaAs strip detectors. The combined system will provide excellent sagitta and $R - \phi$ vertexing with efficient pattern recognition and adequate three dimensional track reconstruction.

3.2 Semi-conductor Detectors

In total, approximately 10,000 single-sided silicon-strip detectors covering an area of about 40 m^2 are required for the outer layers of the barrel section shown in Fig. 7. This represents a 1–2 orders of magnitude increase in quantity over any existing silicon detector. The individual detector modules, of which nearly 3000 are required, will be constructed from pairs of single-sided devices mounted back-to-back with one pair giving $R\phi$ co-ordinates directly and the other being rotated by 40mrad. Electrically they will be configured such that the highest possible efficiency can be maintained even after severe irradiation.

To minimise the number of different components, all four cylindrical layers will be assembled from identical modules. In one possible assembly scheme now being prototyped 14 modules are mounted onto a support stave. Staves are then assembled into cylinders (see Figs. 8 and 9), where alternate cylinders are built of u–ϕ and v–ϕ layers.

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Figure 4: The *Morges* Integrated Semi-conductor Tracker Layout

3.2.1 Silicon Strip Detectors

The required performance of the inner tracker has led naturally to the choice of silicon-strip detectors. The read-out pitch of the ATLAS wafers will be determined by which technique is used to register the ionization signal produced in the silicon substrate. For front-end electronics capable only of binary registration a pitch of 75 μm is required, giving a total of 4.4 M read-out channels. If the analogue pulse height information can be registered, detectors designed to optimise charge sharing between strips allow an equivalent resolution to be readily obtained with a read-out pitch increased to 112.5 μm, corresponding to a total of 2.9 M read-out channels. Recent test-beam results [2], using both standard and radiation hardened prototype LHC analogue read-out, indicate that the required performance may be achieved using even larger read-out pitch (see table 3).

Of major practical importance for the use of silicon detectors within ATLAS is their behaviour after irradiation. The bulk damage will finally be dominated by *reverse annealing* effects. Whilst annealing effects help reduce the radiation induced leakage currents in the detector, reverse annealing increases the required depletion voltage after irradiation has stopped. Such effects can be greatly reduced by operating and maintaining the detector at low temperature throughout its lifetime, which also keeps the leakage current levels acceptable. Considerable advances have been made in understanding both bulk and surface-damage mechanisms [2], and device designs now exist which come close to the required specification.

The module strip length of 12 cm is determined by the charged particle occupancy expected at high luminos-

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Figure 5: Comparison of the Integrated Semi-conductor Tracker Momentum Resolution with the Technical Proposal Design at a P_T of 500GeV/c.

ity and by the capacitive load, rather than by the long-term leakage current. As can be seen from Fig. 10, the depletion voltage grows with irradiation, and the detectors need to be cooled below $0°C$ (see Fig. 11). Reducing the thickness of the detectors from 300 μm to 250 μm would further reduce the operating voltage, but at the expense of reduced signal to noise performance.

The continuing programme of detector prototyping falls within the three options agreed for further consideration by the ATLAS SCT collaboration:

- **Single-sided detectors with p^+ read-out implants.** These are the standard detectors used in current experiments and hence are the best understood. Under irradiation the effective doping concentration in the $n-$type substrate alters and eventually changes to $p-$type. After type inversion the junction moves to the other side of the detector and efficient charge collection requires the $\geq$200 V needed to deplete fully a highly irradiated detector. There is little experience operating at these voltages and modified guard structures, with possible additional lithography on the back side of the detector, are being investigated.

- **Single-sided detectors with n^+ read-out implants.** These detectors require additional processing steps — firstly to isolate the n+ strips and secondly to provide an adequate guard ring structure before type inversion. However, they offer the advantage of a faster signal through electron collection. They can also be operated in a partially-depleted mode after irradiation, and provide high charge collection efficiencies. This design is expected to offer the most robust solution in the LHC environment but at a

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Figure 6: Comparison of the Integrated Semi-conductor Tracker Number of Stereo Pairs with the Technical Proposal Layout. (The dashed lines show the individual contributions of the barrel and forward regions, indicating the extent of the transition region.)

higher anticipated cost than the more conventional p^+ read-out design.

- **Double-sided detectors.** The choice of double-sided detectors has an obvious advantage in reducing the total material per layer by 20% as well as reducing the heat load generated by the increased detector leakage currents after irradiation. Effectively it requires that the problems associated with both single-sided options be overcome. Additional problems in this solution arise from the difficulties of double-sided processing and from the fact that, for double-sided detectors, the read-out is at high potential on at least one side. If these difficulties can be overcome, cost will be the driving consideration.

Many groups, with prominent contributions from the UK, have already carried out detailed detector irradiation studies as part of a comprehensive programme that includes quantitative measurements that relate to the use of capacitive coupling, the implementation of various biasing techniques and the possible use of $p-$type (rather than $n-$type) bulk material. In addition, silicon detector suppliers are co-operating in providing estimates of device yield and hence cost. The technology choices will be finalized by the end of 1996 in order to be compatible with the timescales demanded by the project overall.

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Figure 7: ATLAS Barrel Semi-Conductor Tracker (SCT)

3.2.2 GaAs Strip Detectors

The increased levels of radiation in the most forward regions make the use of gallium arsenide detectors more appropriate for their instrumentation, where doses are expected to be in the range 10^{14} n cm^{-2} to $3 \cdot 10^{14}$ n cm^{-2}. It has been shown that Schottky-based GaAs detectors, when irradiated with neutron fluences up to 3×10^{14} n cm^{-2} and gamma radiation from ^{60}Co up to 1 MGy, show only $\sim 20\%$ decrease in the charge-collection efficiency and a small increase in noise, and maintain a signal to noise ratio of better than 10:1. Leakage current measurements give a value for α_n of $5 \cdot 10^{-19}$ A cm^{-1} (the coefficient of leakage-current-increase with fluence) at room temperature and the absence of type-inversion means that detectors can be operated at temperatures up to $\sim 20°C$.

The detectors will be made from commercially available four-inch diameter LEC-grown semi-insulating GaAs wafers. The wafers will be thinned to 200 μm to provide the best compromise between maximum signal and minimum material. There is a dead area of 0.9 mm around the edge of the detector, corresponding to 0.5 mm from the cutting and 0.4 mm from a guard structure, and there is an additional 500 μm at one end for the biasing structure. The detectors are single-sided and capacitively coupled to the electronics to avoid excessive leakage current being fed into the front-end electronics. The electronics can then be kept compatible with that for the silicon strips. One side of the detector will be patterned with Schottky metalization to give the sensing strips, a guard structure and a biasing-strip structure using a punch-through mechanism. There will be a silicon nitride passivation on top of this layer. The capacitive coupling will be achieved by using either external capacitor chips or intrinsic capacitors by reading out from strips on top of the silicon nitride passivation. On the other side there will be ohmic metalization. At the operating voltage of around 250 V, the leakage current density

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Figure 8: SCT Barrel Stave

will be in the region of 10 nA mm^{-2}.

3.3 On-detector Electronics

The progress in the development of fast radiation-hard electronics in the last few years has resulted in major advances in the design of the front-end(FE) electronics for the ATLAS inner tracker [1], [2]. However, a further year of studies is needed to carry out realistic system tests before establishing the final scheme. This will provide, by mid 1996, the necessary data in both performance and cost to allow the different architectures to be compared. The ATLAS precision tracker has approximately 5×10^6 channels of strip detectors. Each channel has its own amplifier and pipeline. Data will be stored in the pipeline during the 2 μs needed for the level-1 trigger decision. For accepted events the read-out will be multiplexed down optical fibres. There continue to be developments of both bi-polar and CMOS preamplifiers. Current results indicate that, given the length of the silicon strips in the ATLAS SCT (12 cm) with capacitance of around 18 pF, the best compromise in performance

Table 3: Resolution versus read-out pitch and S/N, measured in the ATLAS H8 test beam with prototype LHC analogue read-out electronics

read-out pitch	Signal-to-noise ratio			
	7	10	15	20
50μm		12μm		7μm
100μm	18μm	15μm	12μm	12μm
200μm	40μm		20μm	

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Figure 9: SCT Single Barrel Mechanics

between noise, speed and power will be achieved with bi-polar technology. The key requirements for the FE electronics are listed below and more details can be found in ref. [5]

- **Noise:** The electronics noise should be less than 1300-1500 e for in-situ operation, corresponding to a requirement of approximately $\leq 700e^- + 70e^-/pF$ ENC.
- **Dynamic Range:** A maximum signal of ~ 8 MIP should be recorded, requiring a resolution of 7 bits.
- **Level-1 triggers** will provide a maximum average rate of 100 KHz with a latency of 2 μs.
- **Power** per unit area of detector should be less than 40 mW/cm^2.

The three different architectures under consideration are

- **Binary** in which only hit/no-hit information is recorded.
- **Digital** in which sparsified digitised pulse-height information is transmitted off-detector.
- **Analogue** in which the pulse heights are transmitted off-detector as analogue voltages.

These options are discussed further in the following section.

3.3.1 Front-end Architectures

3.3.1.1 Analogue

This architecture allows the greatest flexibility in signal processing, which is done off-detector, and is particularly necessary if the coherent noise components (*eg* electrical pick-up) are large. However, it does require significantly more fibre links and is more demanding in the off-detector data processing than the other options. Prototypes of the analogue FE chips with 32 channels have been fabricated in both radiation-hard CMOS by Harris (the APV3) and in non-hardened CMOS by AMS (the FElix). Both were tested successfully in a CERN test beam in 1994 and gave signal:noise values of $> 10 : 1$.

Fig. 12 shows that these values are already sufficient for maintaining an efficiency above 99% with a rate of noise hits well below 1%.

These tests also demonstrated that charge division could be used with LHC speed electronics to obtain a resolution significantly better than strip pitch/$\sqrt{12}$ [2]. During 1995 a 128-channel version which includes a 40 MHz multiplexer, APV5, will be operated together with analogue optical links in the CERN H8 test beam.

3.3.1.2 Digital

This solution has the advantage of retaining pulse height information while being less expensive than the analogue option. Prototypes of digital chips, without sparsification, have already been fabricated and successfully tested. The ATLAS groups are working on a digital read out chip, AROW, which uses a sparsification scheme based on the SVXII chip developed for CDF. This scheme is illustrated in Fig. 13.

Each channel has an individual discriminator and ADC that allow simultaneous digitisations to be made of all channels. Those channels above a given threshold (and optionally their neighbours) are flagged as valid and are read out, with channel offsets (pedestals) being removed digitally on the chip. A radiation soft version of the AROW chip will be submitted for fabrication in September.

3.3.1.3 Binary

This option is currently the most advanced. In Fig. 12 results from test beam measurements at KEK show that the binary option can achieve an efficiency well above 99% with the fraction of noise hits below 0.01%. A fully functional data-driven pipeline chip was developed by UK groups for the SDC experiment and shown to operate correctly. A clock driven binary pipeline chip is now being developed for ATLAS so that high efficiency can be maintained with the largest possible occupancies.

3.4 Optical Links

3.4.1 Data Transmission

The data transmission system combines the use of a highly parallel read-out with additional fail-safe principles that ensure that the possible loss of an individual element occurs in isolation with no cascading effect. This is essential for a large system required to run for many years with minimal maintenance. For the analogue option each FE chip is read out by an independent fibre optic link, whereas for the digital (binary) option one fibre link will read out a module with 4(6) FE chips. The FE chips are connected serially, but with a bypass scheme, such that the failure of one chip does not inhibit the read-out of the remainder. The data are read out via a control and monitoring chip, MONROC. If a MONROC chip or a fibre link fails the data can be rerouted via the MONROC chip on the other side of the module. The technologies being considered for the optical links are Multi Quantum Wells (MQWs) and light emitting diodes (LEDs). They are described briefly here and further details are available in [2].

- **MQWs.** The MQW device transmits data by modulating the amount of light reflected back along a fibre which delivers light from a laser on the read-out card in the counting room.
- **LEDs.** The electrical-to-optical conversion is done by a radiation-hard LED on the detector. The light is transferred to the counting room by a fibre where it is received by a PIN diode.

The MQW modulators are passive devices, expected to be radiation hard, and have the advantage of dissipating little power. The LEDs have also been shown to be sufficiently radiation-hard and to have a good lifetime after irradiation. The power consumption of LEDs in a digital application is up to 100μW/channel; in an analogue system, up to $200\mu W$/channel would be needed. Both technologies are being pursued, with more current knowledge of both performance and cost being available for the more mature LED option.

3.4.2 Timing, Trigger and Control Distribution (TTC)

The TTC system is principally required to distribute the following information to all front-end modules:

- The 40 MHz bunch-crossing (BC) clock, with a pulse-to-pulse jitter of less than ± 0.5 ns and a drift rate of less than 1 ns/hour.
- The synchronous level-1 trigger-accept signal.

- Control information of two types : fast control for global and bunch-counter resets, and slow control to provide the set-up information and operate the front-end chips.

The trigger signal, clock and control data from the central trigger system are sent to interface modules using the ATLAS TTC system. These interfaces fan out the data and send it to individual detector modules.

A possible use in ATLAS, based on LEDs, for the links from the interfaces to the detector modules is described in [6]. Pulse-height modulation (PHM) encodes the control data on to the 40 MHz clock, and the data are sent down multi-mode fibres to the front end modules. A feedback loop is then used to set the amplitudes of the light pulses.

3.4.3 Packaging

One low mass package will contain two LEDs and one PIN diode and be needed for each double-sided module. The package will also contain two LED drivers and one PIN diode receiver plus amplifier and the two level discriminator of the DORIC chip (see section 4.6). This will allow the separate clock and control information to be recovered.

3.5 Off-detector Electronics

The off-detector electronics will convert the optical signal to an electrical signal and store the data in a buffer. The data will then be transferred to a standard ATLAS level-2 buffer. For the analogue option the analogue voltages will be digitised and processed. The system will be able to perform fast analysis of all the received data in order to detect and flag serious error conditions.

3.5.1 Data Receiver Modules

In the case of the binary or the digital options the data receiver modules consist of up to 128 channels of PIN diodes plus amplifier/discriminators. An ASIC chip resynchronises the data to the local clock. The data are stored in a local buffer before being transferred to an ATLAS level-2 buffer.

In the analogue scheme, the data reduction is performed off-detector using digital signal processing. The system is based on two modules, the Atlas Optical read-out Module (AROMA) and the Front End Optical Driver Module, the former processing all the data and the latter providing the control signals for the silicon modules. Both modules interface to the data acquisition and global timing systems.

AROMA receives one input from each read-out chip as a stream of serial analogue data on optical fibre. This is digitised by a fast ADC before being passed to the synchronization detection circuitry which identifies the start of each frame. This allows analogue and control information to be separated. In the next digital processing stage headers are added to identify the data and corrections are made for baseline shifts. The processed data are then collected into a single packet by the Local Event Builder for transmission to the data acquisition. Phase adjustment will be incorporated to allow each of the analogue signals to be sampled correctly as the ATLAS global timing system will be used to distribute the 40MHz clock to all the ADCs.

3.5.2 Data Monitoring

Local monitoring of all data accepted by level-1 will detect any errors quickly and issue the appropriate resets. Continuous monitoring of hit maps will provide the information for updating bad channel masks.

3.6 Silicon Strip Modules

3.6.1 Barrel Modules

There are currently two module options under study. One, the **Z–module**, has read-out electronics beside the detectors, distributed along the z axis of the barrel (Fig. 8 and 14), while the other, the **Rϕ module**, has them on top of the detectors, distributed in the azimuthal direction. Although the module designs are linked to aspects of the mechanical support schemes it would be practical to incorporate either of them into the final system after deciding which is preferred on the basis of technical and performance criteria.

One module is made of two (four) 6 cm $\times$ 6 cm double- (single-) sided silicon microstrip detectors as illustrated in Fig. 14. In the double-sided case the two detectors are to be butt glued to form a 12 cm long mechanical unit and strips of the two detectors are electrically connected to form 12 cm long strips. In the single-sided case, the butt gluing is followed by a back to back attachment. One side of the module measures ϕ (the **axial strips**) while the other side is rotated by the small stereo angle of 40 mrad (the **stereo strips**).

The area of 6 cm $\times$ 6 cm is the maximum that can be fabricated in a standard 300 μm thick, 4 inch silicon wafer. The electronics is connected via beryllia or diamond fan-ins to the detector strips and is cooled through contacts on the hybrid to the coolant system. Services to the electronics are supplied on the hybrid which also interfaces to the optoelectronic board.

3.6.2 Forward Modules

Fan-shaped detectors of 12 cm length can be provided by either bonding together two 6 cm long detectors from 4 inch diameter silicon wafers or using a single device cut from a 6 inch diameter wafer. The proposed design is based on that used in the barrel but with read-out at one end of the module. A ϕ detector and a detector with a small stereo angle of 40 mrad are glued back-to-back onto a thin beryllia or diamond substrate which provides both rigidity and a path for heat conduction. A double-sided alumina hybrid is connected to the detectors by means of beryllia fan-ins which again provide rigidity and a path for heat conduction. This arrangement is shown in Fig. 15 and assumes that there will be 512 channels per detector with digital or analogue read-out.

3.7 Gallium Arsenide Strip Modules

A module will consist of two detectors, one with radial strips and the other with strips inclined at a small stereo angle. The two detectors will each be bonded to the read-out hybrid with the electronics, as used for the silicon detectors, placed at the outermost radii in order to minimise radiation dose.

3.8 Mechanics for the Semi-conductor Tracker

The engineering requirements of the barrel are to:

- Support 2 layers of pixel and 4 layers of silicon detectors with a stability at the 10 μm level in $R\phi$, at constant temperature.
- Use long radiation length and radiation hard materials in the construction of the detector.
- Remove up to 30 kW of heat generated by local electronics and irradiated detectors by using a unified fluid-cooling system. The pixels and silicon detectors operate below a temperature of 0 $°C$ with a stability of better than $1°C$. The TRT operates at the detector ambient temperature of $\sim$ 20 $°C$. A thermally-insulating enclosure, with a flow of cold dry nitrogen, will be required around the pixel and silicon detectors to prevent condensation.
- Provide services to and from the detectors, and the multiplexed read-out from millions of channels.
- Ensure that the services, alignment systems and supports do not adversely affect the stability of the supporting structure.

Two approaches to the support structure for the silicon strips are being pursued (see Figs. 7 and 9). In the first, beryllium staves, with built-in cooling channels, are used as the main structural element. Silicon modules are mounted directly onto the binary-ice cooled staves, which results in short thermal paths from the front-end electronics to the coolant (Fig. 8). The staves are then inter-connected using rings and a space-frame structure. This structure must accommodate movements of up 0.5 mm in the z direction, due to temperature changes.

Despite handling difficulties due to its toxicity, beryllium offers a number of key advantages. It is regularly used in space and defence equipment due to its high dimensional stability, reproducibility under thermal cycling and good thermal conductivity. It also offers a long radiation length with established radiation hardness.

The alternative scheme is based on the use of carbon-fibre composite cylinders constructed to have a zero coefficient of thermal expansion. In this case the cooling pipes are clipped into place, but allowed to move in z, avoiding transmission of thermal strain to the silicon modules. Thermal contact is maintained using a heat-sink compound. The cylinder material is likely to be cyanate ester resin with ultra-high modulus carbon-fibre skins and either nomex or carbon-fibre core. The effects of humidity and the dimensional stability of this structure still require further study.

The assembly will proceed in several steps. The details depend on which design of macroscopic support structure is selected. In the case of the barrel stave design, the procedure involves four basic steps, at each stage of which extensive testing and survey are required.

- Firstly modules are assembled using conventional optical alignment techniques and precision jigs. At this stage exhaustive electrical testing is performed.
- In the second phase, fourteen modules are attached to each stave, again using standard precision assembly methods and jigs. This and subsequent phases must take place in a temperature controlled environment. Cables, cooling and fibre optics are attached, producing a complete stave structure.
- The third step involves attaching the stave structures to the space-frame to form barrels. The staves are manoeuvered into position semi-robotically, with the exact location found using an FSI alignment grid (section 4.4).
- Final assembly of barrels into the complete detector can then take place in the ATLAS surface experimental hall.

For the assembly, the tolerances have a preliminary specification of better than 100 μm in $R\phi$, 250μm in R and 500μm in z. This is based mainly on the requirements of the level-2 trigger. After assembly, a survey (if possible at the temperature of operation) will locate each silicon module within a barrel with a precision of 25 μm, to ensure no ambiguity in strip locations. The final required alignment will be achieved using tracks as all modules are overlapped both in z and ϕ. A complete study of the effect on physics of changes in these resolutions is underway.

The detectors will be tested at each stage of assembly: component, module, stave assembly, cylinder assembly, and as interlinked cylinders. The pixel and silicon cylinders are interlinked by end structures to one another and are supported by the TRT barrel, which is in turn supported by a rail system.

The support system proposed for silicon detectors in the forward region will be based on a carbon fibre space frame. A preliminary design, Fig. 16, shows the mounting of 2 silicon rings with provision for the GaAs at closer radius. The detectors in a ring are overlapped in ϕ and the different rings overlap in z. The discs will be connected together with carbon fibre struts to form a forward detector module. One critical area of further study for all mechanics designs is the thermal connection between the cooling pipe and the alumina hybrid. Work on this will continue in parallel with the layout developments.

3.9 MSGC Tracking

3.9.1 Layout

The Technical Proposal layout for the forward region provides high precision measurements at low radius using MSGCs (Fig 3). The MSGC detectors are arranged in wheels, each containing three layers of detectors. In one of the layers, ϕ, the strips run radially in a keystone geometry; the other two layers (u, v) have strips rotated by $\pm 1°$ to give stereo information, and hence a radial measurement.

The outer radius of the active area of the MSGCs is limited to 60 cm by requirements for the surrounding TRT continuous tracking. The inner radius is a compromise between occupancy and channel count; an inner radius of 44 cm allows the active radius to be spanned by a single ring of 16 cm tiles, compatible with current substrate production facilities.

The number and position of the MSGC wheels is determined by the requirement for 6 precision points over the full η range, leading to 4 MSGC points and 2 from the pixel detectors. The current positions and η coverage are given in Tables 1 and 4.

3.9.1.1 Specification of MSGC module

The choice of the substrate, gas and read-out electronics are still to be finalised, but baseline decisions have been made and are presented in [22].

The substrate will be the slightly conductive glass S-8900, cut into a plate of less than 0.4 mm thickness, giving an effective surface resistivity of $10^{13}\Omega/\Box$. The pattern of gold electrodes deposited on the substrate will have a “keystone” design with an average pitch of 200 μm, the widths of the anode and cathode strips will be 10 μm and 70 μm respectively. With a strip length of 16 cm this design gives an acceptably low anode capacitance of 10 pF.

The 2.5 mm drift space will be filled with a 50:50 mixture of Argon and Dimethyl Ether (DME). This combination of gases is found to be resistant to ageing and the high fraction of DME gives it a high ionisation density of 12 electrons per mm and an adequate drift velocity of 50 μm ns^{-1} The chamber will be operated with a drift field of 500 V/mm and a cathode voltage of around 650 V, giving it a gain of 3000. With these parameters the charge collected on the anodes in each year of full luminosity LHC running will be 6 mC/cm.

Table 4: The Geometrical Parameters of the ATLAS Technical Proposal layout with MSGCs.

System	Barrel radii and half-lengths (cm)	Forward z positions and radial ranges (cm)	Element size (μm)
Pixels	R: 11.5, 16.5 $l/2$: 35, 45	 z: 50, 55, 80, 85 ΔR: 11.5–21.3	50×300
Silicon strips	R: 30, 40, 50, 60 $l/2$: ± 82		75 or 112.5 12 cm length
GaAs strips		z: 155.7, ΔR: 20–35 z: 182.5, ΔR: 29–44	50 7.6 cm length
MSGC		z: 90.0, 97.2, 104.3, 118.7 128.5, 138.2, 148.0, 157.7 171.1, 184.5, 197.8, 265.6 ΔR: 44–60 z: 336.0, ΔR: 50–96	200 16 cm length
TRT	64 80 cm straws ΔR: 63–107	z: 80–265, ΔR: 64–103 z: 267–327, ΔR: 50–103	4 mm diameter 39, 53 cm length

3.9.1.2 Mechanics

The MSGC part of the inner tracker consists of two symmetric halves in the forward and backward regions. Currently each half is composed of 12 small wheels and a single full wheel. The full wheel contains 3 concentric rings of detector modules, with the small wheel containing a single ring. A sketch of the $uv\phi$ detector module is shown in Fig. 17, and the support structure in Fig. 18.

Two mechanical structures are being considered for the MSGC wheels. In the *open module* scheme, the detectors and electronics are housed inside a single gas volume in a design that minimises material and dead space between modules. In the *closed module* design, each unit has an individual enclosed gas volume which would enable maximum levels of cleanliness to be ensured, if this were necessary for maintaining detector lifetime.

To provide a highly stable structure, the disc is constructed from a core of 9.5mm Nomex honeycomb sandwiched between 0.25mm carbon/epoxy facings to form a structure having a very high stiffness to weight ratio and a low coefficient of extension with respect to both humidity and temperature. The coefficient of thermal expansion has been estimated to be of order $3 - 5\mu\mathrm{m\ m^{-1}K^{-1}}$.

The proposed alignment system is a compromise between the achievable engineering stability and the desired resolution for physics. Assembly will be made at the millimetre level with subsequent measurement of fiducial marks on the MSGC substrates to about 10μm with respect to the reference points on the wheels. A reference grid is proposed for the continuous monitoring of the alignment. Alignment technologies under discussion [22] are frequency scan interferometry for longitudinal distances, and straightness monitors for displacement transverse to the line of sight.

3.9.1.3 Electronics and Read-out

The guiding principle in the design of the MSGC read-out is to obtain the highest efficiency for recording genuine tracks with minimum fake tracks and dead-time. It is also important to identify the bunch crossing in which the event occurred (BCO tagging).

The module specifications were chosen so that the maximum drift time of electrons in the gas will be 50 ns (two bunch crossings). A fast integrating amplifier with a 15 ns rise time and a fall time of about 500 ns is proposed to read out the anode signal. Double correlated sampling will be used to subtract (at each beam crossing) the signal at (t–50)ns from that at t to maximise the collection of avalanche charge. These subtracted signals will be stored in a pipeline during the level-1 trigger latency. Read-out may then be either a binary yes/no for each channel or an analogue value.

In order to investigate and compare the properties of the read-out schemes, a detailed simulation has been made of the anode signal, including the motions of both electrons and ions in the chamber. The model used the track densities anticipated at the LHC, including low-P_T and looping tracks. This study shows [22] that the efficiency per plane for detecting a high-P_T track is better than 98%, with a resolution of 31-37μm, when the track density is low. At full luminosity, with ten times the track density, the efficiency drops to 92% per plane and the resolution worsens to 35-42μm. The measured efficiency for looping tracks is very low. The channel occupancy at high luminosity is expected to be below 2%.

The first stage of the read-out electronics will be specially adapted for MSGCs because of the need to integrate the signal for 50 ns. However, the pipeline and all later stages of the read-out chain will be identical to that used for the semi–conductor strip tracker.

3.10 Vertex Detector

The vertexing capabilities of the inner detector can be enhanced by the addition of a precision vertexing layer at the minimum practical radius. A concept based on the use of double-sided silicon strip detectors has been developed [24] in order to keep the material to the minimum possible level. The developments required (over and above the general SCT program) to prove the viability of such a detector are :

- Radiation tolerant double-sided detectors with a routing layer to keep the electronics at large z.
- Analogue front-end electronics matched to the high capacitance associated with daisy-chaining 4 detectors.
- Mechanical design of 52cm long modules.

4 UK Areas of Activity within the Inner Detector

4.1 Introduction

It is the intention of the UK groups to take responsibility for final prototyping and construction of major parts of the ATLAS precision tracking; specifically in the areas of silicon modules in the barrel, GaAs forward wheels, a microstrip inner precision layer, overall mechanics, cooling and alignment, off-detector electronics and associated DAQ, and either silicon modules or MSGCs in the forward region, whichever technology is chosen.

To this end the groups began active LHC detector development programmes several years ago, beginning with the first of the CERN DRDC initiatives. The prototyping activities in ATLAS culminate in the construction of a full sector of the inner detector, planned for the period 1996-98.

4.2 The Tracker Sector Prototype Programme

4.2.1 Overview

A significant milestone towards establishing the full operational viability of the proposed inner tracking detector for ATLAS will be the successful construction and testing of a prototype sector of the complete system. This target was proposed and subsequently detailed by the UK ATLAS groups, who are playing a major part in ensuring that it can be implemented.

The performance objectives for the Tracker Sector Prototype (TSP), which for the barrel will cover approximately thirty degrees in azimuth and correspond in length to approximately one half of the final system, are given below. It will be operated in the H8 beam at CERN in a programme that spans the years 1996 to 1998, with the option of having at least parts of the sector in a 1.8T magnetic field.

As discussed above, various options for mechanical and electronic sub–components are already under active study. Results obtained during 1995, from both laboratory and test beam work, will allow the construction of many of the items needed for the TSP. These items will include major mechanical structures as well as optimized detector modules, their electronic read-out and data acquisition. The central aims relate to the specifications and objectives required for the final pixel, silicon microstrip and transition radiation trackers (TRT), which together will form the inner tracking of ATLAS.

The successful integration of all aspects of the inner tracking scheme into a proven unified system is seen by the UK groups to be of the highest priority.

4.2.2 The Main Objectives of the Tracker Sector Prototype

As well as verifying the basic performance characteristics of the tracking devices there are specific physics requirements that must be met by the data recorded in the TSP programme. These include momentum resolution, pattern recognition and vertex reconstruction. System aspects, such as alignment, mechanical stability and operational efficiency under realistic conditions (with all components powered and running) must also be demonstrated within the programme. Some further details on these topics relate to studying :

- the momentum resolution for electrons with the sector operated in the magnetic field (in front of the electromagnetic calorimeter module), with all layers equipped with active devices, and a realistic distribution of passive support and structural material.
- pattern recognition within hadronic jets, and the reconstruction of both primary and secondary vertices, requiring the use of a thin foil target.
- various installation and operational issues :
  - Assembly and mounting procedures
  - Operation at temperatures close to 0^0C
  - Detector alignment
  - Supplying services without introducing stresses and deformations
  - Maintenance and access procedures
  - Evaluation of electronics system performance
  - Read-out and trigger studies
  - Synchronization, control and monitoring of the overall detector system

There will also be additional engineering prototypes to complement the understanding of questions relating to structural behaviour.

The areas of specific UK ATLAS responsibilities are centered on all aspects of the silicon and gallium arsenide tracking systems and the mechanics, cooling and alignment. The UK groups are also involved more widely in general test-beam infrastructure, the overall data acquisition system and off-line data analysis.

4.2.3 The Timetable of TSP Activities

It is planned that the design and construction of the mechanical support for the full sector will begin in 1996, and in 1997 it will be partially equipped with radiation tolerant strip semiconductor tracking modules, built to the final design, and with a TRT module. The full prototype, including the SCT pixel devices and about 50 strip modules, some irradiated, would be tested in the H8 beam in 1998, taking combined data with the ATLAS calorimeter prototype.

4.3 Engineering

The UK is well placed to provide a major contribution to the engineering studies and subsequent construction phase of the ATLAS inner detector. This will build on the extensive investment of UK engineering expertise that has already been fundamental to establishing the current design.

Of particular importance is the work on both stave and composite barrel solutions for the overall SCT structure. Extensive stress and thermal finite-element analyses have been carried out in the UK for both designs. However, full-scale prototyping, with significant UK participation, will be needed to provide the information on which a final choice will be based. Discussions with industry are now well advanced regarding the manufacture of the beryllium staves using an extrusion technique. Aluminium prototypes have already been delivered and the beryllium prototypes are anticipated in 1996. A similar programme with the composite solution must also be anticipated, particularly as this technology is the expected choice for the forward support structure.

For the carbon fibre composite structures, prototypes will be required to address questions of moisture absorption and stability, and to assess the viability of the proposed schemes for mounting and contacting the cooling channels.

4.4 Alignment

The UK intends to take a major role in the assembly of the SCT modules within the detector and is proposing to have sole financial responsibility for alignment. A definitive alignment strategy is under development for use in initial construction, both at sub-component and assembly level and subsequently to monitor the overall working structure within ATLAS.

In order to quantify the requirements the following programme of work is proposed :

- building a full scale, thermally similar, model of a complete barrel of the detector
- operating this barrel under observation with an Electronic Speckle Pattern Interferometer(ESPI) to determine its motions
- making measurements that allow the detector to be separated into logical blocks, each capable of finding at least crude track elements
- equipping the final barrels with an active survey system capable of locating each strip within a block relative to the other strips in the same block without the need for tracks
- and finally locating blocks relative to each other using tracks.

The active survey system for use in such a strategy would need to have the same precision as that required in the final survey.

4.4.1 Alignment Techniques

There are many methods for measuring the distance between objects. Most determine variations rather than absolute distance. Calibration is often required, as in the cases of the capacitance measurements to a taught wire, motion of a glass target ball relative to a fibre light delivery/return bundle or the motion of an LED relative to a PIN diode. There are at least two techniques that could provide absolute measurement. The technique being developed in the UK is Frequency Scan Interferometry (FSI). FSI measures the distance between the end of an optical fibre and a (mm dimensioned) corner cube target. FSI has several attractive features and is the scheme proposed to be used in ATLAS. The FSI method measures only lengths. Rotations must be inferred from multiple measurements using triangulation. FSI has the following features, which make it appropriate for use in the strategy outlined above:

- precision of 1μm (necessary because accuracy is lost during triangulation)
- very low mass
- low cost per measurement (many tens or hundreds required)
- correct operation not dependent on continuous monitoring
- small physical size
- radiation-hard and robust system.

A complex optical system is required to extract the length measurement, but this can be done at the end of a long fibre, probably in the counting room.

The incremental cost per measurement within a relevant system is roughly the cost of two optical fibres and a small corner cube. These corner cubes (external, made from silicon wafers) would be fabricated in one of the UK universities. The low incremental cost and the low mass associated with the corner cube makes practical many hundreds of measurements.

In a scanned frequency interferometer, the light modulations that result from scanning the laser frequency are counted at the receiver. The starting and ending wavelengths, λ_1,λ_2, coupled with a count of the number of oscillations, δ, can be translated into a length measurement, with the optical path distance, D, from the beam splitter to the reflector given by

$$D = \frac{\lambda_1 \lambda_2 \delta}{\lambda_2 - \lambda_1}$$

Methods to overcome the technical difficulties associated with frequency scanned interferometers have been devised, and a demonstration system assembled. Fig. 19 is a diagram showing all the elements required for a real system. All the more complex instrumentation is external to the detector.

Interferometers have been made to work at the end of 100 m of fibre. The interference can be seen with a wide range of target distances and angles relative to the fibres. The next major demonstration must be of a length measurement via frequency scan. In order to make a length measurement with the accuracy required in the final system it would be necessary to buy a Ti Sapphire laser. The purchase of such an expensive laser will be delayed until a proof of principle demonstration is achieved using a semiconductor laser during 1995.

4.4.2 Large Aperture ESPI

ESPI provides a convenient way of measuring real time motions of a full size SCT with a precision of better than 1μm. The principle is illustrated in Fig. 21. Laser light reflected from the target and light reflected from the mirror are made to interfere. The resulting intensity is recorded with a CCD camera. The difference in intensities between two frames gives a series of fringes which provide a measure of the motion of the target between the two frames. This is an industry standard technique. ESPI has already been demonstrated in an ATLAS application by a UK group where the distortion of a silicon detector when cooled was measured. The resulting fringe pattern is shown in Fig. 20.

ESPI will be used to measure the distortions of individual SCT modules when power and cooling are applied, and will also be used to study the distortions of an aluminium prototype of the barrel stave structure under mechanical and thermal loads. These measurements will be critical for verifying FEA calculations.

4.5 Cooling

The cooling of the inner detector semi-conductor tracker will be based upon UK work on the development of a Binary-Ice system. This technique utilises the latent heat of fusion of water to provide a high capacity, fluid coolant that displays essentially isothermal operation. The coolant is an aqueous solution of a freezing point depressant which is chilled by a commercial freon refrigerator. As the temperature of the liquid reaches its freezing point, crystals of ice nucleate on the cooled surfaces of the refrigerator and are removed by a motor driven scraper running inside the ice generator. A suspension of microscopic ice crystals is thus formed and this slurry is then pumped through the cooling tubes of the detector. As the heat generated by the front-end electronics and detector modules is removed, the ice concentration decreases with only a minute rise in fluid temperature.

Work on this area of research started about 2 years ago with a series of tests being carried out at Integral Technologie GmbH, in Germany. The results of these initial tests were sufficiently encouraging to warrant the purchase of a small, 1.7 kW, prototype machine. This was a one-off device, built to a specification defined by members of the UK ATLAS community. The device was delivered and installed at Rutherford Laboratory in early 1994 and has now been tested extensively. Details of the performance of the system have been published elsewhere[11],[12].

Additional hardware has been designed and built to permit testing of mechanical interlinks, detector modules and prototype assemblies in an ATLAS-like environment. An insulated, temperature and humidity controlled enclosure has been built to simulate the conditions likely to exist within the ATLAS inner tracker ($< 30\%$ RH and temperature between $-10°C$ and $1°C$). Measurements of fluid flows, temperatures, pressures and ice concentration are made in a separate test system.

Further R&D on the proposed cooling solution is still needed. At present, the freezing point depressant used for the Binary-Ice is 1,2-propane diol (propylene glycol), which has a melting point of $-60°C$. By varying the mixture from 0% to 50%, by weight, operating temperatures of between $0°C$ and $-24°C$ are possible. In the near future this solute will be changed to ethanol (ethyl alcohol). The reasons for this are (a) to allow a greater range of operating temperatures ($0°C$ to $-41°C$ for 0% to 50% by volume), (b) to use a mixture for which detailed results are available on the radiation induced breakdown of the solution and (c) because evidence is now available that long term chemical decomposition can occur with water/ 1,2-propane diol solutions.

A data acquisition and slow control system is being written which will operate all the controls of the ice generator, fluid monitoring apparatus and gas cooler/dehumidifier plant, providing the possibility of fully remote operation which is foreseen as a primary milestone for this cooling scheme. Furthermore, the programme will permit the automatic collection of data on detector module heat flows, mechanical displacements, fluid parameters and system reliability. A series of alarm levels and shut-down procedures will also be included within the programme. It is planned to complete all the system development by the end of 1995.

If the above tests provide satisfactory results, it is planned that the UK would contribute towards a second Binary-Ice system which would be of sufficient capacity to be used as one of the final two machines installed at ATLAS. This device would be controlled under the same operating system as the prototype machine and could be used in the test beam and in the UK for developing the alignment system for the SCT.

4.6 Barrel Silicon Strip Detector Module

All UK groups from the SCT project are participating in the preparation and running of the beam tests at CERN in the summer of 1995. The goals for the silicon strip activities are centered around studies on new UK detectors that will use the APV5 read-out chips recently fabricated by Harris, with a full analogue read-out chain. The 1995 activities represent the first comprehensive studies of full-scale silicon strip modules with radiation-hard fast electronics and detectors designed to meet the ATLAS specifications. These investigations will also start to provide system tests which will be extended as the full Tracker Sector Prototype programme evolves.

Work in the UK has concentrated on designs for the Z–module, with the hybrid attached beside the detectors (Fig. 14). The cooling runs along the hybrid in z and makes contacts between the read-out chips. The front–end electronics and silicon strips are interconnected by beryllia (or CVD diamond) fan–ins which also serve to cool the detectors. Detectors are either back-to-back single-sided or double-sided. The hybrid supports the front–end electronics and provides the control, read-out and bias lines. The front–end chips are mounted on both sides of the hybrid.

This design has the advantage of decoupling the front–end electronics, electrically and thermally, from the silicon, and of providing short cooling paths from the detectors.

Groups within the UK have been responsible for the design, simulation, prototyping and testing of detectors, frontend ASICs, hybrids, fan-ins, support and cooling schemes for these modules. As described below, development programmes have been undertaken with Micron Semiconductor Ltd to establish a fabrication process for the production of radiation resistant detectors based on both p and $n-$type bulk silicon. A parallel programme of electronic development has also been followed which has culminated in the 128 channel, radiation-hard APV5 chip, due to be tested on the prototype modules this summer. Fan-ins with fine lithography metal tracks have been developed on ceramic and diamond substrates and UK designed double-sided multi-layer hybrids have been fabricated.

At present there is a complete design of module layout and assembly, and a scheme to integrate this with the necessary support and cooling structures is well advanced. Finite element analyses (FEA) have been performed on both the module and support structures to evaluate thermal and structural performance and to assess the magnitude of thermally induced distortions, stresses and deformations due to static and vibrational loads. Direct measurements to verify the FEA simulation are being made on all components of a pseudo-final ATLAS module. Within these thermal models active devices will be powered and cooled to simulate true running conditions within ATLAS.

Detailed information will be obtained from the fully operational modules to be used in the H8 test beam this summer. This work is providing valuable experience within the UK community on the assembly and testing procedures required for constructing final modules, thus establishing the UK as one of the principal international centres for the construction of the SCT modules.

The UK work towards the module components is summarised below.

4.6.1 Silicon Detectors

The UK groups have been particularly active in developing new device designs that combine good performance with affordable cost. These are based on using the long established principle of capacitive charge division[10] as incorporated in all the LEP silicon microvertex designs. By using detectors with intermediate strips (biassed to the same potential as the read-out strips through a high impedance) typical precisions of $\sim$ pitch/10, compared with the pitch/$\sqrt{12}$ expected for binary read-out, are readily achieved with moderate signal to noise performance (see Table 3). Whereas in LEP experiments the motivation is to achieve the best possible resolution for a given read-out pitch (typically 5μm with a 50μm pitch limited by inputs to the high density read-out electronics), for the SCT the motivation is to retain a precision of better than 20μm while minimising the number of channels and the overall cost.

The general objectives within RD2, RD20 and for SDC centred on improving the robustness of devices in designs where all implant strips were read out. In contrast the UK groups, with ATLAS collaborators, have concentrated on demonstrating that charge division can be used to provide designs optimised for a given precision with a minimal number of read out channels. This programme has required the UK groups to design and fabricate capacitively coupled detectors with differing strip and read-out pitch and new guard ring structures.

In association with this work RAL engineers designed the radiation-hard APV3 chip within the RD20 programme. This was used successfully by ATLAS UK groups in H8 beam tests at CERN in 1994. At LHC speeds and with moderate signal to noise this early electronics iteration gave the analogue information of the strip pulse heights and using enhanced charge sharing from intermediate strips interpolation techniques resulted in precisions approaching pitch/10 even up to 150μm read-out pitch (Fig. 22).

In 1994 much of the UK activity was associated with preparation and running of the H8 beam tests, and the subsequent offline analyses of data. This groundwork will now provide a solid base for the entire ATLAS track-detector prototype work for the coming few years, which will continue with beam tests in H8.

The UK groups provided the precision mechanics for the silicon telescope ($\pm 2\mu$m track extrapolation), the on-detector electronics and buffers, the voltage supply and monitoring, much of the DAQ and almost all the subsequent analysis. The detectors were designed in the UK and fabricated by Micron Semiconductors Ltd and both the detectors specific to this study, and earlier Micron detector designs employing polysilicon biasing (for UK RD20 groups) were tested using APV3 and the non-radiation hard FElix LHC electronics from Oslo. The overall ATLAS detector specifications which were formulated in the UK during 1994 relied heavily on these studies, and details are given in [1] and [2]. If the analogue or digital read-out schemes are adopted, the ATLAS detectors will incorporate intermediate strips to linearise the charge division and have a read-out pitch of 112.5μm to achieve the necessary precision when formed into a back-to-back module with active area per side of 6cm by 12cm.

The barrel module silicon detectors for use in the H8 test beam in 1995 have again been designed in the UK and fabricated by Micron Semiconductor Ltd. The designs draw heavily on the experience gained in the RD2 and RD20 collaborations and are adapted from designs for microstrip detectors developed by ATLAS UK groups within RD20 (following a lengthy prototyping procedure which resulted in large area double-sided detectors being fabricated, again in the UK). The detectors are based on n^+-strip read-out with $n-$substrate and employ $p-$stop isolation, polysilicon resistor biassing, multi-guard-rings and $p-$side photolithography for pre-inversion operation. The mask layout for the full-sized 6×6cm detector is shown in Fig. 23 which has the diagonal row of bond pads needed for connection to the z-module fan-ins (Fig. 14).

Whilst these detectors represent the most robust design based on current knowledge further studies are required to optimise the design. The specific areas of high-voltage operation, $p-$substrate processing and guard ring optimization are under investigation in collaboration with Micron Semiconductor Ltd, sponsored by PPARC through the PIPSS initiative and a CASE studentship.

4.6.2 Hybrids

The final hybrid design will evolve from the work on double-sided ceramics for the 1995 UK test beam modules. Currently these hybrids provide routing between the amplifier chips and give external connections to a board that emulates the functionality of what will become the on-detector control electronics. The hybrids have been designed in the UK using extensive experience from the DELPHI experiment and require multi-layer thick-film processing with track width/gaps down to 75μm. Beryllia hybrids and aluminium tracking are being pursued as options for the final design.

4.6.3 Electronics and DAQ

The UK groups have been active in all three options for the FE electronics (analogue, digital and binary), as well as those needed for use off-detector. RAL Electronics designed the prototype analogue chips, APV3 and APV5, and collaborated in the design of prototype digital chips, APC3, APC3-RH and ADAM. The UK collaborated with CERN and Geneva on the design of a test chip for sparse read-out, and designed a CMOS digital chip for the binary option. UK ATLAS has designed the DORIC chip for clock and control, and has collaborated in RD23 to produce and test MQWs. A collaboration with GEC and ABB Haffo has produced low mass packages for LEDs and PIN diodes. Within the overall programme of development of front-end chips for use at LHC, the RAL Electronics Group now has a record of several successful fabrication runs in the Harris radiation-hard bulk CMOS process.

For the 1995 test-beam activities, UK groups will provide analogue optical links based on both MQWs and LEDs, and also a prototype of the AROMA module (see section 3.5.1) and a prototype VME module for the clock and control distribution. The UK is providing the data acquisition system for all 1995 SCT work in the H8 beamline.

In parallel, the UK are collaborating in the design of the AROW chip (see section 3.3.1.2) and will be involved in beam tests of the digital option. The UK is also collaborating on long term lifetime tests of LEDs after irradiation and on producing the low mass packages that contain the LEDs and PIN diodes.

4.7 GaAs Detectors

The UK groups have played a leading rôle in the development of gallium arsenide detectors, making extensive use of in-house fabrication in collaboration with their local engineering departments. This has allowed the groups to study many aspects of detector fabrication such as various types of contacts to optimise the response of the detectors and development of capacitively-coupled microstrips [16] [17], giving them considerable expertise in the fabrication of detectors. The groups have used their in-house detectors to develop a quantitative understanding of their operation by studying the distribution of the electric field through the detector and how it relates to the observed charge collection efficiencies of the devices [19], [20]. Various GaAs substrates have been studied. In collaboration with colleagues in solid state electronics, measurements of the concentrations of traps in various wafers have been measured and compared to the measured charge collection efficiencies [21].

This expertise has allowed the UK to take the lead in developing commercial prototypes for ATLAS with EEV Ltd, UK and Alenia SpA, Italy. Both companies have fabricated, with test structures, full–size ATLAS detectors. Simple pad devices have been tested with minimum ionising electrons and have charge collection efficiencies in excess of 60%. This is lower than the figure of 80% which was previously achieved with the best Alenia detectors, but further work is required to optimise both contacts and substrates.

Various microstrip structures were fabricated to allow evaluation of the nitride coupling capacitor, the interstrip capacitance and the reach-through biasing. These studies are being used to develop a model of the behaviour of the biasing and the detector capacitances so that the design can be further optimised.

A 50μm pitch capactively coupled Alenia microstrip detector read out using Viking electronics was tested in a silicon telescope at CERN and found to have a position resolution of 14μm, in good agreement with the assumption of a uniform resolution function between read-out strips [18].

These processing runs have also provided first estimates of possible commercial yields and detector costs, and are consistent with numbers given earlier to cost the forward wheels.

UK groups are heavily involved in all aspects of the GaAs development programme to provide radiation hard detectors for the most severe regions of the SCT. Within this programme a second generation of detectors should be fabricated by mid–1996.

The principal aims of this work are:

- Fabrication and test of fan-shaped GaAs detectors
- Tests of detectors with LHC speed electronics
- Improved understanding of position resolution
- Development of module read-out hybrid and fan-ins
- Improvement of charge collection efficiencies for industrial detectors

GaAs detectors for the forward region require a fan-shaped geometry with read-out from radial strips. Such devices will be fabricated in industry to investigate the problems associated with large scale production such as cutting of detectors off the crystal axis and lift-off from angled strips. The devices will be evaluated to investigate properties such as inter-strip capacitance. In future tests the detectors will be equipped with fast shaping time electronics, as proposed for the silicon detectors in ATLAS, and particular importance will be attached to investigating and improving the intrinsic track resolution.

Detector development will continue through both in-house studies and in collaboration with industrial partners, EEV Ltd, UK, and Alenia SpA, Italy. An important issue is the improvement of the charge collection efficiency of detectors fabricated by industry, to match that already obtained from devices fabricated in-house. The work with EEV is being partially supported by a PPARC CASE studentship and the DRDC has provided funds for the work with Alenia through RD8.

4.8 Radiation Studies

Final versions of the semiconductor tracker elements will be investigated in detail as part of the continuing extensive programme of radiation studies within the ATLAS collaboration. In the UK the ISIS facility will be central to this work, and all elements of the final tracker must be capable of satisfactory operation after sustaining high levels of both neutral and charged particle fluences; these will be respectively $10^{14}n/\text{cm}^2$ and 5MRad which correspond to the expected fluences integrated over ten years of ATLAS operation at LHC.

4.9 The Integrated Semi-conductor Forward Option

An attractive option for the inner tracking scheme for ATLAS is an integrated system based entirely on semi-conductor technology, with silicon detectors at radii greater than 30cm and gallium arsenide detectors at smaller radii. To allow an informed decision to be taken during 1995, both the forward tracking with MSGCs (see section 3.9) and the silicon alternative have to provide further technical data from prototype work in the coming months. For the silicon project the main milestones concern the study of non-uniform radial radiation damage and the efficiency and tracking precision for silicon detectors with a fan geometry.

Layout optimisation is under study, with particular emphasis on :

- uniformity of performance over the full η range with ≥ 4 points per track
- adequate momentum resolution both in stand-alone and combined track reconstruction
- maintaining good angle and two track resolutions
- good performance in the transition region from barrel geometry to disc geometry

The UK has completed the design for a fan geometry detector, using the conventional p strips in $n-$type substrate for initial evaluation, and the detectors are currently being fabricated by Micron Semiconductor Ltd. The geometry has a pitch varying from 100 μm to 130 μm along a 12 cm length. The module has 256 read-out channels with a shape such that both halves can be obtained from a single 4 inch diameter wafer. The gap has been kept constant at 75 μm and the strip width to pitch ratio has been chosen as a compromise between the interstrip capacitance and the electric field considerations. A fan-in has been designed to allow this module to be read out using the same hybrid as used in the z-module. The performance of this detector will be studied both in the laboratory and in the H8 test beam in summer 1995, and radiation studies will be undertaken using ISIS.

If the forward silicon option is adopted for the final ATLAS tracker it will be necessary to carry out further detailed prototyping of all aspects of the forward modules including detectors, electronics and the associated mechanics and cooling.

4.10 The MSGC Forward Option

4.10.1 Introduction

The technology choice for the forward tracker will be determined in the next few months. In the past five years MSGCs have developed from a laboratory device to active elements of HEP experiments. Their first use was in the NA12 experiment at CERN to exploit their high rate capability as beam counters, in the future a larger installation of 100 detectors will be used in the HERMES experiment at HERA.

Properties that make them appropriate for the ATLAS forward tracking include:

- an operational effective gain of around 1500, much below the typical breakdown value of 10,000,
- high measured intrinsic efficiency: greater than 98% with noise occupancy less than 0.1%,
- good pattern recognition capability in each $uv\phi$ three layer module,
- no significant drop in gain or efficiency when they are subjected to the charged particle flux expected at a radius of 40cm in ATLAS,
- little radiation damage or ageing: less than 20% decrease in gas gain after an accumulated charge equivalent to 10 years of operation at full LHC luminosity,
- ionisation spread over many strips for unwanted low transverse momentum tracks so their detection efficiency is low, with consequent reduction in occupancy.

Below the achievements to date are briefly decribed, and a description of the remaining development work to be completed by September 1995 is given.

4.10.2 Status of the MSGC Baseline Detector

The UK groups have carried out beam tests within the RD28 collaboration in 1993 and 1994, and demonstrated that an efficiency per layer of $> 98\%$ could be achieved with less than 0.1% noise hits at an intensity of 6×10^4 mm^{-2} s^{-1} (Fig. 24). The detectors had a pitch of 200μm, were operated with Ar/DME 80:20 gas mixture and gave a measurement precision per layer of 45 to 50μm.

Accelerated ageing tests have been carried out in the laboratory using X-rays. The same gas showed an 8% loss of gain after 45mC/cm, with a logarithmic time-dependence that would extrapolate to 11-15% loss after

100 mC/cm. Figure 25 shows the result of a more gradual ageing test using a strontium source which has shown a gain drop of 12% in 66 days, corresponding to a total dose of about 60 mC/cm. These gain losses can be recovered by a small increase in cathode potential so the performance of the detector is not expected to change significantly during the LHC lifetime.

The design of anode and cathode strips has advanced with a scheme that now overcomes earlier difficulties in strip-end damage and a detector with gold electrodes has been built with an active area of 13cm by 16cm.

This work has demonstrated the successful operation of full size MSGC modules on 400 μm S-8900 glass which can meet the necessary specifications for use in ATLAS.

4.10.3 The Current Development Programme

During the summer of 1995 specific features under study include:

- improving the radiation length of the glass, which in S-8900 is dominated by the barium content. A simple reduction in glass thickness from 400μm to 200μm is not feasible on account of both cost and practical handling considerations. However investigations into the use of magnesium is underway, as well as the use of sub–millimetre sputtered S-8900 glass on lightweight D263 glass.
- several laboratories will extend the accelerated ageing tests with X-rays to the full 100 mC/cm in order to demonstrate that the clean gas conditions that are essential for good ageing results can be reliably reproduced. S-8900 MSGCs are also in use in the WA102 experiment in Omega at CERN where 100 days running in the beam is providing the equivalent dose from charged particles to 2 years LHC running at design luminosity.
- the effects of neutron flux on performance is being further studied using ISIS at RAL, where encouraging results are being obtained.

The UK H6 test beam work within RD28 will be completed this year, using the facilities from previous runs to provide input for the milestone objectives:

- measurement of two-track resolution - this has already been studied from simulation using old data
- scanning of full size keystone detector to check gain uniformity
- a study of efficiency and resolution close to edges
- a check of beam crossing (BCO) tagging algorithms
- a study of efficiency and resolution with track angle.

4.11 Vertex Detector

Although the scale of the vertex detector is small compared to the overall SCT, it is an area which is also of particular interest to UK groups and well matched to expertise from LEP. These groups are currently active in the design of the detector, in the technical development studies and in the layout optimisation for heavy flavour physics. Funds are requested to allow the UK to play a significant part in constructing the final instrumentation.

5 UK Funding and Construction for the Inner Detector

5.1 The Planning Strategy

The UK ATLAS groups will continue to build on their current expertise and interests through the next few years of final design, leading into the large scale production and module building for the final instrumentation.

Such is the construction scale for the ATLAS inner detector that it demands a rigorous control of engineering and production processing, with the necessary quality assurance. This is being agreed within the world-wide collaborating institutes, and has led naturally to a proposed small number of centres within Europe, Japan and the USA for production, assembly and testing of the barrel silicon modules. In line with their investment in design and prototyping activities, the UK and Japan will be the largest centres, each proposing to produce and hence finance about 25% of the total. For the forward silicon scenario, the UK would provide an additional production centre and be responsible for 25% of the total silicon modules of the complete inner detector. The UK also proposes to take responsibility for construction of about 50% of the inner vertexing layer.

Given the UK involvement in clock and control, receiver electronics and data acquisition, we would wish to provide 30% of the total cost of these items. We also propose providing 100% of the finance and taking sole responsibility for the system alignment. The UK will also take major responsibilities for the project engineering and semi-conductor cooling system and proposes to provide 50% of the funding.

For GaAs the UK will provide a production and assembly centre for modules and proposes to contribute 50% of the project funding.

The forward MSGC option will involve major production facilities in the UK and funding resources at the level of 50% of the module and engineering costs.

The scale of these projects requires the full deployment of all the available UK resources. To contribute effectively many UK institutes will require upgraded or new clean room facilities, some with automatic wire bonders and all with probe stations equipped with the necessary instrumentation for device characterisation and testing. Very high quality optical microscopes are another requirement for this work. These facilities will all need to be commissioned within the next two years, together with the training of the necessary additional skilled staff to carry out the several years of full-time production work. It is anticipated that a small part of the requested manpower for the project will be located in the Universities to provide additional short-term technical support during the construction phase.

5.2 Institute Responsibilities

5.2.1 Silicon Tracker

Each UK ATLAS institute will be responsible for one or more aspects in this production process, as well as collaborating in the work at the relevant co-ordinating UK site where sub-component integration will be part of the final module production and detector assembly. In particular, short and long term testing of final modules will occur at Cambridge, Liverpool, QMW and RAL.

The decision on final ATLAS technologies will clearly affect the details of the UK internal plan, but already agreed options exist.

Silicon strip modules for the barrel will, in any option, be constructed in the UK, with the following distribution of responsibilities:

- Birmingham : optical links
- Cambridge : wafer procurement and testing; data receiving modules and data acquisition
- Liverpool : hybrid procurement; on–hybrid ASIC wire bonding and testing
- Oxford : assembly of structural mechanics and global alignment; clock and control
- QMW : front-end chip testing and precision assembly mechanics
- RAL : structural engineering, cooling, module assembly and wire bonding, micro-electronics and system support

The overall cost of the project and the UK request are given in Tables 5 & 6.

If silicon devices also become the technology for the forward region the present effort foreseen for MSGC production from Birmingham, Manchester, RAL and UCL would be used within an extended UK silicon project. Some of the groups would join with Liverpool, who in this scenario would concentrate on forward module production, and the others would take responsibilities within the barrel detector project to maintain the current proposed UK commitment. The proposed areas of responsibilities of the different institutions are summarised in table 8.

5.2.2 Gallium Arsenide Modules

The UK groups are leading experts in these devices, and will provide a UK-based production centre for the module construction at one of their institutes. This will clearly benefit from techniques across mechanics and electronics that are in common with the larger scale UK silicon module production. In the case of a forward silicon solution, it is envisaged that the integrated GaAs and silicon wheels would be the UK's specfic responsibility. The responsibilities of the GaAs groups during construction are listed below:

- Detector testing, module assembly and module testing will be carried out at Glasgow, Lancaster and Sheffield.
- Glasgow: Detector procurement, hybrid procurement, assembly with FE electronics and testing, assembly of modules onto wheels.
- Lancaster: Wheel mechanics and cooling, alignment, hybrid testing, power supplies procurement and testing.
- Sheffield: Detector procurement, off-detector electronics and DAQ.
- RAL: Bonding of both detectors and FE-electronics to hybrids.

5.2.3 MSGC Construction

The forward tracker will require a major production site in the UK, in a project shared financially principally with NIKHEF. The UK institutes, Birmingham, Manchester, RAL and UCL will each take on responsibilities to cover all aspects of chamber construction and testing.

5.3 The Timescales and the Funding Request

The overview of the general time-tabling of the project is given in the ATLAS inner tracker bar chart. In Table 5 a cost summary is provided of each of the sub-detectors of the inner detector project: the barrel semi-conductor tracking, together with the forward semi-conductor tracking option and the forward MSGC tracking. Together these amount to 60MSF, which becomes 68MSF when the complete data-acquisition and future development costs are included.

The intentions of the UK groups, given above, are shown in Table 6 for the sub-component items that form the basis of this request for PPESP funding. The total and sub-total costs are summarised in Table ??, on the basis of an exchange rate of SF1.8/£, together with an indication of the required spend profile and request for additional manpower for the project. Table 8 gives the areas of responsibilities to be taken by the UK institutes, and Table ?? lists the physicist and engineering effort they will provide.

The funding request for the inner detector project over its development, construction and commissioning phase totals £14.62M, plus an additional 359 SY of effort.

Task	Responsible	Other contributors
Barrel Silicon Tracker		
Module Construction		
Detectors	Cambridge	Liverpool, QMW, RAL
FE Electronics	QMW	RAL
Hybrids	Liverpool	Birmingham
Fan–ins	RAL	–
Assembly	RAL	QMW
Mechanics & Assembly	RAL	Oxford
Cooling	RAL	–
Alignment	Oxford	–
Data Links	Birmingham	RAL
Receiver modules and DAQ	Cambridge	RAL
Forward Silicon Tracker (if adopted)		
Module Construction		
Detectors	Liverpool	RAL
FE Electronics	QMW	RAL
Hybrids	Birmingham	Liverpool
Fan–ins	RAL	–
Assembly	Manchester	Liverpool
Mechanics & Assembly	Liverpool	Manchester, RAL
Cooling	RAL	UCL
Alignment	Oxford	–
Data Links	Birmingham	RAL
Receiver modules and DAQ	Cambridge	RAL
Forward MSGC Tracker (if adopted)		
Module Construction	RAL	Birmingham, Manchester
Module Testing	Manchester	Birmingham, RAL, UCL
Clean Gas Monitoring	Birmingham	UCL
Wheel Assembly	RAL	Manchester
Cooling	RAL	–
GaAs Forward Wheels		
Detectors	Sheffield	Glasgow
Module Construction	Glasgow	Sheffield
Mechanics, Assembly & Cooling	Lancaster	RAL

Table 8: **Areas of Responsibility of UK groups for Construction of the Inner Detector**

Item	Costs (MCHF)
Integrated Semi-conductor Tracker	
Barrel Silicon	
CORE Items	25.271
DAQ	1.600
R&D	2.840
Contingency	6.551
Barrel Silicon Sub-total	**36.262**
Forward Silicon *Preliminary cost estimate based on CORE SCT*	
CORE Items	18.352
DAQ	1.100
R&D	1.090
Contingency	4.758
Forward Silicon Sub-total	**25.300**
Silicon Total	**61.562**
Semi-conductor+MSGC Tracker	
Silicon Barrel	
CORE Items	31.045
DAQ	2.000
R&D	2.840
Contingency	8.000
Silicon Sub-total	**43.885**
MSGC Forward	
CORE Items	12.146
DAQ	1.000
R&D	2.000
Contingency	0.972
MSGC Sub-total	**16.118**
Silicon+MSGC Total	**60.003**
GaAs Wheels	
CORE items	4.974
DAQ	0.550
Modules/facilities	0.400
R&D	0.500
Contingency	0.500
GaAs Total	**6.924**

Table 5: **Complete Costings of Inner Detector Components**

Item	Costs (MCHF)
Integrated Semi-conductor Tracker	
Module Construction	12.33
Engineering/Cooling	4.53
Alignment	1.26
Off-detector/DAQ	1.21
Vertex	0.63
Sub-total	**19.96**
Local Infrastructure/facilities	0.90
R&D	2.0
Sub-total	**2.90**
Silicon Total	**22.86**
Semi-conductor+MSGC Layout	
SCT-silicon Barrel	
Module Construction	9.00
Engineering/Cooling	2.52
Alignment	0.63
Off-detector/DAQ	0.83
Vertex	0.63
Sub-total	**13.61**
Local Infrastructure/facilities	0.50
R&D	1.36
Sub-total	**1.86**
Silicon Total	**15.47**
Forward (MSGC)	
Module Construction	4.78
Engineering/Cooling	1.05
Off-detector/DAQ	0.39
Sub-total	**6.22**
Local Infrastructure/facilities	0.35
R&D	0.80
Sub-total	**1.15**
MSGC Total	**7.37**
GaAs Wheels	
Materials for two wheels	2.74
Off-detector/DAQ	0.28
Facilities	0.20
R&D 96+97	0.25
GaAs Total	**3.46**
Grand Total	
Integrated Silicon	**26.32**
Silicon+MSGC	**26.30**

Table 6: **UK Tracker Project Funding Request**

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Figure 10: Variation of depletion voltage and strip leakage current with radiation for 300 μm thick detectors at a radius of 30 cm, for 12 cm $\times$ 112.5 μm strips operated at $0°C$. The luminosity scenario assumed is three years at $\mathcal{L} = 10^{33}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ followed by seven years at $\mathcal{L} = 10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$.

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Figure 11: The dependence on operating temperature of the depletion voltage and strip leakage current after 10 years of operation. The curves are for 300 μm thick silicon detectors at a radius of 30 cm with 12 cm $\times$ 112.5 μm strips.

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Figure 12: Noise versus efficiency as measured in test beams for analogue and binary read-out electronics

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Figure 13: Block diagram of the ATLAS digital FE chip, AROW.

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Figure 14: The Barrel Silicon Module.

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Figure 15: The Forward Silicon Module.

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Figure 16: Forward Silicon Wheel Preliminary Design.

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Figure 17: MSGC Detector Module

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Figure 18: MSGC Support Structure

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Figure 19: Components for a Frequency Scan Interferometry System

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Figure 20: Fringe Patterns with ESPI

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Figure 21: ESPI Principle

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Figure 22: Charge Division Resolutions.

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Figure 23: The Barrel Silicon Strip Detector Wafer.

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Figure 24: Two independent measurements of MSGC performance at high rate.

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Figure 25: MSGC ageing test with Sr^{90}.

6 The ATLAS Level-1 Trigger

6.1 Introduction

The ATLAS trigger system must have unprecedented selectivity, handle an enormous number of detector channels, and at the same time cope with a 25 ns bunch-crossing period and multiple interactions per bunch crossing. The level-1 trigger system must make decisions in under 2 μs, without deadtime. It will use special-purpose processors acting on reduced-granularity data from the calorimeters and muon detectors.

The level-1 calorimeter trigger is being developed by a collaboration from Birmingham, CERN, Heidelberg, QMW, Stockholm and RAL. The processor uses information from $\sim$ 8000 trigger cells to form electron/photon, jet and missing-E_T triggers. The UK trigger design, developed over the past three years, has been accepted as the ATLAS baseline and is being proven in a series of beam tests. We are now requesting PPESP support for continued UK leadership in the final design, testing, construction and operation of the calorimeter trigger.

6.2 Physics Rates and Signatures

6.2.1 Signatures

The task of the level-1 trigger is to examine in real time the 40 million bunch crossings per second, each containing $\sim$18 proton-proton interactions, and to select no more than $10^4 - 10^5$ of them containing potentially interesting physics to be passed on to the level-2 trigger. The sub-detectors used at level-1 are the calorimeter and muon systems. The signals of interesting interactions are high-E_T leptons, partons, and photons. The level-1 calorimeter trigger looks for energy deposition corresponding to:

- Electromagnetic showers (electrons, photons)
- Jets (quarks, gluons)
- Missing E_T (neutrinos, other weakly-interacting particles)

The algorithms proposed to detect these signatures are described below. Collisions producing W and Z bosons must be detected with good efficiency, and this sets the transverse energy scale for the trigger. Table 10 lists some of the most interesting particles which might be produced and suggests suitable trigger selections and thresholds.

6.2.2 Electromagnetic Cluster Trigger

The most challenging trigger at level-1 is the electromagnetic shower trigger. This requires energy deposition in a small area of the electromagnetic calorimeter, and has a very large background coming from QCD jets. The rate of false triggers can be reduced by decreasing the size of the electromagnetic trigger cells, but this must be balanced by the resulting increase in the number of cells and therefore in the overall cost.

In figure 26 we show a window of the combined calorimeters consisting of a 4×4 array of electromagnetic and hadronic trigger cells. The algorithm is based upon cluster and isolation sums formed within such windows. The windows overlap, sliding by one cell in both directions. Defining an electromagnetic cluster as the sum of transverse energy in a pair of trigger cells adjacent in rapidity or azimuth, the simulated level-1 trigger rate is shown in figure 27 as a function of trigger cell granularity. This is for a 40 GeV transverse-energy threshold at full LHC luminosity. The rate is dominated by jet-induced false triggers.

We find that a cell size of 0.1×0.1 represents a reasonable compromise between level-1 rate and the number of trigger cells, and this is the size used for the cluster algorithm simulations. Other cluster definitions have been studied, namely a single trigger cell and a 2×2 cluster, but these have been rejected from considerations of cluster energy resolution and increased trigger rate respectively.

Figure 27 indicates that the simple cluster requirement alone may not bring the total level-1 trigger rate safely below the maximum level-2 input rate of 10^5 Hz. A further reduction can be achieved by requiring that the cluster energy is isolated. This is not be the case for QCD jets, which typically extend over an $\eta - \phi$ region of about 0.8×0.8, and also penetrate through the electromagnetic calorimeter into the hadronic calorimeter behind. Limits on the lateral and longitudinal extent of the energy deposition can be applied by requiring little energy in the surrounding electromagnetic cells, and in the hadronic cells behind. The additional jet rejection expected from the application of these isolation requirements is shown in table 11. In our chosen cluster algorithm, isolation is imposed by requiring the total transverse energy in both the outer sum and in the

Process	**Signature**	**Level-1 selections**
$H^0 \to \gamma\gamma$ height$H^0 \to ZZ* \to l^+l^-l^+l^-$ $(M_H < 2M_Z)$	$E_T^{\gamma_1} > 40$ GeV $E_T^{\gamma_2} > 25$ GeV two lepton pairs, one $M_{ll} = M_Z \pm 10\ GeV/c^2$	$\geq 1\gamma, E_T > 40$ GeV $\geq 2\gamma, E_T > 20$ GeV $\geq 2e, E_T > 20$ GeV $\geq 2\mu,\ p_T > 20$ GeV $e + \mu,\ E_T > 20$ GeV
$H^0 \to ZZ* \to l^+l^-l^+l^-$ $(M_H > 2M_Z)$	two lepton pairs, both $M_{ll} = M_Z \pm 10\ GeV/c^2$	$\geq 2e, E_T > 20$ GeV $\geq 2\mu,\ p_T > 20$ GeV $e + \mu,\ E_T > 20$ GeV
$Z \to l^+l^-$	Z-mass requirement	$\geq 2l, E_T > 20$ GeV
$W \to l\nu$	lepton p_T and missing E_T	$\geq 1l, E_T > 40$ GeV
top: 3 jets + leptons	two jets with M_W + 1 jet of $p_T > 50$ GeV opposite lepton	$\geq 1l,\ E_T > 40$ GeV
Multijets	three jets, $p_T > 300$ GeV	≥ 3 jets, $E_T > 250$ GeV
SUSY: Classical	circularity of events	≥ 3 jets, $E_T > 250$ GeV + missing $E_T > 200$ GeV
SUSY: Cascade	two $Z \to l^+l^-$ candidates, 4-lepton mass > 250 GeV + missing $E_T > 100$ GeV	$\geq 2l,\ E_T > 30$ GeV

Table 10: Benchmark physics processes and trigger criteria.

Isolation test	**e.m. alone**	**hadronic alone**	**e.m. AND hadronic**	**e.m. + hadronic**
Rejection at 20 GeV	2.5	1.7	3.0	2.7
Rejection at 40 GeV	6.0	3.1	7.8	7.0

Table 11: Rejection factors from isolation for events passing cluster thresholds of 20 GeV and 40 GeV. Isolation thresholds were chosen to give 95% efficiency for electrons.

16 hadronic cells to be below separately adjustable thresholds (penultimate column). The less flexible option of applying one threshold to the sum of the two regions (last column) performs almost as well.

Studies have been made of the resolution required for digitisation of the analogue signals from the calorimeters, and also the threshold level which should be applied to individual trigger cells before they are allowed to participate in the cluster algorithm. The conclusions are that a digitisation resolution in E_T of 1 GeV is sufficient for trigger purposes, and that a cell threshold of 1 GeV in E_T optimises the effectiveness of the isolation requirement.

The cluster algorithm we have described has the problem that single electromagnetic depositions can give cluster triggers in several overlapping trigger windows. The final trigger signal which goes to the central trigger processor must contain the number of actual clusters found, so logic must be provided to extract the number of clusters from the pattern of cluster triggers.

6.2.3 Jet Trigger

Jet production will be the dominant high-p_T process at LHC. For level-1 jet triggers the most important problem to solve is that of jet energy resolution at the trigger level. The production of jets rises rapidly as E_T decreases, and if the E_T resolution is poor the threshold will be badly defined. This will lead to a very inefficient trigger or a very high rate.

Jet resolution at the trigger level is affected by many factors, including the difficult problem of the different calorimeter response for electromagnetic and hadronic energy deposition. This can be partly compensated by adjusting the relative weightings of e.m. and hadronic calorimeter energies. The size of the jet window has been

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Figure 26: View of a 4×4 trigger-cell area of the calorimeter.

investigated, and the favoured solution is to set a jet window with $\eta - \phi$ dimensions of 0.8×0.8. Such a window, overlapping and sliding in both η and ϕ by 0.4, gives good jet containment and therefore potentially good jet energy resolution.

6.2.4 Missing Transverse Energy

Detection of missing transverse energy in an event indicates the possible production of a weakly interacting particle. Missing transverse energy resolution is sensitive to any lack of hermeticity. This can be caused by cracks and joins between different detectors, and also by insufficient coverage in $|\eta|$ by the calorimeters contributing to the level-1 trigger. Simulation has shown that for acceptable missing-E_T resolution, calorimeter coverage will have to be extended out to $|\eta| = 5$, in contrast to $|\eta| = 2.5$ for electromagnetic clusters and $|\eta| = 3$ for jets. A study of missing transverse energy resolution as a function of effective calorimeter granularity indicates that $\eta - \phi$ dimensions of 0.4×0.4 are acceptable, and this is a good match to the granularity favoured at present for jets. Problems coming from cracks between calorimeters and non-physics background tracks are still being evaluated.

6.3 Physics Simulation and Expected Trigger Rates

Events have been generated corresponding to some of the physics channels in table 10, namely:

- $H^0 \to \gamma\gamma$; $M_H = 120\ GeV/c^2$
- $H^0 \to ZZ^* \to e^+e^-e^+e^-$, $e^+e^-\mu^+\mu^-$; $M_H = 130,\ 150\ GeV/c^2$
- Top events, where the top quarks decayed to electrons

Events containing isolated electrons and events containing high-E_T jets have also been generated. They were passed through the ATLAS calorimeter simulation chain, and used to optimise trigger algorithms for electromagnetic clusters, jets, and missing transverse energy triggers at level-1. The results of the simulations are presented below. More details are given in reference [25].

The expected trigger rates for the trigger selections indicated are shown in table 12. At lower luminosity, e.g. $10^{33}\ cm^{-2}s^{-1}$, the rejection required at level-1 will be lower. Here it will be possible to lower the single cluster

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Figure 27: Trigger rate at L = 10^{34} $cm^{-2}s^{-1}$ vs. cell size ($\Delta\eta \approx \Delta\phi$) and vs. number of e.m. trigger cells.

threshold to 20 GeV in order to have good efficiency to search for the pseudoscalar Higgs decay, $A^0 \rightarrow \tau^+\tau^-$ for A^0 masses greater than 100 GeV/c^2. Low-luminosity running may also enable a study of B physics by lowering the cluster threshold to a very low value.

6.4 The ATLAS Level-1 Calorimeter Trigger

6.4.1 Level-1 Trigger System

The level-1 trigger system for ATLAS, shown in figure 28, is based on calorimetry (electron, photon, jet, missing transverse energy triggers) and on muon detectors. The two trigger processors operate independently and in parallel to summarise the characteristics of each event in terms of: the multiplicities of electrons and photons above several E_T thresholds, the multiplicities of jets above several thresholds, the multiplicities of muons above several thresholds, and missing E_T above several thresholds. These results are sent to the level-1 central trigger processor, where the overall level-1 trigger decision is taken. In addition, information on regions of interest in the calorimeter and muon systems is passed to the level-2 trigger in order to reduce the amount of data it has to process.

The level-1 trigger system is based on purpose-built digital processors and makes extensive use of custom microelectronics. The processing is pipelined, and many operations are performed in parallel. Such processors have a fixed set of algorithms, but are programmable at the level of parameters. In order to minimise latency due to propagation delays in cables, the calorimeter trigger processor and the central trigger processor will be placed in an underground electronics room near the experiment.

6.4.2 Level-1 Calorimeter Trigger: Architecture

Birmingham, QMW and RAL are involved in the design and prototyping of a purpose-built, synchronous digital processor for the level-1 calorimeter trigger. The design has evolved in intensive studies over the past year, and full details are given in a backup document [25] to the ATLAS technical proposal. Its main components, shown in figure 29, are the front-end summing and digitisation system, bunch-crossing identification (BCID) logic, a high-speed transmission system, and the processor itself, identifying e.m. clusters, jets and missing E_T. The system accepts signals from all the calorimeters, in the form of ~8000 reduced-granularity 'trigger cells'. This design has been adopted as the ATLAS baseline [1].

Trigger selection	Rate at $L = 10^{34} cm^{-2} s^{-1}$
Single cluster, $E_T \geq 35$ GeV, e.m. and hadronic isolation	3.5 ± 0.4 kHz
Single cluster, $E_T \geq 55$ GeV, hadronic isolation	1.4 ± 0.3 kHz
Single cluster, $E_T \geq 75$ GeV, no isolation	1.8 ± 0.3 kHz
Pair of clusters, $E_T \geq 16$ GeV, e.m. and hadronic isolation	2.4 ± 0.5 kHz
Pair of clusters, $E_T \geq 30$ GeV, hadronic isolation	0.9 ± 0.3 kHz
Pair of clusters, $E_T \geq 40$ GeV, no isolation	1.4 ± 0.4 kHz
Combination of above selections	8.4 ± 0.8 kHz

Table 12: Estimated electromagnetic cluster-trigger rates at LHC design luminosity.

6.4.2.1 Front-end processing

Analogue signals from the calorimeters are summed on the detector to form trigger cells of granularity $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$ and are digitised by an 8-bit linear FADC with a nominal resolution of $E_T = 1$ GeV per count. The digital data pass through a look-up table where pedestal subtraction and final calibration are applied, yielding an 8-bit E_T measurement for the trigger cell. The data then pass through a BCID stage where the digitisation corresponding to the pulse peak is selected, and other FADC samples are set to zero. Following BCID, pairs of trigger cells are combined to form 16-bit words for transmission on optical fibre at 800 or possibly 1600 Mbaud. Approximately 65 m of fibre is needed to carry the signals from the detector to the underground counting room where the trigger processing crates are situated.

6.4.2.2 Integrated-optics multi-chip module

The optical fibres will be received on the cluster-processing modules in four-channel integrated-optics multi-chip modules (MCMs). Each MCM will include: an integrated optical-to-electrical converter with a fibre pig-tail; a serial-to-parallel converter to translate the incoming serial bit-streams to 16-bit words (i.e. data from two trigger cells) every 25 ns; a 4-bit $\times$ 4 serialising ASIC, which will transmit the 16-bit word on four serial links operating at 160 Mbit/s, as required by the cluster-processing ASIC and crate backplane; and diagnostic and readout memory. The parallel-to-serial and serial-to-parallel converters at the two ends of the transmission chain form a chip-set using the same serial protocol.

6.4.2.3 Crate backplane

Data from a large number of channels within each crate must be fanned out to one, two or four neighbouring modules, using a minimum number of input/output pins. We have chosen to use 160 Mbit/s single-ended serial signals (i.e. two per trigger cell) in the backplane transceiver logic (BTL) standard of Futurebus+, in order to minimise connector pin count. The required backplane is a dense, multi-layered device.

6.4.2.4 Cluster processing

Reception of data into the cluster-processing modules and ASICs at the required density and rate has proved to be the most demanding aspect of the trigger development. The design calls for a cluster-processing ASIC to process 16 overlapping trigger windows, using E_T values from a total of 98 cells (7×7 trigger cells for each of the e.m. and hadronic calorimeters). Each cluster-processing module houses four ASICs and takes in E_T values from 242 trigger cells to process a total of 64 overlapping trigger windows. To achieve this density, data enter the cluster-processing ASICs synchronously as two serial 160 Mbit/s streams per cell, using two I/O pins. Input signals at this speed are received on the modules both from the crate backplane and, after multiplexing, from the 64 optical fibres which are brought directly onto each module.

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Figure 28: Level-1 trigger architecture.

6.4.2.5 Subsequent processing

Information from the cluster-processing modules is sent to the three subsequent trigger stages. Transverse energy components Ex and Ey are summed in results modules in each crate, and then sent to the missing-E_T module for final adding and thresholding to yield a combined E_T flag for the event.

The jet-finding algorithm uses the E_T added over 4×4 trigger-channel areas of the calorimeter from the cluster-processing modules. These super-towers will be further summed into 2×2 sliding windows, each of which will be compared to eight threshold values. This operation is performed in eight jet-processing modules.

The cluster-counting electronics for jets and e.m. clusters is identical, and will use veto logic to avoid double-counting of contiguous hits. Cluster-counting modules will examine, for each E_T threshold, a 256-pixel array of hits from either the e.m. cluster-processing modules or the jet-processing modules and count non-vetoed pixels. The resulting multiplicity will then be compared to multiplicity thresholds.

The results flags generated in the electron, jet and E_T processing are sent to the central trigger processor, where information from the muon trigger is also received. The resulting level-1 accept signal is distributed throughout the detector within 2 μs of the original bunch-crossing to initiate event readout.

6.4.2.6 Physical layout

The data reception and e.m. cluster processing is the most demanding part of the system, and this will be housed in four crates. Subsequent processing will require two further crates. The trigger will use six different ASIC designs. Figure 30 shows a block diagram of the trigger processor layout.

The system can be built using standard 9U-high crate mechanics with commercially available connectors. Extensive test and monitoring facilities are included in the design, and allow intermediate results to be checked for exact bit-for-bit agreement.

6.4.3 Level-1 Calorimeter Trigger: Key Design Issues

A number of alternative front-end designs for the calorimeter electronics are still under consideration. If the trigger cells are formed by analogue summation, the signals can be digitised on the detector and transmitted using high-speed optical fibres, as in our baseline design described above. This requires further work to master high-speed and high-density serial data transmission, and these are part of our core programme for the immediate future [26]. Alternatively, the data could be transmitted in analogue form to the processor using either copper cables or analogue optical-fibre transmission. Even in this option, with trigger ADCs near the processor, considerations of pin count make high-speed serial input to the trigger processor mandatory.

In a completely different approach, the calorimeter signals would first be digitised and then summed on the detector (as in the FERMI system). They would then be transmitted digitally on optical fibres.

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Figure 29: Block diagram of the level-1 trigger system.

Analogue pulses from the calorimeters typically extend over many bunch-crossings, while the level-1 trigger must identify without ambiguity the energy deposit associated with each bunch-crossing. Various approaches to the problem of BCID can be envisaged. We are concentrating on digital solutions with programmable parameters, allowing the system to be adapted to pulse shapes from the different calorimeters. The algorithms under study use digital filtering to sharpen the pulse, followed by one of several peak-finding algorithms. Test-beam studies were performed in 1993 [27] using a single-channel BCID module to process data in real time from the RD3 liquid-argon prototype e.m. calorimeter, and in 1994 from the tile and liquid-argon hadron calorimeters. Construction of a more compact 36-channel system, for use in more extensive test-beam studies in 1995, is nearing completion.

The electron/photon trigger algorithm at the heart of the system, shown in figure 26 , identifies localised deposits of E_T in the e.m. calorimeters, and optionally requires isolation. The feasibility of pipelined logic for finding e.m. clusters at the required speed was demonstrated in a test beam in 1993, when an ASIC incorporating the e.m. component of the trigger was successfully demonstrated at the full LHC bunch-crossing rate of 40 MHz [28].

Implementation of this algorithm requires a very high degree of fan-out of the input information. This is because the number of windows needed is equal to the number of e.m. calorimeter trigger cells, and each window requires information from 16 e.m. and 16 hadronic cells. Although each cluster-processing ASIC will handle several such windows, the interconnections would demand too many pins both on modules and on ASICs if the data were fanned out in parallel format. Our trigger design therefore uses high-density, high-speed backplanes to transmit data between modules within a crate using serial format. The speed chosen, 160 Mbit/s, is only just feasible using current CMOS ASICs. For fan-out between crates, we propose to use passive splitters in the optical fibre links. These fan-out issues are another part of our immediate core programme [26].

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Figure 30: First-level calorimeter trigger processor.

6.5 The Role of the UK Groups

6.5.1 Introduction

The architecture of the ATLAS level-1 calorimeter trigger system described in section 6.4.2 represents the culmination of over three years work by the three UK institutes, which has drawn heavily on their extensive experience of designing first-level trigger systems for earlier experiments (UA1, H1). Although some of the technical features of the proposal have arisen as a result of a growing collaboration between ourselves and groups from Stockholm and Heidelberg universities, it is undoubtedly the UK groups that have provided the leadership of the project.

We have played a leading role in the area of physics simulation, upon which much of the subsequent hardware design and development has been based. Our R&D work has progressed through several stages, each of which has led (or is planned to lead) to the extensive evaluation of hardware in the realistic environment of the ATLAS test beam. We have maintained a high level of test-beam activity and continue to place considerable importance on this aspect of our programme.

The first R&D phase involved the implementation of an electromagnetic cluster-finding algorithm, selected on the basis of our simulation studies, in a fast ASIC. This work was successfully concluded in 1994 and the results published [28]. It was followed by theoretical studies of the BCID problem which led to a hardware implementation of algorithms selected on the basis of our simulation work [27].

6.5.2 Current Demonstrator Programme

The BCID demonstrator programme will conclude in 1995 with beam tests of a 36-channel system, designed using re-configurable Xilinx field-programmable gate arrays (FPGAs) to study a range of algorithms operating on calorimeter pulses with various shaping times. Many features of the proposed level-1 calorimeter trigger system are known to be viable from the results of our demonstrator-based R&D work over the last three years (e.g. electromagnetic cluster-finding algorithms and BCID algorithms operating at full LHC speeds). However, parts of the architecture – in particular the techniques for data transmission and fan-out – involve some novel technologies that require further evaluation. A final demonstrator programme is currently under way to explore these areas throughout 1995/6 [26]. The successful conclusion of this programme will allow a realistic prototype trigger system for ATLAS to be constructed.

6.5.2.1 Minimal demonstrator system

Our demonstrator system is based upon a data transmission chain (figure 31) which exercises all the novel technologies in the proposed ATLAS architecture:

- Optical (and electrical) data transmission/reception at up to 1600 Mbaud
- Integrated-optics techniques on high-speed MCMs
- Fan-out of 160 Mbit/s data using transmission-line backplanes
- CMOS ASIC I/O at 160 Mbit/s

This minimal sub-system begins with a flash-ADC module to digitise data with 8-bit resolution at 40 MHz. A transmitter module pre-processes these data (subtracts pedestals, applies calibration constants and performs BCID) and launches serial bit-stream data into 65 m-long multi-mode fibres from laser diodes at 800-1600 Mbaud.

At the front end of a cluster-processing module the data are received by customised integrated-optics devices mounted on an MCM, which contains both commercial serial-to-parallel dies and time-multiplexing ASIC dies to convert the resultant data into multiple 160 Mbit/s bit-streams. This MCM is designed to resemble the final system MCM as closely as possible.

The 160 Mbit/s bit-stream data are transmitted from the MCM to the cluster-processing ASICs, and also to the transmission-line backplane which acts as the fan-out medium for distributing data between neighbouring cluster-processing modules (only two of which are provided in the minimal system). To execute the cluster-processing algorithm for a maximum of four trigger windows, each module requires data from up to 25 trigger cells, four of which are fed directly from the MCM and the remaining 21 from the backplane.

The conversion of the 160 Mbit/s serial bit-streams to parallel data, which will take place in the front-end of large cluster-processing ASICs in the final ATLAS system, is performed here by part of a dual-function ASIC, the other part of which is used for the time-multiplexing function on the MCMs (as described above). Dual functionality leads to a considerable reduction in NRE costs. The cluster-processing function is achieved by the original ASICs which were used in the first-phase demonstrator work.

Central timing is provided by a programmable multi-phase clocking system, allowing precise synchronisation of data passing between different stages of the system.

An intensive R&D programme involving industry during 1995 will lead to the installation and evaluation of this minimal system in the ATLAS test beam in early 1996.

6.5.2.2 The full demonstrator system

Whilst experience is being gained with this sub-system at CERN, the complete demonstrator system (figure 32) will be constructed. This processes a 3×3 array of electromagnetic calorimeter trigger windows, using information from a 6×6 trigger-cell array.

Analogue signals from the ATLAS liquid-argon electromagnetic calorimeter prototype are summed laterally and in depth to form 36 trigger cells which are digitised by a system of 9 FADC modules. The resultant signals are pre-processed by a set of nine transmitter modules feeding optical (or electrical) data at up to 1600 Mbaud to a series of nine cluster-processing modules, communicating with each other via a transmission-line backplane. Each cluster-processing module receives and fans-out data from a 2×2 array of trigger cells.

The system may easily be extended to incorporate a Readout Controller (ROC) as well as modules to perform missing-E_T and jet processing functions, to conform with the architecture described in section 6.4.2.

6.5.2.3 Timescales

The BCID demonstrator system is currently nearing completion and will be installed in the ATLAS test-beam in May 1995, with data-taking studies in June and September 1995.

Many key elements of the main demonstrator programme are already well advanced. The dual-function ASIC design is complete and has been submitted for fabrication, and a commissioned design study of integrated-optics technologies has been finished. With the specification complete, industry has been invited to bid for the

MCM design and manufacture in a recent tender action. After consultation with industry the transmission-line backplane specification is also complete and quotations are being obtained for design and manufacture.

We aim to produce sufficient modules for the minimal system by the end of 1995, and we have a milestone to install this system in the ATLAS test beam in March 1996. During the first half of 1996 the full demonstrator system will be assembled, with a milestone of test-beam installation in June 1996.

By 1997 the aim is to achieve sufficient understanding of the technologies under study in the demonstrator systems (including that of the Stockholm group – see section 6.6.2) to allow well-informed technology choices to be made by ATLAS.

6.6 Related Work

6.6.1 Overall Level-1 Work

The overall level-1 trigger is made up of several sub-systems, as shown in figure 28. The UK groups are working solely on the calorimeter trigger processor, and other groups in the ATLAS collaboration are responsible for the other sub-systems.

The muon trigger processor is the responsibility of the Rome group. CERN groups are working on the central trigger processor, which receives summary information from the calorimeter and muon trigger processors to produce an overall level-1 trigger decision, as well as the central timing, trigger and control distribution system. CERN is also responsible for the region-of-interest unit (RoI builder), which passes information assembled from the calorimeter and muon trigger processors to the level-2 trigger.

In the general area of calorimeter front-end electronics there are still parallel solutions under study by several non-UK groups (e.g. FERMI, analogue pipeline techniques, etc.).

6.6.2 Demonstrator Programme of the Stockholm Group

The Stockholm group is pursuing the design of a level-1 calorimeter trigger processor designed to explore the potential advantages given by alternative architectures and very advanced technologies [29]. The design involves a high-density MCM for opto-electrical conversion of input data, and two highly-complex processing ASICs performing bit-serial arithmetic. The bit-serial architecture, which is fundamental to their design, demands very high clocking speeds in these processing ASICs.

A technical demonstrator programme intended to verify the system performance has been funded and is under development. Prototype ASICs, MCMs and modules will be produced and evaluated in test-beam studies during 1996. Depending on the outcome of these tests, the trigger design presented in the ATLAS technical proposal may be modified to benefit from improved performance and/or reduced cost.

6.6.3 Collaboration with the Heidelberg Group

The UK and Heidelberg groups began collaboration when the phase-1 trigger demonstrator system was used to instrument the TGT liquid-argon calorimeter for test-beam studies as part of the R&D work for RD27. Building on their experience of trigger FADC design, the Heidelberg group subsequently produced a set of customised FADC modules to instrument the UK phase-2 BCID and trigger demonstrator systems, and they will participate in all future test-beam activities with the UK groups.

The Heidelberg group has also recently established an ASIC design facility, and an early project is the design of an ASIC to replicate the Xilinx FPGA in the UK BCID programme. A future generation of devices could incorporate higher channel-density, more sophisticated algorithms and higher processing speeds. It is expected that, together with the FADC expertise, this will lead to an increasing involvement in the general area of front-end level-1 calorimeter trigger electronics for ATLAS.

6.7 Resources

6.7.1 Costing

A detailed cost estimate of the calorimeter trigger has been reviewed by the ATLAS Cost Review (CORE) Committee. It is based on the design in chapter 5 of the ATLAS technical proposal [1] and related backup document [25]. A summary is given in table 13. The construction of the trigger, and its cost, are to be shared among the collaborating institutes. In addition, we have given the cost of the UK demonstrator and prototype programme separately at the bottom of the table.

Cost summary	k£
ADC and BCID system	552
Optical transmission system	977
Optical receiver system	1111
Optical fibres, splitters and connectors	366
Trigger processor	1385
Shipping and commissioning	13
Computers; module test station	133
Module development and repair facility	66
Test boards	40
Total cost of level-1 calorimeter trigger	**4893**
UK fraction (75%)	**3482**
UK demonstrator and prototype systems	250
UK project total	**3732**
Common Fund contribution	**2023**

Table 13: Level-1 calorimeter trigger cost summary.

The estimate covers the cost of the trigger front end, data transmission and trigger processing systems, appropriate spares, a small module testing facility, computers and installation. It also includes infrastructure needed in home institutes for component and board manufacture, testing and repair.

6.7.2 Manpower

The engineering effort required at RAL for the completion of the first level calorimeter trigger is estimated to be 67 staff years from 1995 to 2004. This includes design engineering staff, drawing office staff and design services staff. This is in addition to the 25 staff years which will be contributed by Birmingham and QMW.

6.7.3 Timescale

The detailed timescale given in the backup documents is based on an LHC start date of 2004. The trigger front end must be installed in 2002 with the LAr calorimeter, when the cluster processing section should be fully operational for detector commissioning and readout tests. Manufacture and testing of approximately 100 modules is expected to require two years, and should therefore start in 1999. The trigger concept must be frozen in 1997 to allow time for detailed design and final prototype testing before manufacture begins.

The resulting cost and engineering effort profiles are shown in tables 14 and 15.

Year	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004
Spend (UK k£)	115	80	35	186	431	840	1520	325	100	100
Accumulated (UK k£)	115	195	230	416	847	1687	3207	3532	3632	3732

Table 14: **Level-1 requested spend profile**

Year	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004
Engineering staff (RAL S/Y)	2	2	3	5	6	6	4	4	2	1
Technical staff (RAL S/Y)	0.5	1	1.5	4	4	5	5	5	4	2

Table 15: **Level-1 requested manpower profile**

6.7.4 Cost Sharing

Discussions on resource sharing are underway between the German, Swedish, and UK groups involved in the calorimeter trigger. Although detailed decisions cannot be reached until the trigger technology choices are made in 1997, it is already accepted that each country will contribute to infrastructure as well as having specific design, manufacturing and testing responsibilities.

Excluding CERN and commercial companies, from whom no capital contribution is expected, the UK groups account for significantly more than half of the signatories to the level-1 calorimeter trigger backup document to the ATLAS Technical Proposal. From the earliest stage of the ATLAS trigger work, UK groups have taken the leading role on physics simulation and architectural design studies, and test beam evaluations of trigger prototypes have been performed to date solely by the UK groups. To maintain this dominant role we feel that a UK share of 75% of the project is required.

6.8 Conclusions

The UK groups have established themselves over the last three years as the leading contributors to the ATLAS level-1 calorimeter trigger effort. We have carried out a very innovative and successful programme of trigger processor hardware development firmly based on simulation studies, and we continue to place particular emphasis on the importance of evaluating this hardware in the realistic environment of a test beam. Close working relationships have been developed with the calorimeter community, in particular in the area of front-end electronics where mutually-acceptable technical solutions must be found.

Our lengthy collaboration with the Stockholm group has been mutually beneficial in a number of ways, and we confidently expect to work closely with them after ATLAS has made technology choices in 1997. The collaboration with the Heidelberg group is more recent but is already proving very fruitful. With their strong background in hardware design and development they have made significant contributions to our current demonstrator programme, and together with their plans to build up expertise in ASIC design they would be well placed to contribute to the ATLAS front-end trigger electronics.

We therefore believe that the UK groups lead a very strong international team which is now accepted by ATLAS to be responsible for the design and construction of the level-1 calorimeter trigger system. With world-class electronics facilities, expertise and experience to draw upon, the UK groups are now ideally placed to capitalise on the work which we have done so far and to lead the project over the next decade. Financial and manpower resources commensurate with this leading role are thus sought from the PPESP.

NO FILE: t1$_{d}ata.eps$

Figure 31: Data transmission chain.

NO FILE: t1$_{d}emo.eps$

Figure 32: Demonstrator system block diagram.

7 The ATLAS Level-2 Trigger

7.1 Physics Rates and Signatures

The level-2 trigger is required to reduce the level-1 trigger output rate to that which can be accommodated by the event builder. After allowing for uncertainties in those rates, the design criteria for the level-2 trigger at high luminosity ($10^{34}\ cm^{-2}s^{-1}$) are an input rate of 100 kHz and an output rate of 1 kHz. To achieve a rate reduction of this factor it is necessary to operate with new algorithms on full granularity data from the sub-detectors and to combine their information. It is not sufficient to repeat the level-1 algorithms with improved resolution.

Table 16 shows the input and output trigger rates expected from simulation work from inclusive trigger selections at level-2. Table 17 shows how these triggers can be used to select physics processes. Substantial improvements in selectivity are expected from applying topological constraints in the level-2 trigger and further studies will be necessary to examine this additional rejection power.

At low luminosity ($10^{33}\ cm^{-2}s^{-1}$), the 'high-luminosity' programme will be supplemented by measurements on the B system [30]. B-physics triggers will need to operate in parallel with the 'high-luminosity' triggers and the level-2 system will be designed to run them simultaneously.

7.2 ATLAS level-2 Trigger

7.2.1 Overview

At high luminosity, the total data rate from the detector after a level-1 trigger is around 150 GByte/s. To reduce the data transfer requirements into the level-2 trigger system, the overall philosophy adopted is to use guidance from level-1 to select the data to be processed. This guidance is in the form of pointers in $\eta - \phi$ space to regions of interest (RoIs) which correspond to significant transverse-energy deposits in the calorimeter or tracks in the muon trigger chambers. Only data from within a region of interest are transferred to the level-2 system for processing. This reduces the data volume to be transferred by up to two orders of magnitude.

As shown in Fig. 33, level-2 data processing is divided into two main steps.

- Feature extraction is used to reduce the data from one sub-detector from basic cell information to more physical quantities (e.g. for a calorimeter these would be cluster parameters).
- Features for all RoIs from all appropriate sub-detectors are combined and a global event decision is made.

In general, feature extraction can take place in parallel for each RoI in each sub-detector. In some regions of the detector, however, it may be necessary for information from two sub-systems to be combined for satisfactory feature extraction, for example in the overlap area between barrel and forward sub-systems.

7.2.2 Architecture

The basic level-2 architecture [?] is shown in Fig. 33. All data are moved off the detector after a level-1 trigger and transmitted to control rooms on the surface where they must reside in temporary buffers during the level-2 trigger decision time. Data from sub-detectors are grouped so that the rate into each buffer is approximately 100 MByte/s and the total number of buffers is around 1700.

Information from the different parts of the level-1 trigger system is gathered together in an RoI builder. This information is passed to the level-2 supervisor which is responsible for the overall control of the level-2 system. The supervisor sends the RoI information, together with any processor allocation information, to the level-2 buffers via an RoI distribution system, with a similar distribution system used for the final level-2 decisions received from the global processors.

Because data for one RoI in a sub-detector can be spread across a number of buffers, a network is required to gather the RoI data into one processor for feature extraction. After feature extraction, the data are passed through another network to one of a set of global processors. The feature extractors and the global processors are assumed to be programmable processors with a processing time long compared with 10 μs so that many of them are needed to cope with an input data rate of 100 kHz.

A critical parameter for the level-2 system is the latency. Increased latency implies that larger buffers are required to store the data during the level-2 decision, but, more significantly, that more processors are required in the system as the processing of more events overlap in time. To minimise the latency in the system, the overall philosophy adopted for high luminosity running is to divide processing into parallel tasks where possible. For

Table 16: List of level-1 and level-2 trigger requirements and associated rates at high and low luminosity

Trigger requirement	level-1 rate (kHz)	level-2 rate (kHz)
Luminosity $\mathcal{L} = 10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$		
≥ 1 μ $p_T > 20$ GeV ($1\mu_{20}$)	4	
≥ 1 isolated μ $p_T > 20$ GeV ($1\mu_{20}$I)		0.2
≥ 1 μ $p_T > 40$ GeV ($1\mu_{40}$)		0.1
≥ 1 isolated em cluster $E_T > 30$ GeV ($1\mathrm{em}_{30}$)	20	
≥ 1 e $E_T > 30$ GeV ($1\mathrm{e}_{30}$)		0.3
≥ 1 γ $E_T > 60$ GeV ($1\gamma_{60}$)		0.1
≥ 2 μ $p_T > 6$ GeV ($2\mu_6$)	1	
≥ 2 μ $p_T > 10$ GeV ($2\mu_{10}$)		0.08
≥ 2 isolated μ $p_T > 6$ GeV ($2\mu_6$I)		0.1
$\mathrm{B_d^0} \to \mu^+\mu^-$, $\mathrm{B_s^0} \to \mu^+\mu^-$		0.01
≥ 2 isolated em clusters $p_T > 20$ GeV ($2\mathrm{em}_{20}$)	4	
≥ 2 e $p_T > 20$ GeV ($1\mathrm{e}_{20}$) **or** ≥ 2 γ $p_T > 20$ GeV ($2\gamma_{20}$)		0.2
≥ 1 jet $p_T > 150$ GeV ($1\mathrm{j}_{150}$)	3	
≥ 1 jet $p_T > 300$ GeV ($1\mathrm{j}_{300}$)		0.1
≥ 3 jets $p_T > 150$ GeV ($3\mathrm{j}_{150}$)		0.04
Large E_T^{miss} (E_T^{miss})	1	0.1
Other prescaled triggers	5	0.1
Total	$\lesssim 38$	$\lesssim 1.4$
Luminosity $\mathcal{L} = 10^{33}\mathrm{cm}^{-2}\mathrm{s}^{-1}$		
≥ 1 μ $p_T > 6$ GeV ($1\mu_6$)	8	
B-physics LVL2 triggers		0.8
≥ 1 μ $p_T > 20$ GeV ($1\mu_{20}$)		0.2
≥ 1 isolated em cluster $p_T > 20$ GeV ($1\mathrm{em}_{20}$)	10	
≥ 1 e $p_T > 20$ GeV ($1\mathrm{e}_{20}$)		0.2
≥ 1 γ $p_T > 40$ GeV ($1\gamma_{40}$)		0.06
≥ 2 isolated em clusters $p_T > 15$ GeV ($2\mathrm{em}_{15}$)	2.5	
≥ 2 e $p_T > 15$ GeV ($2\mathrm{e}_{15}$)		0.01
≥ 2 γ $p_T > 20$ GeV ($2\gamma_{20}$)		0.01
≥ 1 jet $p_T > 100$ GeV ($1\mathrm{j}_{100}$)	0.9	
≥ 1 jet $p_T > 200$ GeV ($1\mathrm{j}_{200}$)		0.06
≥ 3 jets $p_T > 100$ GeV ($3\mathrm{j}_{100}$)		0.02
Large E_T^{miss} (E_T^{miss})	0.1	0.01
Other prescaled triggers	1	0.1
Total	$\lesssim 23$	$\lesssim 1.5$

Table 17: Representative list of physics processes and triggers through which they would be selected at high luminosity. The notation for the different triggers is defined in Table 16.

Process	LVL1 trigger	LVL2 trigger
$(W \rightarrow \ell\nu) + X$	$1\mu_{20}$	$1\mu_{20}I$
	$1em_{30}$	$1e_{30}$
$(Z \rightarrow \ell^+\ell^-) + X$	$2\mu_6$	$2\mu_6I$
	$2em_{20}$	$2e_{20}$
	$1\mu_{20}$	$1\mu_{20}I$
	$1em_{30}$	$1e_{30}$
$H \rightarrow \gamma\gamma$	$2em_{20}$	$2\gamma_{20}$
$H \rightarrow ZZ^* \rightarrow 4\ell$	$2em_{20}$	$2e_{20}$
	$2\mu_6$	$2\mu_6I$
	$1em_{30}$	$1e_{30}$
	$1\mu_{20}$	$1\mu_{20}I$
$A^0 \rightarrow \tau^+\tau^-$	$1\mu_{20}$	$1\mu_{20}I$
	$1em_{30}$	$1e_{30}$
$t\bar{t} \rightarrow \ell^+\ell^- + X$	$2\mu_6$	$2\mu_6I$
	$2em_{20}$	$2e_{20}$
	$1em_{30}$	$1e_{30}$
	$1\mu_{20}$	$1\mu_{20}I$
$t\bar{t} \rightarrow \ell^\pm\nu$ + jets	$1\mu_{20}$	$1\mu_{20}I$
	$1em_{30}$	$1e_{30}$
SUSY $\rightarrow$ leptons	$1\mu_{20}$	$1\mu_{20}I$
	$1em_{30}$	$1e_{30}$
QCD jet studies	$1j_{150}$	$1j_{300}$
W', $Z' \rightarrow$ jets	$1j_{150}$	$1j_{300}$
SUSY $\rightarrow$ jets	$1j_{150}$	$3j_{150}$
	E_T^{miss}	E_T^{miss}
B-physics	$1\mu_{20}$	$1\mu_{40}$
	$2\mu_6$	$2\mu_{10}$
		$B^0 \rightarrow \mu^+\mu^-$

example, RoIs in each sub-detector are processed in parallel in different feature extractors and each sub-detector is connected to an independent local processing system.

At low luminosity, the trigger rate and sub-detector cell occupancy are substantially lower, and a trigger which uses a sequential set of operations (and is compatible with the high luminosity architecture) is being studied. The process is to refine the muon trigger selection using the precision chambers and then to process the TRT data to find tracks above about 1 GeV/c in p_T. For regions of the detector around the TRT tracks, data from the silicon tracker and the calorimeter are then evaluated to provide information to the global processors where mass cuts can be applied to select the required physics signatures. As the luminosity is increased above $10^{33}\ cm^{-2}s^{-1}$ the muon threshold can be raised to maintain the trigger rate within the limits set by the level-2 system.

7.2.3 System Components

Personality cards are required for each sub-detector, between the input data streams and the level-2 buffers, to format the data into a common frame appropriate for the level-2 trigger and event building. Liaison with sub-detector groups to define these cards is starting.

The level-2 buffer accepts data from the sub-detector via the personality card and stores them during the level-2 decision time. On receipt of a message giving the event identifier and relevant information from the level-2 supervisor via the RoI distributor, the buffer pushes the trigger data into the level-2 system. A level-2 accept signal causes the buffer to push the full event data to the level-3 network and then to release the buffer space for further events. On a level-2 reject signal, the buffer space is released. By including the capability to pre-process the trigger data, in or close to the level-2 buffer, substantial savings can be made in the network bandwidth required. For calorimeter jet data, for example, there is little point in transferring basic cell data to the feature extractor.

The local network must route data for one RoI from a number of buffers for one sub-detector to a single feature extractor. Among critical issues for the networks in the system are latency and data integrity. The network for each sub-detector has to handle events containing around 5 RoIs at 100 kHz event rate. However the performance of any part of the network depends on the connectivity demanded, e.g. the average rate at which one data buffer in the calorimeter system is asked to supply data is less than 5 kHz. The volume of data to be passed to the feature extractor for one RoI depends on the sub-detector and the degree of pre-processing in the data buffer. For an electromagnetic cluster trigger, the calorimeter RoI data volume is about 1.5 kBytes but this is spread over several buffer sources (the number depends on the position of the RoI relative to the buffer coverage) and the network must be capable of handling a significantly higher data volume per RoI. This leads to a throughput requirement for a sub-detector local network of between one and five GByte/s.

Feature extraction is performed in the local processors which need to be fast with good I/O response. Measurements have been made on a number of systems for current TRT, SCT and calorimeter algorithms [31] but the overall performance of the processors in a realistic situation must be tested. For a 300 μs execution time of the complete algorithm including handling the I/O and any data formatting required, with 5 RoIs and 50% utilisation, 300 local processors are required for one sub-detector. For the calorimeter algorithm, current processors with about 100 Mips equivalent performance can satisfy this requirement. For the TRT and SCT algorithms, processors with hardware accelerators are needed. The estimated total computing power in the local processing system is between one and five times 10^5 Mips equivalent distributed over about one thousand processors. Improvements in processor computing power and their I/O handling, in particular, would lead to a dramatic reduction in the number of processors required. Commercial boards with RISC processors and digital signal processors (DSP) are being evaluated.

The global network transfers information for all the RoIs in the event from the feature extractors for the different sub-detectors active for that event to a global processor. The network must connect all feature extractors to all global processors. A high performance network is required to handle the feature data of typically 1-2 kBytes per event at 100 kHz. The global network must also be fault tolerant, and must be flexible enough to allow expansion of the processor farm without latency penalties or excessive reorganisation. At present there is no proven technology which will address the high band-width, low-latency, many-to-one problem in the transmission of many small feature records to a single global processor. Technically the most promising solution is Scalable Coherent Interface (SCI) [32] which uses high speed point-to-point links, and where the total bandwidth scales roughly with the number of nodes. This technology is being used for supercomputer applications and is being developed commercially for various computer connections.

Global processors are organised as a farm operating with a 100 kHz decision rate, running algorithms developed in offline trigger studies and thus requiring high performance general purpose processors. A total time of 400 μs is considered necessary for the tasks of collecting and organising the feature records, and making the global decision, leading to a farm size of approximately 80 processors at 50% occupancy. Wherever possible data collection, formatting and reorganisation should be performed in hardware, and we are developing solutions based on FPGAs. Algorithm tests with current RISC processors do not achieve the full speed required, but with performance increases of a factor of 5-10 likely by the time the final system is required this number of processors should satisfy the requirements. The level-2 decisions from the global processors are passed to the level-2 supervisor via part of the global network.

The RoI trigger builder is required to provide the guidance information to level-2. Information from the level-1 calorimeter, muon and central trigger processors are combined to provide the information on event identification and regions of interest for use by the level-2 trigger. The information is passed to the level-2 supervisor. A design study is in progress to establish the full functional requirements [33]. A circuit based on FPGAs could accomplish this task, but a test using a DSP [34] indicates that a programmable processor may provide a more flexible option if some increase in performance can be achieved.

The level-2 supervisor controls the operation of the level-2 trigger. It receives the event information from the level-1 system, adds, if required, information on routing (including global processor allocation) and passes the modified information to the RoI distributor. Results from the global processors are used to initiate data transfers from the level-2 buffers to the event builder or free the buffer space. Information on transfer and processing errors are passed to the supervisor which also monitors time-outs in the processing chain. A design study is in progress to establish the full functional requirements [35].

The RoI and level-2 decision distributors sit between the level-2 supervisor and the buffers. The RoI distributor guides messages to the appropriate buffers. In this way each buffer does not have to respond to all

RoI messages for every event but only to those which require it to take action. All buffers have to respond to the level-2 decision message at 100 kHz, but in most cases (99%) this is a reject signal which results in the relatively simple operation to free buffer space. An RoI message requires the buffer to organise the movement of data to the level-2 system and a level-2 accept signal requires the buffer to move data to the event builder.

7.3 Current Status of UK Level-2 Activities

A major accomplishment of the group was the successful operation of a small system in the H8 beam line at CERN during September/October 1994 [36]. Invaluable experience was gained by integrating with a real detector providing data. This demonstration provided an existence proof for an asynchronous local/global level-2 trigger system based on our architectural ideas and establishes a firm foundation from which future work can evolve. Much study has also been carried out under test conditions in the laboratory and has started to cross-fertilise architectural modelling work.

In much of the work described below, the UK group has led the field and increasingly other groups have started to contribute.

7.3.1 Beam Test Demonstration

The beam test system (Fig. 34), contained two level-2 buffers [37], one 'link unit', two feature extractors, a 'global gateway', a four node global network and a single global processor. The 'link unit' provided the local network and the 'global gateway' acted as the interface from the local to the global system. The local system components were based on Texas Instruments TMS320C40 (C40) DSP, the global network was based on SCI and the global processor was a DEC Alpha workstation. The buffers and the SCI node interfaces were designed and built 'in-house'. Data were derived from a HIPPI spy unit which formed part of a router system [38] placed in the data readout path of the RD-6 Transition Radiation Detector (TRD) [39]. The whole system was self-triggered by the passage of an event on the RD-6 HIPPI lines. Parasitic operation in the beam line ensured minimal disruption to other parts of the ATLAS tests and enabled the work programme to remain independent of other activities.

In the initial phase of the beam tests only the local part of the system was used. In this phase some 50K events were successfully recorded to disk. An example of an event recorded by the system is shown in Fig. 35. In the second phase, the SCI ring and global processor were added. It is believed that this is the first time that 'live' detector data has been passed round an SCI ring at a beam line.

7.3.2 Laboratory Tests

The level-2 buffer is controlled by buffer manager software. Timing tests of this program have been made with a software emulation of the buffer hardware. Additional DSPs acted as data sources and sinks, so that the I/O environment seen by the buffer manager was essentially the same as in a real system. The performance of the assembler-coded buffer manager was comfortably above the design goal of 100 kHz event rate. The results of these software-based timing tests are consistent with those obtained using a hardware level-2 buffer driven by a SLATE [40] event generator board.

For the 'link unit' tests, one C40 was used to send RoI data randomly to each of a set of link unit processors. With only a limited number of units available, interconnections have been wrapped around to simulate a fully connected mesh system. Tests have been run using two and three interconnected link units. Fifteen million events with event sizes between 1 and 2 kBytes were transferred through the system with zero errors yielding a link unit throughput of a approximately 20 MByte/s.

In the laboratory, tests of the SCI components have been made at data rates approaching the limits of our first generation SCI hardware [41]. In two node tests we have achieved ring occupancy of over 20%, and have investigated the latency effects associated with packet collision on the SCI ring. The correct operation of the custom SCI interfaces have been confirmed in this regime, and it has been shown how performance will degrade as the system scales. An understanding of these details is important input to the modelling studies and for the determination of the best ways to incorporate and use this technology in future interfaces.

Investigations have also started into the way the PCI local bus is driven by the DEC Alpha processor (21066), and the best way to access the processor memory system for optimal flow of feature data from the global network. Including PCI overheads, data transfer at a rate of 80 MByte/s has been observed - implying a transfer latency of about 25 μs for all of the feature data for an event from the SCI interface into the memory.

Item	Responsible	Other Contributors
ID interface	UCL	RHBNC, ID groups
Buffers	RHBNC/UCL	
Local processing	RHBNC/UCL	
Node interfaces	Manchester	RAL
Networks	Manchester/RAL	
Global processing	RAL	Manchester
Modelling	Oxford	RAL, RHBNC, UCL
Trigger simulation	RHBNC/UCL	Oxford

Table 18: Level-2 areas of responsibility

7.3.3 Modelling

Members of the UK group have played a key part in setting up and directing a broad collaboration of people to model the performance of multi-level DAQ/Triggering systems based on networks and multi-processing. In addition, they have taken on the responsibility of developing and maintaining the core of the software.

A modelling system, SIMDAQ [42], has been developed based on the object-oriented simulation language MODSIM II. Input files of data generated from physics simulations and of detector readout segmentation allow architectures to be studied under realistic conditions.

The first implementation of this system has been applied to simulations of level-2 trigger architectures of the type studied by the UK groups. The performance of the level-2 trigger has been evaluated for three ATLAS sub-detectors, the electromagnetic and hadron calorimeters, and a tracking detector, the TRT. SIMDAQ has proved flexible and studies using it have provided valuable information on the performance requirements of system components.

Because test systems will be constructed on a scale small compared with ATLAS, modelling will provide the only way of assessing full scale architecture performance. Modelling, therefore, will remain a central component of the UK activity. Measurements on test systems and components will be used to provide input to models and results from the modelling of full scale systems will be used to assist in the specification of component parts.

7.4 UK Responsibilities

Discussions on the division of responsibilities in the level-2 trigger are only just starting and the programme described below takes into account our best evaluation of other group's preferences. The UK groups support and complement each other in their range of interests, experience and expertise. Based on these strengths, we propose to work on the development of the local level-2 trigger system for the inner detector, the global level-2 trigger system, physics studies in relevant areas (including B-physics triggers) and system modelling for the trigger and data acquisition.

In this proposal we bid for the construction of 75% of the level-2 local system for the inner detector and for the construction of the level-2 global system. The RHBNC and UCL groups will take responsibility for the buffers, local processing, physics studies and tracking algorithm development. The Manchester and RAL groups will take responsibility for the networks, global processing and global algorithm developments. The Oxford group will lead the modelling activity and participate in the algorithm development. Table 18 shows further details.

The significant UK participation in the inner detector makes it sensible and efficient for part of the level-2 activity to be concentrated in this area. The work, in collaboration with the inner detector group, will be on the development of off-detector hardware for the inner detector and on the algorithms for track recognition for both triggering and off-line analysis. UK groups have been working on high performance networks with tightly integrated RISC processors, and are now starting to investigate how this promising technology can be optimised for global processing. These activities will lead naturally to the UK responsibilities outlined above, where the scale of the proposed activity is commensurate with the size and strength of the UK groups involved.

7.5 Work Programme

The work programme is divided into three phases. The current phase is to prove architectural ideas and examine generic problems and will lead to an architecture choice at the end of 1997. This choice will be followed by a period of technology development and assessment resulting in technology selection for the level-2 system components around 2000. The third stage is the final design, construction and operation of the system.

The UK groups will continue with the development and exploitation of their current systems during the first phase and will move to improved devices and better technologies if and when these become available.

7.5.1 Short Term (1995-97) - Evaluation and Design

For a system of the complexity of level-2, which depends on the interaction of several thousand processors, the monitoring and control of the system performance is vital. Each part of the system must be testable independently, and as a whole, without modification of any of the connections in the system. Fault tolerance must be built-in. With data spread across many memories and processors, the system must be designed to tolerate the loss of single components without serious compromise to the overall performance. Rapid reconfiguration of the system is required to circumvent failed components. For areas where reconfiguration does not or cannot help, high reliability of components will be essential. These issues are central to the ability of the system to operate reliably.

With many processors active on many different events simultaneously, the performance of the system as a whole must be considered. It is insufficient to make measurements on each component of the system in isolation. It is imperative that complete systems are modelled and tested in the laboratory before serious architecture and technology comparisons can be made. For this reason, the twin activities of modelling and laboratory (and test beam) demonstrations are vital elements of the level-2 trigger programme in both the short and medium terms.

Over the next 3 years the work will continue with a balanced programme of modelling, simulation, and tests both in the laboratory and at a test beam. Many issues need to be studied including RoI guidance, integration of multiple detectors, fault tolerance, error-recovery, optimization of the use of network bandwidth and compute power, initialization procedures, monitoring and control. In parallel, activities concentrated on the definition of data formats, the development of prototype local and global algorithms and the specification of level-2 supervisor functionality will be conducted. At all stages the results of laboratory tests will be used as input to the modelling activity. The modelling will seek to simulate the performance of the test system and to estimate the performance of full scale sytems.

Preparations for this test work will include the development of a front end to the current prototype level-2 buffer to accept data from the silicon detectors. This will be done in collaboration with the ATLAS UK groups working on the inner detector. High bandwidth, low latency interfaces optimised for the global system will also be developed.

This work will be conducted in close collaboration with many non-UK partners working on complementary parts of the level-2 system. At the end of this phase, decisions on details of architecture and specific technologies will be made by ATLAS and will be adopted by the UK group for subsequent phases.

7.5.2 Medium Term (1998-2000) - Large Scale Prototype

In this phase a large scale prototype will be constructed with the chosen architecture and candidate technologies will be subjected to rigorous tests and optimization. This will include evaluation of the physics performance of the full system design and the definition of diagnostic procedures.

This work will take the form of construction of a complete slice through the level-2 trigger system (both local and global), permitting the inner detector and the level-2 trigger to be tested. The connection to the inner detector prototype will provide the level-2 group with real data and therefore realistic tests.

The prototype tests will be accompanied by further modelling work to ensure optimum and scalable system performance.

7.5.3 Long Term (2001-04) - Production and Integration

The final phase is sub-divided into procurement or construction, module tests, integration and initial operation. Table 19 shows the number of modules that will be required and indicates the full scale of the project.

Item	**number**
Input to Inner Detector Buffers (GByte/s)	20
Number of Inner Detector Buffers	240
Number of Feature Extractor Processors	350
Local Processor power (MIPs/processor)	500
FeX processing time (μs)	350
Local network throughput (MByte/s)	2000
Global Processors	80
Global Processor power (MIPs/processor)	1000
Global processing time (μs)	400
Global network throughput (MByte/s)	200

Table 19: Estimates of system size and requirements for the inner detector local system and the global system

Item	**total**	**fraction**	**total**
Inner detector buffers	1440	75%	1080
demonstrator	140	75%	110
local system	3600	75%	2700
demonstrator	360	75%	270
Total (kCHF)	5540	75%	4160
global system	1530	100%	1530
demonstrator	230	100%	230
Total (kCHF)	1760	100%	1760
Grand Total (kCHF)	7300		5920

Table 20: CORE costings for the inner detector buffers and local system, and the global system

The UK expertise in high performance networks and tightly integrated RISC processors will be brought to bear in the specification of modules to be purchased commercially or to be built ‘in-house’. The latter being necessary to achieve the fully optimised performance required.

All modules must undergo test procedures to ensure quality and reliability of the final system. To this end, these procedures will be defined as appropriate.

Integration of components will not only involve bringing together parts of the local and global sub-systems, but also the connections to sub-detectors, to the level-3 event building and DAQ system and to the level-2 supervisor. The final local and global trigger algorithms will be implemented and put to test.

Final debugging and test of the full system will be during the year 2003 and will include the implementation of full scale initialization, monitoring, control and diagnostic procedures. This should ensure a reliable level-2 system for production operation in 2004, able to efficiently trigger on candidate physics processes.

7.6 Resource Tables

Year	pre-96	96	97	98	99	00	01	02	03	04
Spend (kCHF)	150	100	110	150	100	500	2000	2500	200	100
Accum. (kCHF)	150	250	360	510	610	1110	3110	5610	5810	5910

Table 21: Level-2 spend profile

Year	96	97	98	99	00	01	02	03	04
Physicists	10	11	11	12	12	13	13	13	13
Engineers	6	6	7	7	7	7	7	7	7
Technicians	4	5	5	6	6	7	7	5	5

Table 22: University and RAL PPD staff for level-2 (excluding students)

Year	pre-96	96	97	98	99	00	01	02	03	04
Electronics SYs	-	2	3	3	4	8	8	8	8	6
Accumulated SYs	-	2	5	8	12	20	28	36	44	50

Table 23: Level-2 RAL Engineering Staff request

7.7 Conclusions

The UK groups have made substantial contributions to the work on the level-2 trigger within ATLAS and play a leading role in this activity. The programme outlined allows the groups to maintain a significant profile during the design and development stages and to provide a substantial section of the level-2 trigger. The work programme is well matched to the experience and expertise in the UK groups and provides an interesting and varied programme of work covering many aspects of the trigger activity. The proposed spread of trigger activities, spanning from level-1 through local level-2 to the global level-2 system, gives the UK activities breadth and cohesion. By concentrating the local system work on the connection to the inner detector, the coherence of the UK efforts is further strengthened.

NO FILE: t2$_{f}ig1.eps$

Figure 33:

NO FILE: t2$_{f}ig2.eps$

Figure 34:

NO FILE: t2$_{f}ig3.eps$

Figure 35:

NO FILE: t2$_{f}ig4.eps$

Figure 36:

8 Summary of Requests

8.1 Human Resource Requirements

Institute	Physicists	Engineers/Appl.Phys.	Programmers/Phys.Prog.	Technical Support
Birmingham	4.0	1.0	0.5	1.5
Cambridge	2.5	2.5	1.5	3.0
RAL PPD				
Glasgow	3.75	1.5	1.0	3.0
Lancaster	2.0	1.0		2.0
Liverpool	4.25	3.0	1.5	4.0
QMW, London	3.0	3.0	1.5	3.5
RHBNC, London	4.0	1.0	1.0	2.5
UC, London				
Manchester	3.25	3.5	7.5	
Oxford	6.5	4.5	2.0	6.0
Sheffield	2.5			2.0

Table 24: **Overall Manpower Effort During the Construction Phase**

8.2 Schedule

8.3 Spend Profile

Item	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	Total
Precision Tracking											
Spend (UK K£)	170	650	1080	3400	3570	2800	1850	700	300	100	14620
Manpower (S/Y)	19	33	48	52	49	50	39	30	23	16	359
Level 1 Trigger											
Spend (UK Pounds)	115	80	35	186	431	840	1520	325	100	100	3732
Manpower (RAL S/Y)	2.5	3	4.5	9	10	11	9	9	6	3	67
Level 2 Trigger											
Spend (UK Pounds)	82	56	61	83	56	278	1111	1389	112	55	3283
Manpower (RAL S/Y)		2	3	3	4	8	8	8	8	6	50
Not final	*	*	*	*	*	*	*	*	*	*	
Possible CF contribution (in k£)		455	550	620	3710	3870	740	605	240	230	11020

Table 25: **Profile of Requested Spend and Additional Manpower**

The ATLAS UK groups have built up leadership positions in their chosen areas of the detector; as well as in the overall project management where appointments are made to management positions after receiving nominations from the whole collaboration. All major decisions must be ratified by the Collaboration Board, while the running of the project is delegated to the Executive Board, consisting of experts in each area. The detailed technical work on each system is led by a Steering Group.

Current UK positions of responsibility are:

- P.P.Allport. Member of SCT Steering Group. Resposible for silicon strip detectors.
- P.S.L.Booth. Member of the Inner Detector Review Panel, responsible for internal refereeing of this system.
- C.M.Buttar. Member of SCT Steering Group. Responsible for gallium arsenide strip detectors.
- A.A.Carter. Member of SCT Steering Group. Responsible for detector module coordination.
- J.D.Dowell. Deputy Chairman and Chairman elect of the Collaboration Board. Member of the ATLAS Executive Board. (In the past he has also chaired the internal review panel which recommended the choice of overall calorimeter design).
- S.M.Fisher. Member of the Computing Steering Group.
- C.N.P.Gee. Member of the Trigger/DAQ Steering Group with responsibility for the Level 1 Trigger.
- F.J.Harris. Member of the Trigger/DAQ Steering Group with responsibility for Architecture Modelling.
- R.B.Nickerson. Member of SCT Steering Group. Responsible for detector alignment.
- P.R.Norton. Member of the ATLAS Executive Board. Member of the Muon System Steering Group with special responsibility for the design of the End Cap Toroids.
- S.O'Neale. Member of the Computing Steering Group.
- M.A.Parker. Member of the ATLAS Executive Board. Chairman of the Inner Detector Steering Group, with overall responsibility for this subsystem. (He previously chaired the Hadron Calorimeter Panel, which reviewed the choice of technologies for this subsystem. He was also selected by the collaboration to present the ATLAS technical proposal to the CERN LHCC in its open session.)
- K.M.Smith. Member of the Inner Detector Steering Group with responsibility for Gallium Arsenide detectors.
- J.A.Strong. Member of the Trigger/DAQ Steering Group with responsibility for the Level 2 Trigger.
- G.J.R.Tappern. Member of the Inner Detector Steering Group as Project Engineer, responsible for all engineering issues in this system.
- M.Tyndel. Member of the ATLAS Executive Board. Member of the Inner Detector Steering Group. Chair of SCT Steering Group.

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