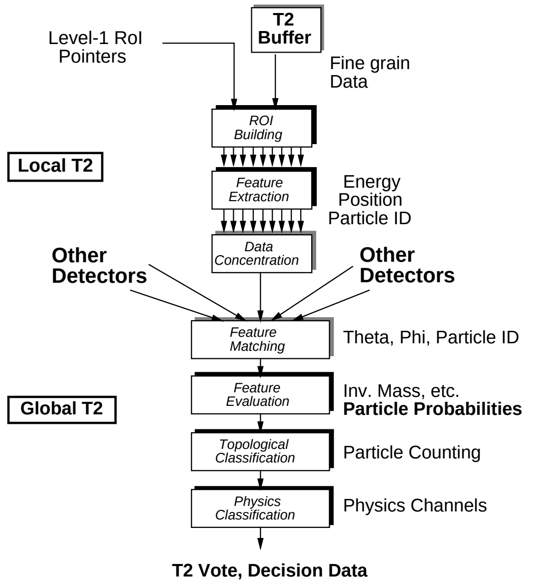


Figure 1. Functional architecture of a second level trigger system.

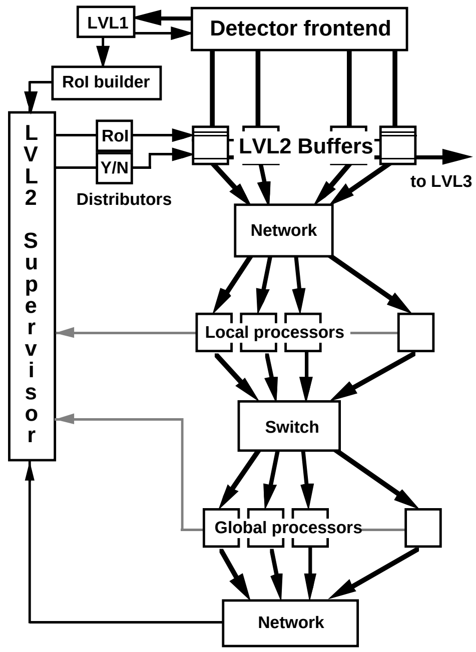


Figure 2. Block diagram of a second level trigger system implementation.

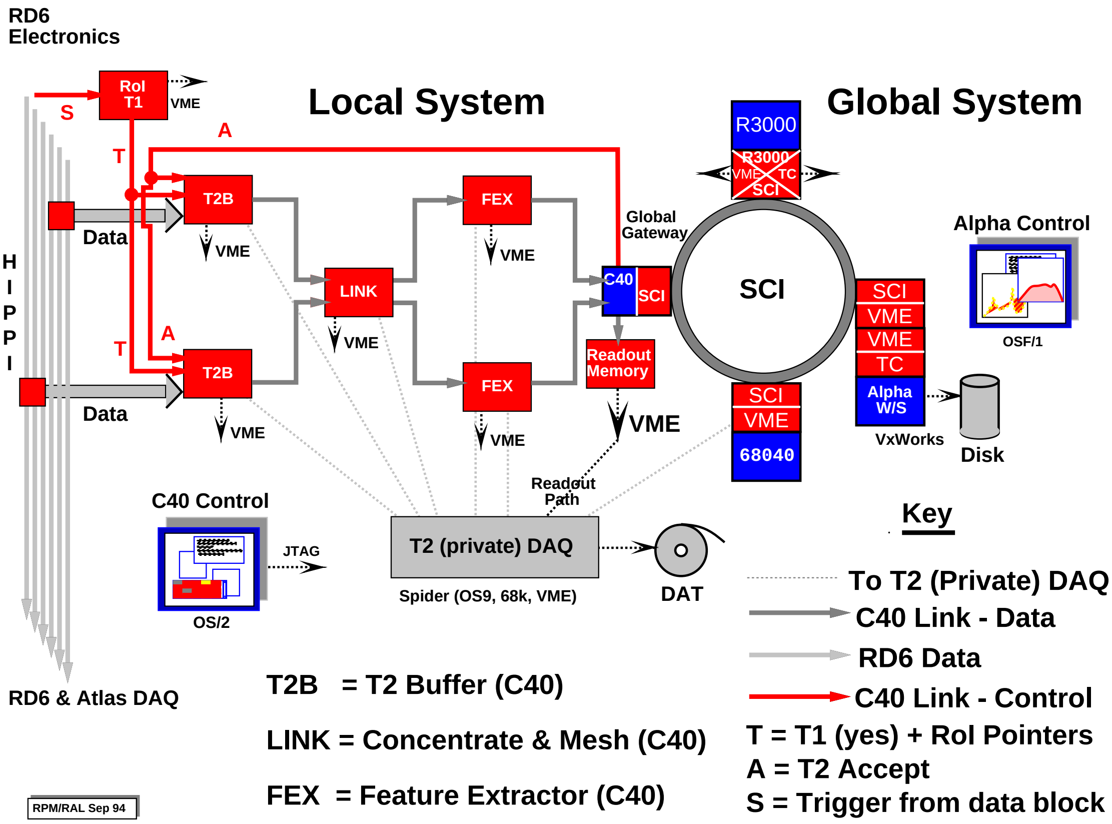
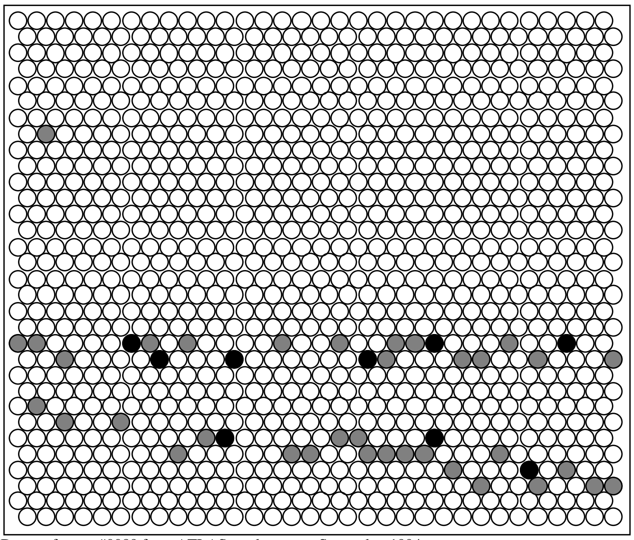


Figure 3. Test beam set-up, autumn 1994.



Dump of event #0089 from ATLAS test beam run September 1994

Figure 4. Example event recorded by the test beam system.

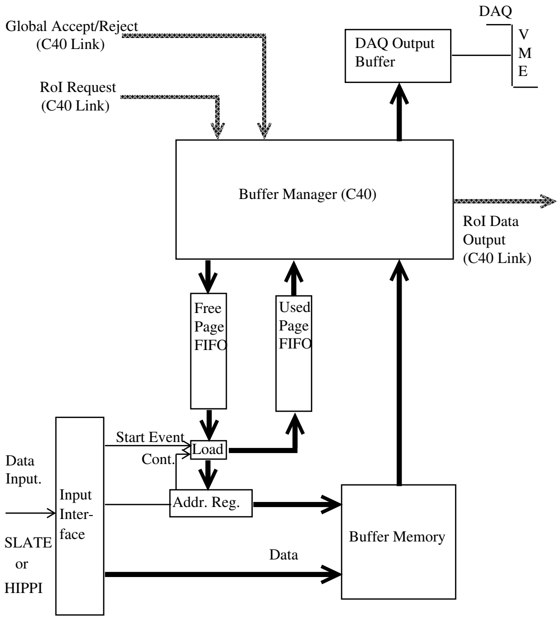


Figure 6. T2 buffer design.

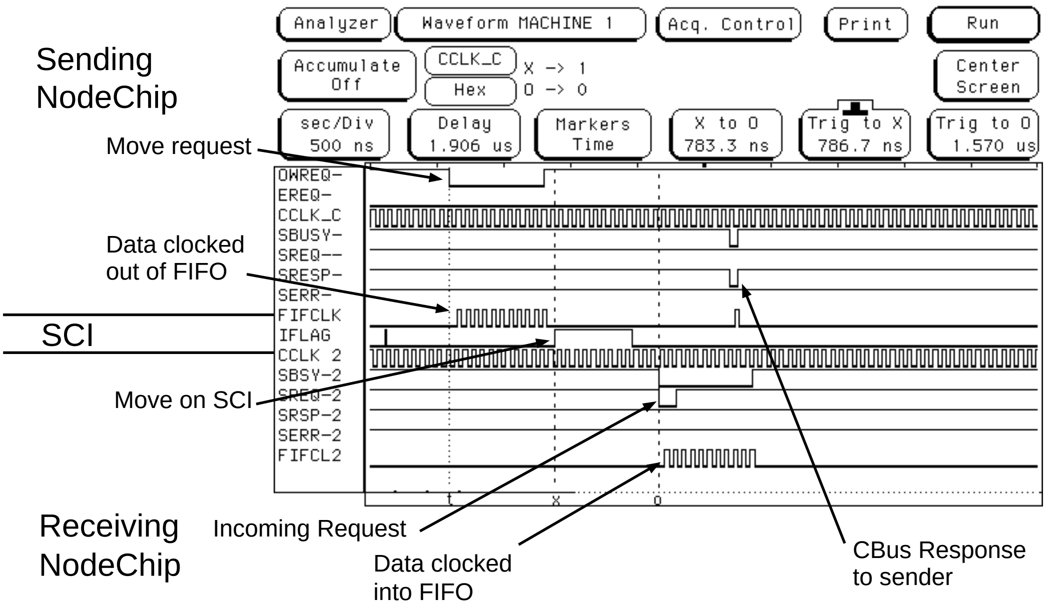


Figure 5. Logic Analyser trace for an SCI move.

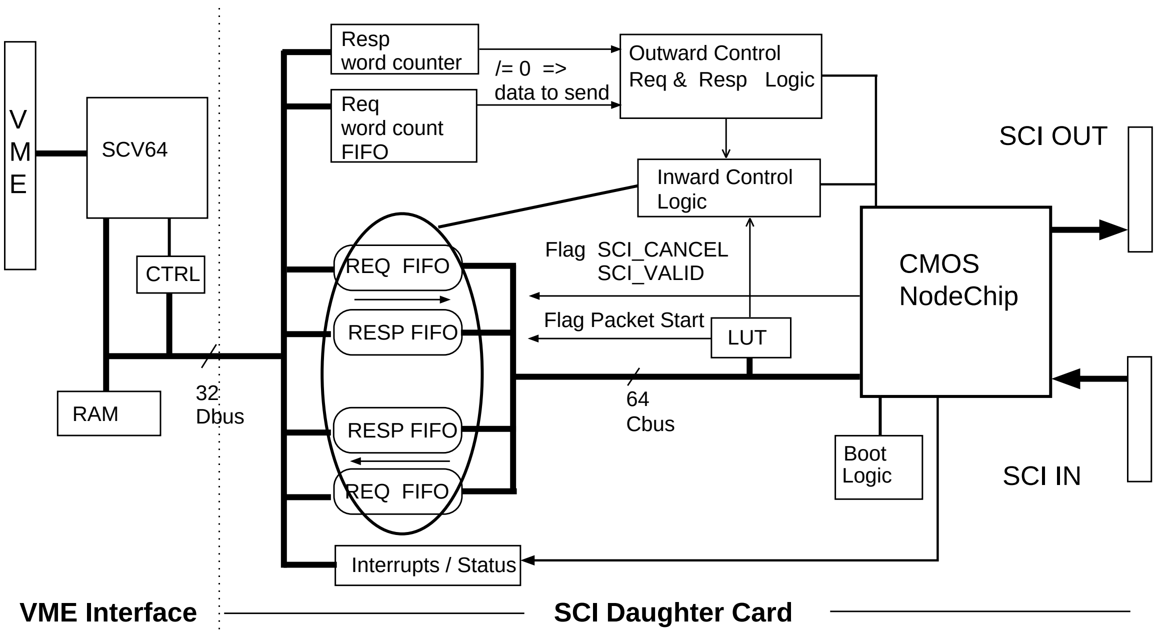


Figure 7. Block diagram of the SCI Daughter Card.

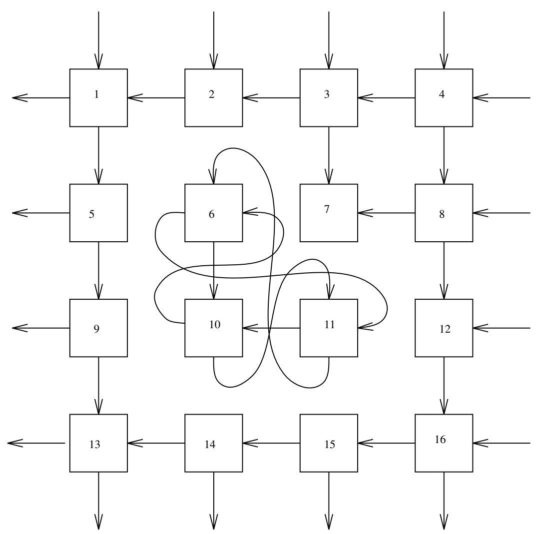


Figure 8. Using 3 Link Units to simulate a complete mesh.

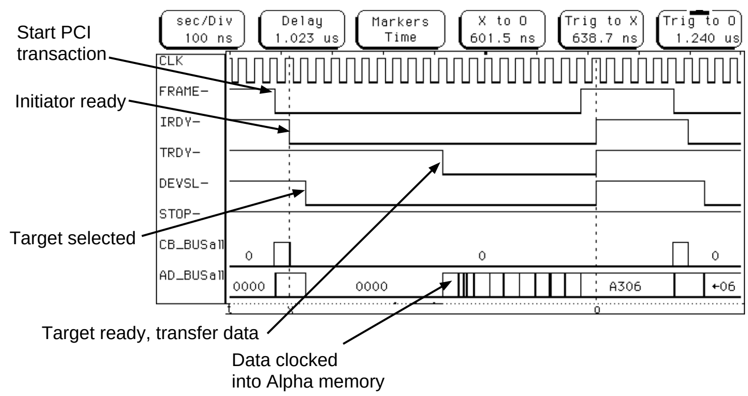


Figure 9. Logic Analyser trace for a PCI DMA to Alpha memory.

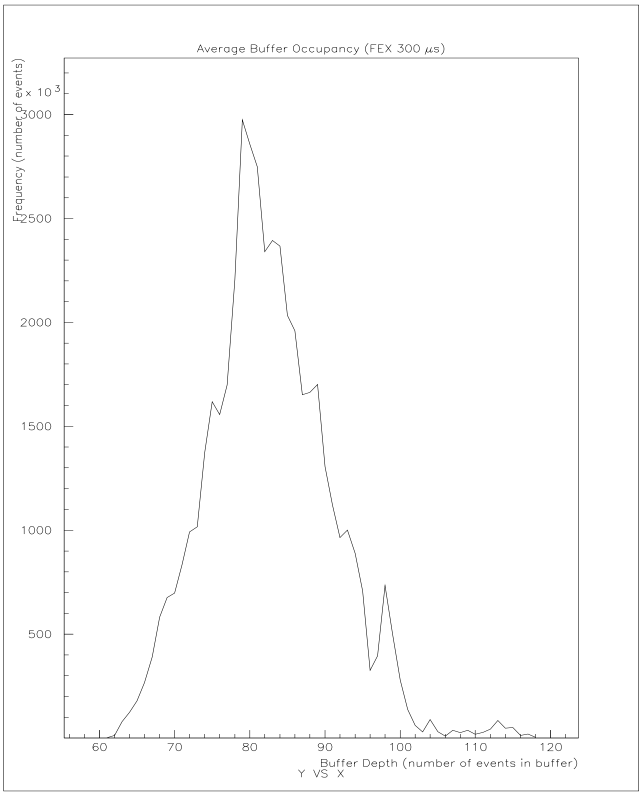


Figure 10. Example result from modelling a second level trigger system with an SCI network.

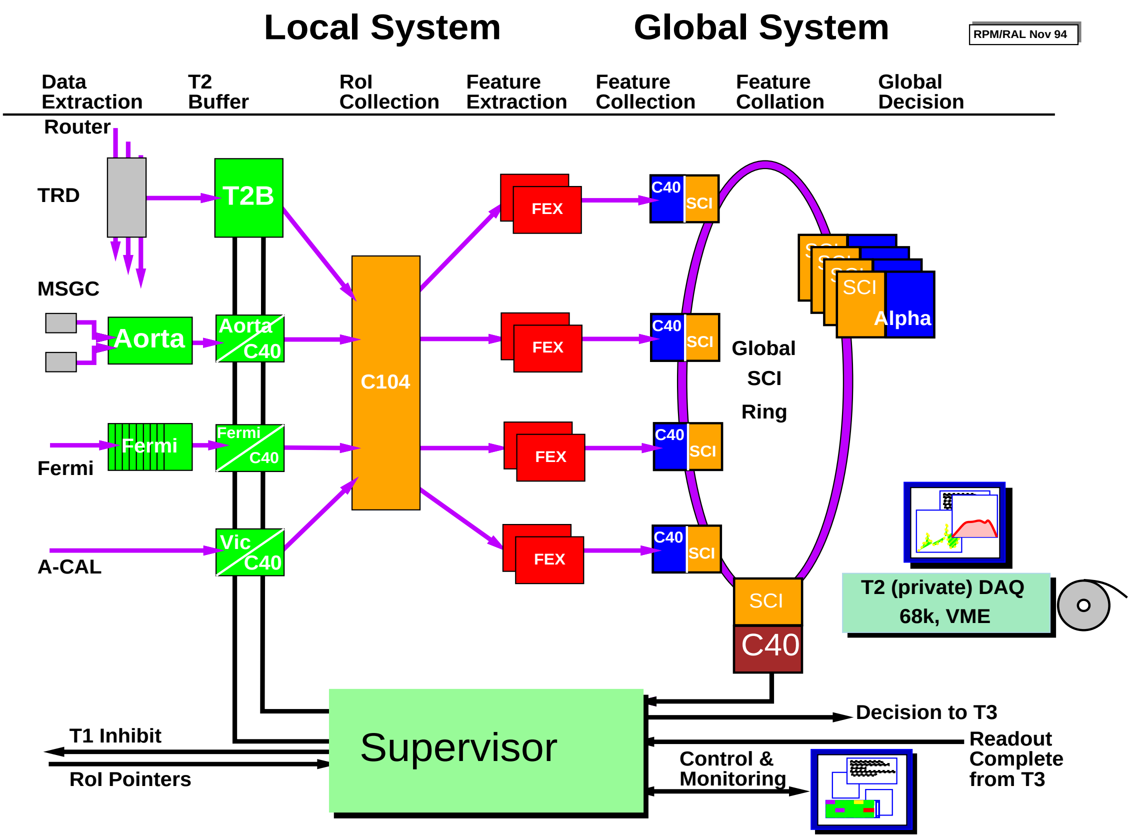


Figure 11. Test beam set-up for 1995.