**Clock and control board to DIF board interface**

# System Architecture

Clock and Control Board

5 MHz Clk generator

DIF 1

DIF 3

DIF 2

**HDMI link**

External trigger

**RS232**

PC

**USB**

# Signals between CCC and DIF

|  |  |  |  |
| --- | --- | --- | --- |
| **HDMI pin** | **CCC name** | **DIF name** | **use** |
| **1-3** | LCK\_OUT | LDA\_CLK (in) | 5MHz CLK |
| **4-6** | LCONT\_OUT | LDA\_DL2D (in) | command |
| **7-9** | LBUSY\_IN | LDA\_DD2L (out) | BUSY |
| **10-12** | LSPAREIN | LDA\_SPD2L (out) | Ramfull |
| **15-16** | LFTRIGOUT | LDA\_SPL2D (in) | External trigger |
| **2-5-8-11-17** | ground | ground | ground |
| **13-14-18-19** | Connected through 0 ohm R | 3.3 V | NC |

# Command list (from PC to CCC through RS232 link)

|  |  |  |
| --- | --- | --- |
| Name | Function | Encoding |
| DIF reset |  | x0 |
| BCID reset |  | x1 |
| Start acquisition |  | x2 |
| Ramfull ext |  | x3 |
| Trigger ext |  | x4 |
| Stop acquisition |  | x5 |
| Digital readout |  | x6 |
| Analog readout |  | x7 |
| Clear Memory (DIRAC) |  | x8 |
|  |  |  |
|  |  | X15 |

# Serial protocol for commands between CCC and DIF

HEADER

COMMAND

CHECK SUM

HEADER (4 bits): to be defined

COMMAND ( 4 bits) : command (among 16 max)

Check sum (4 bits) : header xor command (xor or something else)

# Commands between PC and CCC through RS232

To be defined (see first what is already existing).