1 Introduction

The design [1] for a calorimeter for future ILC poses challenges to the data acquisition system (DAQ) mainly due to the large number of channels to be read out. A generic scenario for the DAQ system is as follows. Mechanically, the calorimeter will consist of 6000 slabs, of length 1.5 metres, each containing about 4000 silicon diode pads of 1×1 cm^2, giving a total of 24 million pads. At the very front end (VFE), ASIC chips will be mounted on the silicon pads. The ASICs will perform pre-amplification and shaping and should also digitise the data and may even apply a threshold suppression. The current design [2] of such chips will each contain 32 channels, although this may be higher in the final calorimeter. The data will be digitised in the ASIC and the data transferred to the front-end (FE) electronics which are placed in the detector at the end of the slab. It is expected that a zero suppression will be done at the FE in the FPGAs to significantly reduce the rate. The data will then be transferred off the detector, probably via a switch, to a receiver which would be PCI cards in a PC farm.

This proposal highlights areas of R&D where bottlenecks may arise in such a DAQ system. Alternative designs of a DAQ system which could affect the layout of the final detector are also considered. The proposal is split into three sub-workpackages, each of which has a few distinct tasks. These workpackages investigate the different stages of the DAQ system: the connection from the VFE to the FE; the connection from the on to off detector; and the off-detector receiver.

This programme will allow us to continue aiding development of new technologies by providing the data acquistion system. We will also write a chapter in the future technical design report on the data acquisition system for a calorimeter. This will place us in lead position to build the DAQ system for future large-scale prototype calorimeters and the final system.

If we assume the parameters of the TESLA design for data taking at 800 GeV, the following parameters have to be considered. There will be a 4886 bunch crossings every 176 ns in a bunch train, giving a bunch train length of about 860 μs. The bunch train period is 250 ms, giving a duty factor between trains of about 0.35%. In a shower, up to 100 particles/mm^2 can be expected, which in a $1{\times}1$ cm^2 pad equates to 10000 minimum ionising particle deposits. The ADC therefore needs a dynamic range of 14 bits. Assuming that 2 bytes per pad per sample, then the raw data per bunch train is $24 \cdot 10^6 \times 4886 \times 2 = 250$ GB which equates to 0.3-2.5 MBytes for each ASIC depending on whether they process between 32 and 256 channels. The data appears within a bunch train length of 860 μs giving a rate out of the ASIC of 0.4-3 GBytes/s, which we take to be 1 GB/s from now on. Details of rates after the VFE depend on the assumptions and system layout and will be discussed for each individual case where necessary.

2 DAQ1: Connection from the VFE to the FE

If threshold suppression can be done in an ASIC, the rates to the FE would be reduced by two orders of magnitude. This would simplify the data transfer process. Current designs do not plan this and may not even be desirable or possible, so we should assume the threshold suppression will be done elsewhere and 1GB/s has to be transferred. Whether an electrical or optical connection would be needed has to be investigated. Although chip-to-chip fibres are not yet standard technology, this is an active area of industrial research [3].

2.1 DAQ1.1: Readout for calorimeter prototypes

A new VFE ASIC chip is currently being designed in Orsay, France. In the next 1-2 years, they expect to have a version 0 of such a chip with 32 channels and an ADC incorporated. We propose to build a circuit board to hold 16 chips, thereby reading out about 500 channels. The PCB will be designed and layed out at Imperial College where they will also write the required firmware with the appointment of a new Research Associate. Imperial College, in collaboration with the French groups, will then perform tests of reading out all chips. The PCB will be connected to a development board in a PC. This UK activity is obviously closely coupled to the work of the French design team so is anticipated to be concentrated towards the end of the second financial year. The same set-up will be used to read-out the MAPS system as detailed in Section **??**, thereby consolidating costs and effort.

For the final calorimeter, the DAQ should ideally be the same for the ECAL and HCAL, but CALICE-UK has so far concentrated on only the ECAL. Our proposals for R&D contained in this document are generic such that both calorimeter sections should be able to converge to use the DAQ system we design. Although it is unrealistic for us to provide the hardware electronics for the HCAL beam tests in 2005-7, we will set up discussions to advise on our design and methods. Therefore, we will collaborate with groups who are building the HCAL prototypes such that we can direct the DAQ system to be a common system in the future. This will be an effective paper study between UCL and the HCAL groups with the only costs being occasional travel to collaborating institutes and test-beams.

2.2 DAQ1.2: Study of data paths over 1.5 m slab

The construction of a 1.5 metre long fully operational calorimeter prototype is unlikely on timescales of the next few years. However, issues of how the data would be transported from the VFE to FE have to be considered and can be done already without a real prototype. Transporting about 1GB/s of data over 1.5 metres is a challenge. One could think of doing it conventionally using copper but here the effects of noise and interference would have to be considered. There is also the possibility of doing it using optical fibres although here there are also design considerations. The size of connectors would have to be investigated as the space at the VFE is of the order of mm. This would also involve understanding the power needed to transmit light out. This work also ties in closely with the mechanical and thermal aspects of the design as discussed in Section **??**.

In preparation for a real prototype, a test system will be built with a 1.5 metre PCB containing FPGAs linked optically or electronically. The data transfer would then be considered as a function of the number of VFEs, whether zero suppression is done in the VFEs and whether data is buffered during the bunch train. The bandwidth and cross-talk of the data transfer will be simulated using CAD tools. The clock and control distribution from the front-end to the VFE chips will be investigated as to whether one transmission line per chip is needed or multi-drop is possible. The resources required would initially be two multilayer 500 mm PCBs for initial tests and investigations before moving onto three 1600 mm PCBs for final tests. Hardware for bit error rate testing could be re-used from the ATLAS design. CAD tools would also be required particularly in the initial phase. Cambridge and Manchester Universities will work together on this project, sharing costs and effort. This would be a project which would run over the three years of the proposal.

3 DAQ2: Connection from on to off detector

In the standard detector configuration, communication from the VFE will be via the electronics at the FE to an off-detector receiver. As threshold suppression would be done at the FE, the rates would be significantly reduced from that at the VFE. Assuming that the rate is reduced to 1% of the original data volume of 250 GBytes and each sample above threshold needs channel and timing label, the total data volume to be read out from the calorimeter is about 5 GBytes or about 1 MBytes per slab. This data has to be read out within a bunch train period of 250 ms, giving a rate of 5 MBytes/s. This is significantly slower than the 1 GBytes/s from the VFE.

In the following, we consider two scenarios: the first is the standard detector configuration and the other is where the FE is removed and the communication is directly from the VFE to the off-detector. The off-detector receiver, as described later is assumed to be PCI cards housed in PCs. As PCs are not 100% reliable, a switch will be necessary to send data efficiently to working PCs. The first scenario would require less high-speed equipment off detector whereas the latter would require many optical fibres with dedicated optical switching. The second scenario would however remove material from inside the detector which would ease construction and have a potentially advantageous impact on event reconstruction and, hence, physics measurements. This would also reduce the number of processing components within the detector which would be inaccessible for long periods of time.

BOTH DAQ2.1 and 2.2 will need the PCI cards discussed later, so check timescales.

3.1 DAQ2.1: Connection from FE to off-detector receiver via network switch

Richard to provide some ideas.

Set-up test bed for more conventional scenario where the FE communicates to the off-detector receiver.

This sub-workpackage is to be led by Manchester with input from UCL who will lead the alternative system. UCL will provide the FPGA to fibre communication interface, related to the clock and control package discussed later.

3.2 DAQ2.2: Connection from VFE to off-detector receiver via optical switch

We propose to setup a test system to validate that fibres can transport the necessary data rates from the VFE to the off-detector receiver and an optical ("layer-1") switch can re-route data with high efficiency. This would contain a bundle of fibres coming into a switch from an effective VFE. A bundle would the come out of the switch to the off-detector receiver. The off-detector receiver, described in more detail in the next section, would be a set of PCI cards housed in PCs. The same PCI card would be used in our test system to emulate the VFE chip. The optical switch efficiency would then be tested when PCs fail and the data has to be swapped to another PC. Also if a PC contains a large amount of data which could be of interest and takes up a large amount of processing time, a busy signal would be sent to the optical switch which would again reroute new incoming data. As it is assumed to do some clustering on the PCI cards, overlaps in geometrical areas of the calorimeter will be necessary. Therefore, the optical switch would also be able to send the same data to different PCs.

The number of fibres required to read-out the 24 million channels would vary between 750 000 to about 90 000 depending on whether the ASIC handles 32 or 256 channels. If we assume that the diameter of a fibre is 150 μm, or with cladding 250 μm then if half of the circumference of 12 m had fibres running along it, the bundle would be up to 1 cm in depth, but as little as 1 mm, depending on the number of ASICs and hence fibres. This would leave ample room for other cables and power supplies. This concept would revolutionise the whole calorimeter design so needs to be considered now when changes in its general structure could be considered.

The test system would consist of (to change):

- optical switch £25 000 for 144 ports (January 2003)
- optical fibres £?????
- connectors, miscellaneous, etc. £?????

This sub-workpackage is to be led by UCL with input from Manchester who will lead the alternative system.

3.3 DAQ2.3: Failsafe FPGA

In a scenario requiring an FPGA on-detector at the front end, it is imperative that the device can be re-configured remotely. This stems both from the number FPGAs, but also the relative inaccessibility of the devices. To facilitate this some sort of non-volatile memory that boots the device into a communicative state, or an external control system that provides an interface between the unconfigured FPGA and the outside world is required.

Using devices with non-volatile memories built-in may have advantages here, but increased cost and limited re-programming cycles make these less attractive. Questions surrounding the reliability in the detector environment of these memories over the lifetime of an experiment also need to be addressed. In contrast modern SRAM based FPGAs boast that they can re-configured infinitely and can therefore be 'refreshed' at regular intervals to ensure their configuration is not corrupted. The option of running with different firmware for different types of run is also attractive.

Reducing the number of components on the front-end-module would be advantageous from a cost, reliability and dead material point of view. To this end we propose a task of researching a means of connecting a commercial network receiver package to an FPGA with the absolute minimum of components, so as to reliably reset and configure the device remotely. We will also consider a literature survey of various FPGAs response to radiation and rates of single event upsets and how to circumvent them.

The test system will be simple and require a PC with a network card and a development board with cables and connectors. This work is closely connected to the clock and control in the next section and will be carried out at UCL.

3.4 DAQ2.4: Transport of clock and control and configuration data

To ensure front-end detector electronics captures data from actual collisions all components in a detector system need to be synchronised to a bunch-crossing clock. Although a 'trigger-less' system is envisaged it is still useful to consider a signal that moderates read-out, such as 'bunch-train-start' signal.

One of the systems in this proposal make use of standard network protocols to tag data at the front-end such that a commercial network can deliver it to a waiting event-builder PC. To co-ordinate this requires that busy information from the event-builder system is used to derive available data destinations that needs to be sent to the front-end. This can be called a trigger ID at some level. Although the need to build a large scale system is still some way off, the means of interfacing these time-dependent signals into the more asynchronous commercial network arena is not understood. The aim of this task is to investigate means of distributing clock and control signals using commercial networking equipment and components, as opposed to a more traditional bespoke system.

This couples well with the previous task of investigating the FPGA failsafe in that it attempts to minimise components and connections on the front-end-module. In many ways this will be an investigation to verify that a single clock, control and configuration system can be constructed using a commercial hardware for both receiver and transmitter hardware. Although it is envisaged that fibre optic will be the dominant communications technology in a final design, lower speed copper based systems are sufficiently similar to allow the first stage of development to use this technology.

The test system will build on the previous FPGA failsafe task and use much of the same equipment. Additional network cards, a fanout board and switch will be required. As stated before, this work will be undertaken at UCL, with a new Research Associate contributing along with Academic and Engineering staff.

4 DAQ3: Off-detector receiver

An ideal system would have all data from the detector sent directly to one PC where full event reconstruction is performed. Given the over 20 million channels in the calorimeter, this seems unfeasible. However, it is desirable to get as much of the calorimeter into one processor as possible. This would allow for local clustering which could be used as a seed to full event reconstruction offline. We propose a system which consists of PCI cards mounted in PCs which receive the data and perform local clustering. The fundamental questions to be answered is how much of the calorimeter can be received into one PC and how much needs to be received to make local clustering effective. The impact this has on full event reconstruction and on simulated physics needs to be evaluated.

4.1 DAQ3.1: Prototype off-detector receiver

The off-detector receiver will consist of a set of PCI cards in PCs. The PCI cards will be part of both of the network systems, being configurable to act as a receiver for either. In a test system, they would also act as the VFE or FE sending data off detector. Recent developments in PCI cards have led to high bandwidth which is scalable due to future increases in the number of lanes using PCI Express technology. We will use cards based on this technology using a PCI Express bus. We will design and build our own PCI card to maximise flexibility for the tests we want to perform. In conjunction with the network workpackages discussed previously, tests will be made to see how efficiently data is transferred if a PC is unreachable or busy. Although it is hard to predict what technology will be around for the final system, gaining experience of cutting-edge technologies now, such as PCI Express, will prove valuable now for estimates of how much data can be received by one computer. So, whilst not trying to absolutely maximise the amount of data which can be transferred into a PC in the test system, the model should be scalable.

The final system would consist of 4 PCs each with a PCI card in them and the possibility to move PCI cards between PCs so as to maximise the data rate to one computer. To act as the VFE or FE sending the data, 4 further PCI cards would be required housed in two PCs. Assuming 4 prototypes at £ 2500 per board, £ 1500 per board for the final eight and six PCs each costing £ 1200, the total price comes to about £ 29 200. The design and build of the PCI card would be undertaken by Cambridge, UCL (with the new RA contributing) and RHUL in conjunction with Manchester and UCL's work on networking. The PCI cards and PCs would be shared by Manchester and UCL for the network system tests.

4.2 DAQ3.2: Local clustering on PCI cards and simulation

With sufficient data transported to one computer local clustering and removal of isolated hits can be performed before full event reconstruction is done offline. This would involved firmware programming of the FPGA on the PCI card, its simulation and subsequent effect on full reconstruction and performance in a physics analysis. This would be undertaken by Cambridge and UCL (lead by the new RA) and would have a large overlap and close collaboration with their interests in the simulation workpackage (see Section **??**).

References

[1] TESLA: The superconducting Electron-Positron Linear Collider with an integrated X-Ray Laser Laboratory. Technical Design Report. DESY 2001-011. March 2001.

[2] C. De La Taille, private communication

[3] http://www.intel.com/update/contents/it04041.htm

Milestones

DAQ1.1: Readout for current calorimeter designs

1. Design of PCB and development board for reading out 16 chips.
2. Layout of boards.
3. Write firmware.
4. Readout prototype chip.
5. Readout 16 chips.
6. Collaboration with HCAL groups to form common system for DAQ.

DAQ1.2: Study of data paths over 1.5 m slab

1. Choice of electrical standard.
2. Clock and control distribution from FE to VFEs.
3. Build test boards to check validity for 1.5 m paths.
4. Data transmission as a function of number of VFEs.
5. Data transmission as a function of whether zero suppression is done on VFE.
6. Data transmission as a function of whether buffering done during bunch train.
7. Simulation of bandwidth and cross-talk.
8. Estimate of electrical pick up at pads.

DAQ2.1: Connection from FE to off-detector receiver via network switch

1. blah

DAQ2.2: Connection from VFE to off-detector receiver via optical switch

1. blah

DAQ2.3: Failsafe FPGA

1. Become familiar with a modern FPGA reset/configuration implementation (e.g. Xilinx Virtex-4).
2. Investigation of FPGA radiation tolerance and rates of single event upsets.
3. Build a test system using signals generated from a digital signal source (e.g. another FPGA) to test reset and configuration protocols.

4. Explore capabilites of commercial networking devices.
5. Build a test system to interface a commercial networking devices to the signal required in 2) above.
6. Upgrade the system to use modern very-high speed network links (10 Gbit Ethernet).
7. Examine integration of such a system into a commercial network based DAQ system.

DAQ2.4: Transport of clock and control and configuration data

1. Evaluate the clocking requirements for a front-end-module in the front-end.
2. Investigate means of regenerating a clock from commercial network links. Build test module to do this with standard (100 Mbit) components.
3. Investigate means of extracting accurate trigger/spill timing signals.
4. Explore using commercial network equipment to distribute triggers. Build a small network, driven from a PC for testing.
5. Examine problems associated with scaling to a 10000 link system.
6. Look at cost effective ways of distributing time sensitive signals using a more proprietary system, still making use of commercial transmitters and receivers. Would involve building a small test board.
7. Make use of a proprietary (the CALICE PCI card) to generate these signals in a point-to-point or low-level fanout configuration.

DAQ3.1: Prototype off-detector receiver

1. Investigation of latest PCI technology.
2. Design and build PCI card probably based on PCI Express.
3. Test PCI card.
4. Fabricate batch of PCI cards and setup test system for prototype off-detector receiver.
5. Efficiency of data transfer when PCs unreachable or busy
6. Amount of data, i.e. how much of calorimeter, can be transported to a PC.

DAQ3.2: Local clustering on PCI cards and simulation

1. Program FPGAs to perform local clustering and do hit removal.
2. Simulate in Monte Carlo.
3. Effect of local clustering on final event reconstruction.

4. Effect of local clustering on physics process.

5. How much of calorimeter needs to be contained in a PC for clustering to be effective.

GANNT chart

DAQ Workpackage	FY 05/06				FY 06/07				FY 07/08			
	1	2	3	4	1	2	3	4	1	2	3	4
DAQ1.1: Readout for VFE prototype chip												
1. Design of PCB and Dev. board							=	=				
2. Layout of boards								=	=			
3. Write Firmware								=	=			
4. Readout prototype chip									=			
5. Readout 16 chips									=	=		
6. Collaboration with HCAL groups	=	=	=	=	=	=	=	=	=	=	=	=
DAQ1.2: Study data paths of 1.5 m slab												
1. Choice of electrical standard	=	=	=	=								
2. Clock and control from FE to VFEs			=	=	=	=						
3. Build test boards for 1.5 m paths			=	=	=	=			=	=	=	=
4. Data transmission as a function of number of VFEs					=	=			=	=		
5. Data transmission with zero suppression on VFE						=	=			=	=	
6. Data transmission with buffering during bunch train							=	=			=	=
7. Simulation of bandwidth and cross-talk					=	=	=	=	=	=	=	=
8. Estimate of electrical pick up at pads									=	=	=	=
DAQ2.1: Connection from FE to off detector												
DAQ2.2: Connection from VFE to off detector												
DAQ2.3: Failsafe FPGA												
1. Familiarisation with FPGA configuration	=	=										
2. FPGA radiation tolerance and SEU rates	=	=	=	=								
3. Test reset and configuration protocols		=	=									
4. Explore commercial networking			=	=								
5. Test system linking signals and network				=	=							
6. Upgrade to high-speed networks					=	=						
7. Integration into DAQ system						=	=					
							=	=				
DAQ2.4: Clock and control and configuration data												
1. Evaluate the clocking requirements					=	=						
2. Regeneration of clock from commercial network links						=	=					
3. Extracting trigger /spill timing signals							=	=				
4. Build small network for testing								=	=			
5. Problems scaling to a 10000 link system									=	=		
6. Proprietary systems on a small test board										=	=	
7. Test of system											=	=
DAQ3.1: Prototype off-detector receiver												
1. Investigation of latest PCI technology	=	=										
2. Design and build PCI card		=	=	=								
3. Test PCI card				=	=							
4. Fabricate batch of PCI cards and setup test system					=	=	=					
5. Efficiency of data transfer when PCs unreachable or busy							=	=	=	=		
6. How much of calorimeter can be transported to a PC										=	=	=
DAQ3.2: Local clustering on PCI cards												
1. Program FPGAs	=	=	=	=								
2. Simulate in Monte Carlo				=	=	=	=	=				
3. Effect on final event reconstruction							=	=	=	=		
4. Effect on physics process									=	=	=	=
5. How much of calorimeter needed											=	=

Deliverables

- Demonstration of functionality of new ASIC chips.
- Properties of data flow along 1.5 metre board.
- Most reliable data transportation and routing method off the detector.
- Need (or not) for front-end electronics.
- Method for rebooting and reconfiguring inaccessible FPGAs on the front-end electronics.
- Method of synchronisation of commercial standard components to an accelerator clock.
- Scalable model of off-detector receiver to answer how much data can be sent to one PC.
- Amount of data needed in one PC for local clustering to be effective.
- Write chapter on data acquisition for calorimeter for technical design report.

Effort

Name	Position	Institute	Funding	2005/6	2006/7	2007/8
M. Goodrick	Engineer	Cambridge	PPARC (RG)	0.2	0.5	0.6
ELECTRONICS	Technician	Cambridge	PPARC (RG)	0.2	0.5	1.0
MECHANICAL	Technician	Cambridge	PPARC (RG)	0.0	0.15	0.15
P. Dauncey	Academic	Imperial	HEFCE	0.0	0.2	0.0
O. Zorba	Engineer	Imperial	PPARC (RG)	0.0	0.4	0.0
ELECTRONICS	Engineer	Imperial	PPARC (RG)	0.0	0.3	0.0
New RA-1	RA	Imperial	PPARC (new)	0.0	0.4	0.0
R. Barlow	Academic	Manchester	HEFCE	?	?	?
R. Hughes-Jones	Engineer	Manchester	PPARC (RG)	?	?	?
S. Kolya	Engineer	Manchester	PPARC (RG)	?	?	?
M. Green	Academic	RHUL	HEFCE	?	?	?
OTHERS?	?	RHUL	?	?	?	?
M. Lancaster	Academic	UCL	HEFCE	0.2	0.2	0.2
M. Postranecky	Engineer	UCL	PPARC (RG)	0.3	0.3	0.5
M. Warren	Engineer	UCL	PPARC (RG)	0.3	0.5	0.5
M. Wing	Academic	UCL	HEFCE	0.3	0.3	0.3
New RA-2	RA	UCL	PPARC (new)	0.6	0.6	0.6
Total FTE				2.1	4.35	3.85
Total new				0.6	1.0	0.6

Table 1: Table of FTE effort from all Universities

Costs per task

	2005/6	2006/7	2007/8
DAQ1.1: Hardware	£0 k	£9 k	£0 k
DAQ1.2: Hardware+CAD	£10 k	£12.5 k	£12.5 k
DAQ2.1: Hardware	£? k	£? k	£? k
DAQ2.2: Hardware	£? k	£? k	£? k
DAQ2.3: Hardware	£0 k	£5 k	£0 k
DAQ2.4: Hardware	£0 k	£0 k	£6 k
DAQ3.1: Hardware	£5 k	£17 k	£7.2 k
DAQ3.2: Hardware	£0 k	£0 k	£0 k
DAQ: Total equipment	£15 k	£43.5 k	£25.7 k
DAQ: Travel	£10 k	£14 k	£16 k

Table 2: DAQ: Total costs