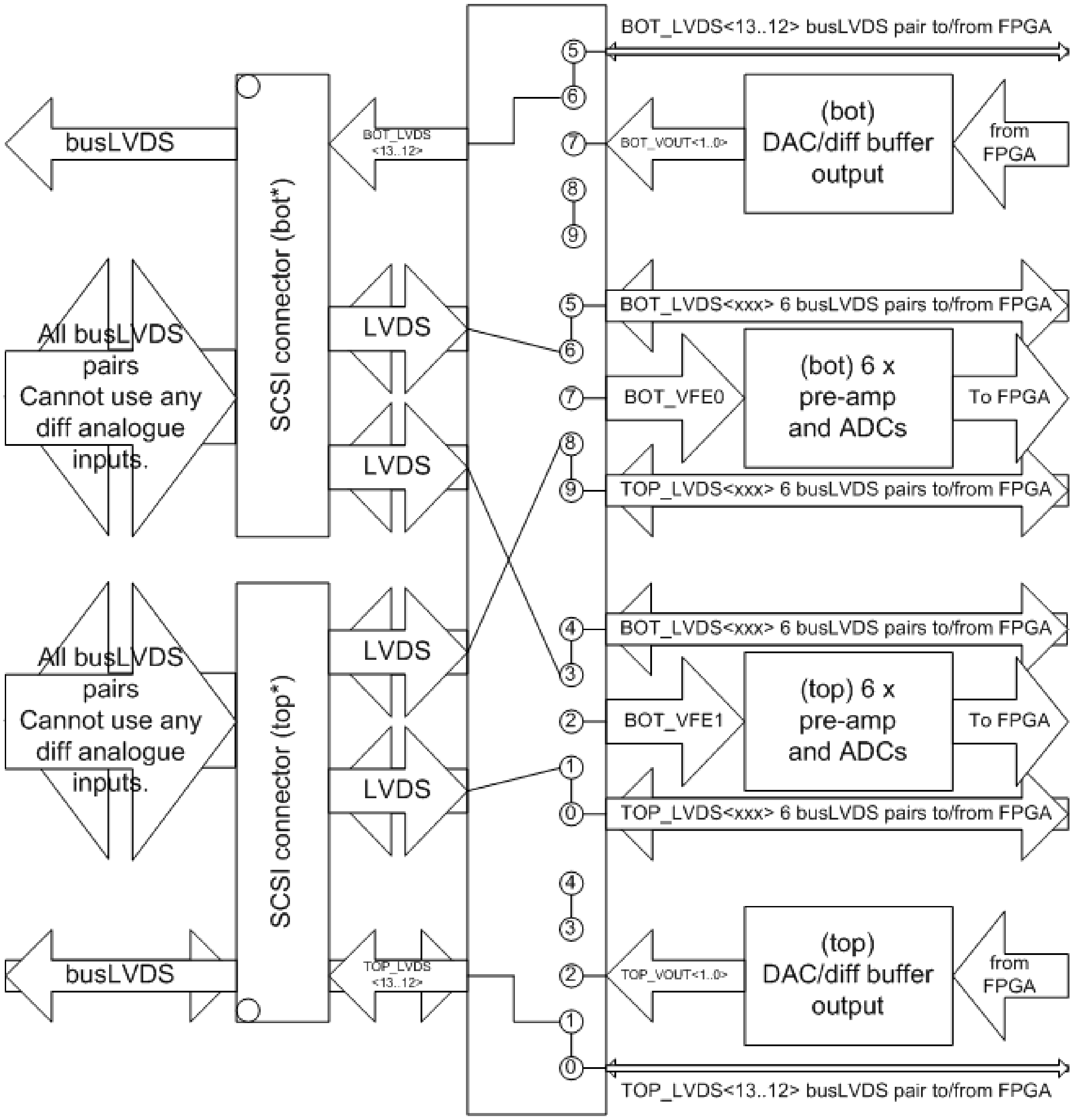
Standard dual busLVDS configuration (HCAL)

link columns, 9-8, 6-5, 4-3, 1-0.



Two full busLVDS cable (HCAL type)

Both SCSI connector may be used for arbitrary busLVDS I/O including clock generation.
ADCs and DACs are completely bypassed and should be powered down.
All busLVDS connections straight from the SCSI connectors to the FPGA are not shown.