

A concept for power cycling the electronics of CALICE-AHCAL with the train structure of ILC

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Abstract

Calorimeters, like CALICE-AHCAL, aiming for particle flow measurement need high granularity readout in all three dimensions. This requires electronics to be integrated into the detector volume with typically 1000 channels/square-meter. To keep the mechanics simple and homogeneous, heat generated should be conducted away by the steel of the absorber layers only. The resulting heat production limit of $40\,\mu\text{W}$ per channel can be achieved by switching the current sources in the readout ASIC off for 99% of the time when no bunches are delivered by the ILC accelerator. By adequately designing printed circuit boards and using discrete capacitors the effect of high frequency components of the switched currents can be minimized. At the end of each readout layer space is available to stabilize the voltage, to place more and larger capacitors, and to install circuits for filtering. The readout electronics is connected by long cables to supply instruments located in the electronics rooms of the experiment. Using charge storage at the layers and galvanic isolation of the supply instruments results in cable currents and voltages which vary only with low frequencies, which minimizes disturbance to other subdetectors.

The proposed solutions and their impact are described for all stages of the readout chain, from the detectors in the active volume to the external supply units. Results of simulation and first measurements demonstrating the reachable parameters for the system are shown.

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1. Introduction

The next generation of TeV electron-positron colliders are planned to be linear accelerators. The ILC[1] proposes the use of superconducting RF-cavities operating with an accelerating RF flat top of 1 ms followed by 199 ms during which the accelerating RF-field is switched off allowing the superconducting RF-cavities to cool down. Correspondingly collisions at detectors appear with the same time structure and signals have to be recorded for only 0.5 % of the time.

The physics to be investigated requires that the detectors used have extremely good resolutions and the ILD-collaboration[2] requires a calorimeter with a jet energy resolution of $30\%/\sqrt{E_{jet}}$. The calorimeter being developed by the CALICE-collaboration, the analogue-hadron-calorimeter AHCAL[3, 4], described in detail in section 2, uses the particle algorithm[5] to achieve this. This requires high granularity readout in all three dimensions and 60 000 channels are used per cubic-meter, resulting in 4 million channels in the barrel region alone. However, high channel densities lead quickly to large heat loads which have to

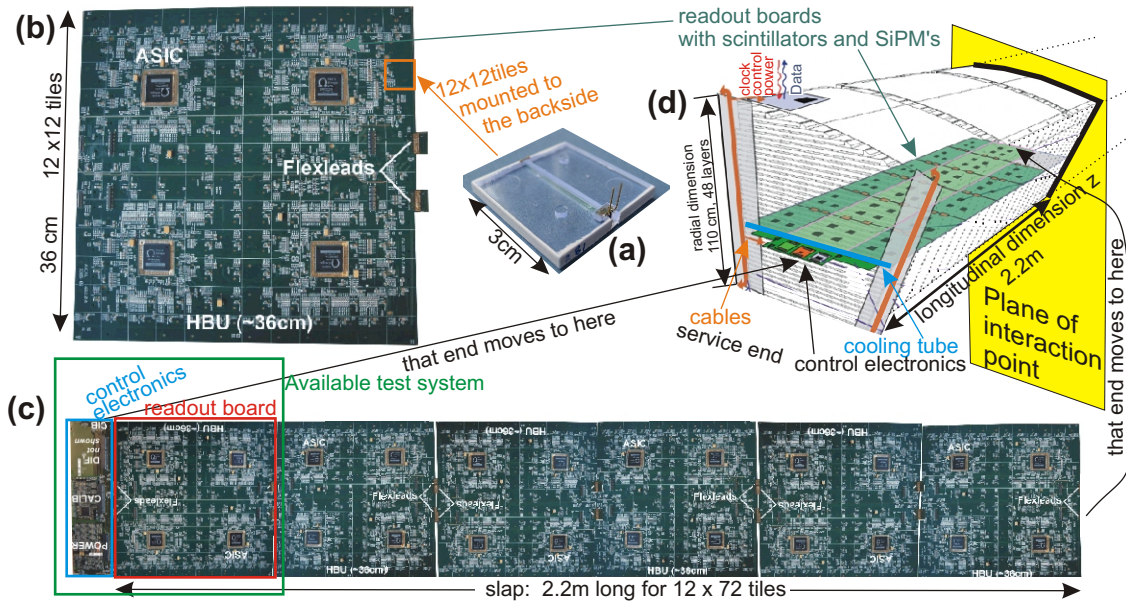


Fig. 1. Construction of the AHCAL with the main elements of the detection system and electronics: (a) Scintillator tile with a SiPM, (b) 12x12 tiles mounted to a single readout board, (c) a complete slap for a detection gap composed of 6 readout boards and a control part, at the moment only the control electronics with one readout board is available for tests and (d) the mechanical structure of a half octant for the sampling calorimeter with three parallel slaps installed into one detection gap

be dissipated. By operating the front end electronics with the same time structure as the accelerator and implementing power on and standby modes the power budget is reduced by two orders of magnitude and the limit per channel of $40 \mu\text{W}/\text{channel}$ can be reached, but requires the electronics and their powering system to cope with non stable current consumption. Initial ideas and measurements of how this can be achieved are described in sections 3-6.

2. The analogue hadron calorimeter (AHCAL) for ILD and the need of power cycling

The analog hadron calorimeter (figure 1) is designed to measure the energy of hadronic particles entering the calorimeter by sampling the subsequent shower evolution and using amplitude and shape information to derive the energy. Additionally the sample information is used to identify components with electromagnetic, hadronic or muon-like character within the hadronic shower. For the barrel part of the hadron calorimeter this will be realized by a repeating longitudinal sampling sandwich structure of 12 mm planar stainless steel plates surrounding the beam axis as an octagon, 3 mm thick scintillators and 2.5 mm space for a layer of electronics. Scintillator layers are segmented into $3 \times 3 \text{ cm}^2$ large tiles and light is collected by a wavelength shifting fiber and guided to a SiPM[6, 7], the output of which is connected via a printed circuit readout board to an ASIC[8]. Each $36 \times 36 \text{ cm}^2$ sized readout board handles 12×12 tiles. Flex leads are used to build up 2.2 m long structures, called slaps, by daisy chaining 6 readout boards and a control board at the service connection end, where maintenance is possible and where cooling will stabilize the stainless steel structure. By mechanical design the heat of the control board is kept away from the sensitive SiPM's. The SiPM signal stability required is achieved by regulating the temperature to within 0.5 K. By installing three slaps side-by-side, a detection layer with 2600 channels will be built up for each half-leg of a calorimeter octant.

To keep the calorimeter design homogeneous and simple no cooling is foreseen within the readout or stainless steel absorber layers and heat generated by the active components is transported, by the stainless steel structure, to the service end. The longitudinally distributed electronics and SiPMs components within each layer lead to a temperature gradient within the stainless steel structure. The temperature is lowest at

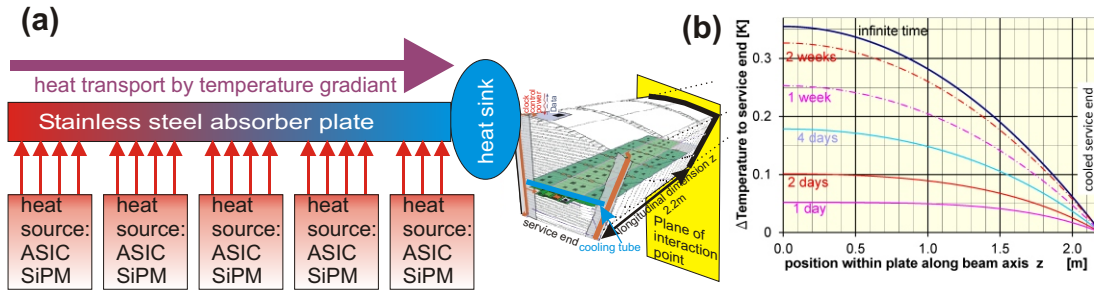


Fig. 2. Geometric profile of the temperature within the AHCAL: (a) Geometrical approach for the calculation and (b) the calculated temperature profile and its time dependence after start of the heating with $40\mu\text{W}/\text{channel}$ (9cm^2).

the service end and increases in the direction of the symmetry plane at $z=0\text{cm}$ where the interaction point is located. Numerical calculations performed[9] using a simplified geometry and experience gained with the HES detector at the ZEUS experiment[10] indicate that no significant heat flow exists between sandwich structures via the air gaps, which are too large to conduct the heat but too small for building up streaming air. For AHCAL that means that in the radial direction around the beam pipe no heat is transported and the barrel octagon can be approximated as a cylinder with heat flow along the z -axis parallel to the beam pipe. This observation allows the heat flow, Q , to be calculated using a differential equation with time and z dependence as described in [9]. The numerically calculated temperature variation along the steel structure after various heating periods is shown in figure 2 assuming the plate is heated homogeneous with a mean value of $40\mu\text{W}/(3\text{cm})^2$, that the temperature is stabilized by cooling at the service end, and that no heat is transported towards the symmetry plane ($z=0\text{cm}$). For long periods the variation remains below 0.5K demonstrating the need to keep the power consumption low and the use of the factor 100 offered by power cycling, even if the later reduces the measurement time for non-collision events and requires additional design effort within the electronics and its power system.

The behavior of the AHCAL power system is determined from contributions of all electronics blocks, see figure 3, whether active (ASIC, SiPM, external power supply, etc.) or passive (layer readout boards, cables, etc.). In the following four sections the decisions made regarding block design and the impact of the decisions on system performance are described.

3. ASIC

The AHCAL ASIC, a SPIROC[8], performs all SiPM signal processing operations: it amplifies the SiPM output signal, stores the results per collision in a self managed capacitor pipeline, digitizes the stored current using a slow ADC, stores the result in RAM, and manages and sends its digitized data to the control electronics of the service end using a highly multiplexed gather of all data in the layer. All operations are

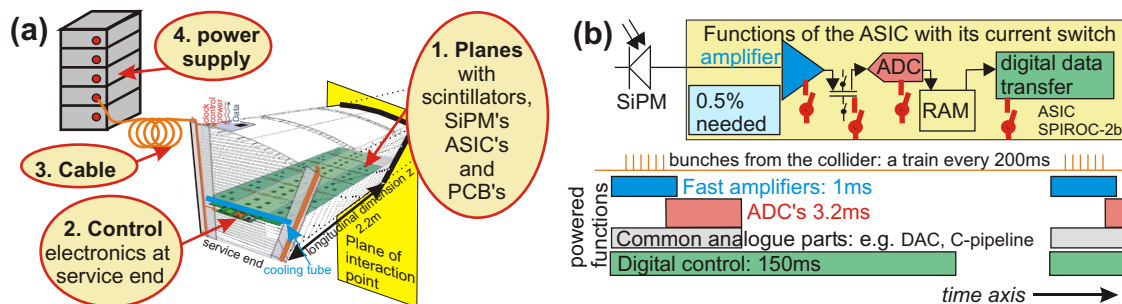


Fig. 3. Power system for a cycled current consumer: (a) Involved components and (b) current cycle of the tasks of the ASIC.

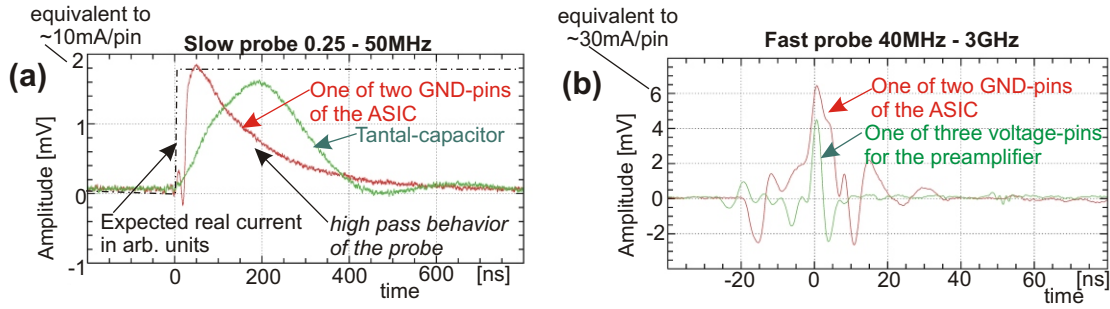


Fig. 4. Current in the Pins of the ASIC: The current are measured with (a) a slow probe for 0.25-50MHz and (b) a fast probe for 40MHz-3GHz at a single of two parallel connected pins of the SPIROC-ASIC. In (a) a curve is included, which shows the current provided by the Tantal capacitor of the charge storage alone. In (b) is indicated that the frequency spectrum for the preamplifier and the total current of the SPIROC-ASIC including the ADC and the digital part differs.

performed during train delivery by the ASIC except digitization and data transfer to the service end which are performed during the consecutive intertrain gap after acquisition.

Concentrating functionality in the ASIC naturally leads to its choice as an actor driving power saving. Requested by a few low power control lines the ASIC will switch off its current sources for the different functions: the power hungry fast input amplifiers, the analogue capacitive storage cells, the ADCs, the RAM, and the digital electronics for management and data transfer. The optimized times for the different switch-off tasks are shown in figure 3. Using this concept power hungry circuits, like accurate transfers on long signal lines or fast electronics, are avoided or switched off for most of the time.

The power management described means that the ASIC's current consumption is changing drastically as show in figure 4 by measurements on the pins of the ASIC. The measurements are performed with magnetic coupled probes at single pins of the ASIC. This coupling behaves like a bandpass filter and reduces the current jump at the measured pin due to increased impedance compared to the parallel connected none measured pins. For low frequencies the measurements do not show the real current behavior as indicated by the dash curve in figure 4, but instead a slow fall off which is an artifact of the bandpass. The total switched current per ASIC is expected to be 40 mA adding up to 3 A per layer. This somewhat limited measurement demonstrates that the printed circuit board (PCB) electronics has to deal with a wide frequency band reaching well into the few 100 MHz range and with amplitudes of a few 10 mA/ASIC. For this reason it is recommended to close current loops near to the switching consumer and to provide effective charge storage at adequate distances. This reduces the risk of disturbing conductor guided electromagnetic interferences because the common mode fast changes of the voltages within the power system are limited to small regions and their amplitudes are kept small and the current loops get very small avoiding transformer like couplings.

4. Front end ASIC and SiPM printed circuit board

The PCB to which the scintillator tiles, the ASICs and nearby drivers are mounted, have to be thin to keep the calorimeter compact[11]. Designing it as multilayer board with a pair of nearby power and ground planes, separated by $d_{plane}=50\mu m$ of FR4-material, generates a good capacitor for the high frequency range with a capacitance of $\approx 60pF/cm^2$ (figure 5). Its contribution was simulated with PSPICE and VHDL-AMS[12] by replacing a small area of $A_{cell}=1cm^2$ by a two dimensional delay line and taking the resistivity of $17\mu m$ thick copper layers into account. The capacitance C_{cell} is the capacitance of two parallel plates, while the inductance L_{cell} can be calculated from the transit times of a one dimensional wave:

$$C_{cell} = \epsilon_0 \epsilon_r \frac{A_{cell}}{d_{plane}}, \quad L_{cell} = \frac{1}{c_{light}^2 \epsilon_0} d_{plane}, \quad \epsilon_r(FR4) = 4, \quad c_{light} = 3 \cdot 10^8 m/s, \quad \epsilon_0 = 8.9 \cdot 10^{-12} \frac{As}{Vm} \quad (1)$$

The result of the simulation, curves "PCB-alone" in figure 5, shows that the PCB provides a good capacitive like behavior, upto nearly 100 MHz, and an impedance below 1Ω upto 1 GHz. Due to the granularity of $1cm \approx 70ps$, used in the simulation, results above $1/(10 \times 70ps) = 1.5GHz$, cannot be trusted.

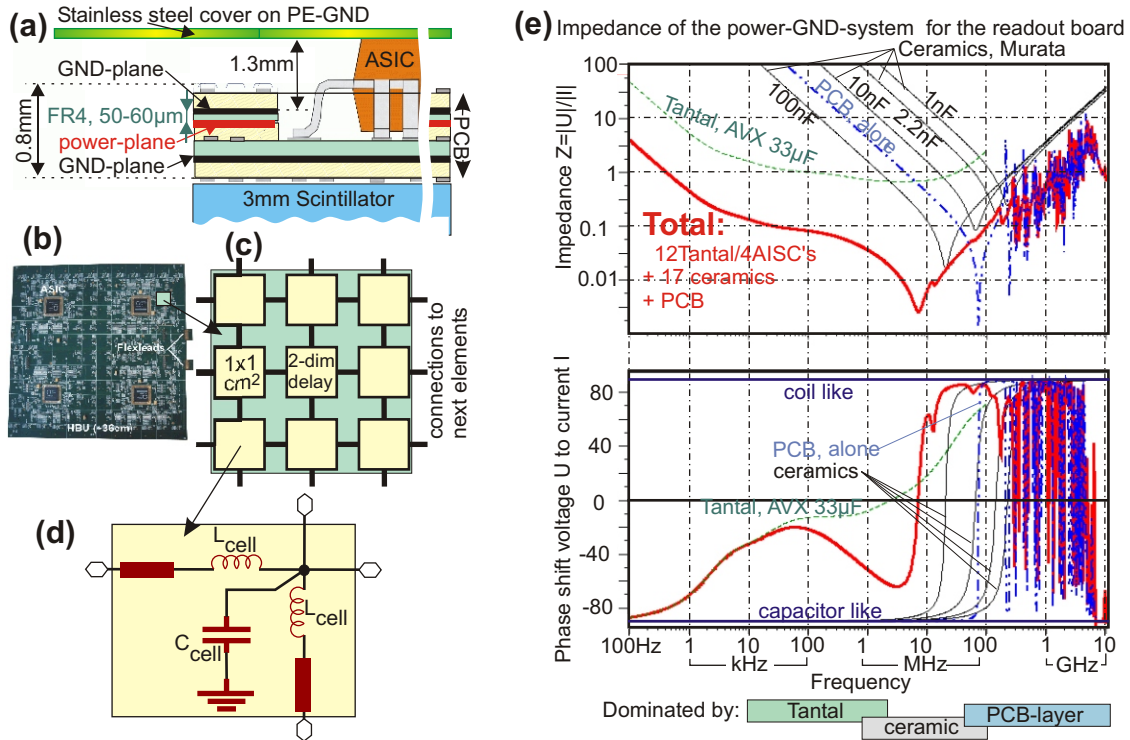


Fig. 5. Impedance for providing the charge by the readout board: (a) layer structure of the PCB, (b) the PCB with the indication of a simulation element, (c) the discrete element structure for simulation, (d) the circuit for a single $1 \times 1 \text{ cm}^2$ element appearing 36×36 per readout board and (e) the result of a simulation of the layer structure and additional capacitors.

For the lower frequencies, up to a few 10 MHz, the charge storage can be provided by ceramic capacitors mounted onto the board to avoid geometrical symmetry and standing waves. Capacitors with X7R material have been chosen because of their broad region changing from capacitor to inductor like behavior. Parallelizing different capacitors generates combined with the layer system of the PCB, a wide frequency range of low impedance ($< 0.1 \Omega$) and phase shifts between currents and voltages, which damps starting oscillations. For the very low frequencies a few Tantal-capacitors are added to the board. These are available with thin housing for capacitances of $33 \mu\text{F}$ and do not increase the total thickness of the electronics layer, whilst improving the impedance for the range up to 1 MHz.

These measures produce a low impedance system (0.1Ω) where resonance damping behavior is reached for frequencies above 10 kHz. At lower frequencies - trains last 0.6 ms - the charge storage needs further support which can be installed further away, e.g. at the service end of the 2.2 m long slap (see section 5), as the reaction time can be larger. For the few 100 MHz range the resonances seen in the simulation are expected to be smeared out by the partial resistance like load of the current consumers, like the ASICs which are not yet included into the study.

5. Service end electronics and charge storage

At the service end more space is available for the control electronics and heat can be cooled away. As illustrated in figure 6 this space can be used to install a capacitor bank, C_2 , which is discharged during the bunch train delivery, and by a regulator which stabilizes the voltage for the front end. Since the reaction time of voltage regulators is limited, it is supported by an external FET transistor and a capacitor at its output (LT1575 with IRL3714). The input capacitor, C_2 , value of 3.4 mF is a compromise with respect to the space required, a few cm^2 , and the additional heat production because it is discharged by 0.6 V during a

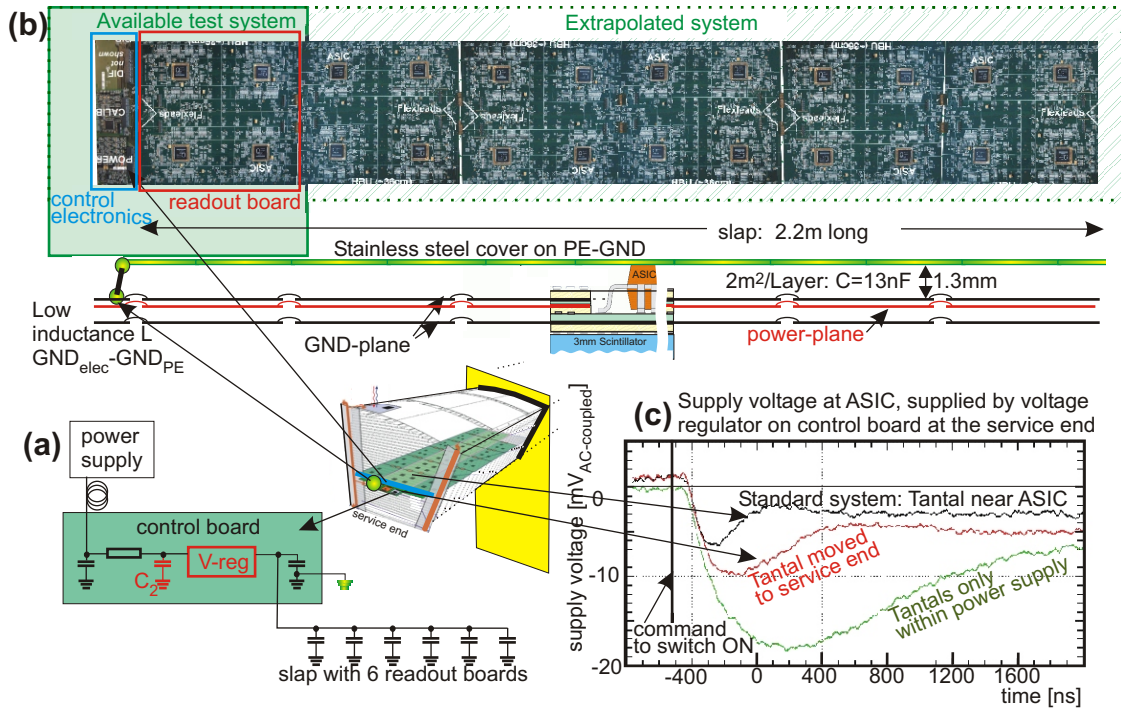


Fig. 6. Concept and behavior of the control electronics at the end of a sampling layer: (a) the concept of charge storage and voltage stabilization, (b) definition of the connection to the environmental and protection ground (PE) and (c) measurements of the stability of the voltage at the ASIC and the effect of Tantal-capacitors and their distance to the ASIC's.

bunch train, requiring an increased supply voltage. With the electronics currently available a reduced setup has been connected, see figure 6, and the voltage stability at the ASIC readout has been measured to be 4 mV. Extrapolation to a full layer taking into account the higher current and the additional resistance of the interconnects suggests that the voltage step will be less than 80 mV. The measurement also shows that the voltage stabilizes within a few $\mu\text{seconds}$, allowing the ASICs to switch the current sources on a very short time before the train starts. Additional trials of repositioning the Tantal capacitors from the front end to the control board or omitting them completely demonstrated that the best performance is reached by having them at the front end.

The voltage drop will appear on the ground and the power plane. As a layer has an area of 2 m^2 and has to be kept thin, a fairly large capacitor is generated from the ground layer and the stainless steel forming the protection earth system (PE) with a 13 nF for a distance of 1.3 mm. It is therefore important to keep the rise and fall times slow. In a setup containing the described PCB, distributed capacitors on the readout boards and a voltage regulator at the service end 150 ns (figure 6) are measured.

Taking the worst case scenario of a voltage change on the GND-side, induces a current of $2\text{ mA}/\text{layer}$ into the local PE. Since the analogue circuitry from the SiPM to the ASIC is noise sensitive and deals with 10^5 to 10^6 electrons only, a local ground connection between electronics ground and PE is needed, but only at one point because the switched currents are large, $2\text{ A}/\text{layer}$, and should not appear in the PE. Since the induced currents are already kept low and slow by the design of the front end PCBs, it should be possible to choose an easy connection point at the service end of the layer and to tolerate the 5 ns travel time to it, see figure 6. To really guide the current back at that connection a low impedance wiring is needed, but can only be verified after full scale prototypes are available.

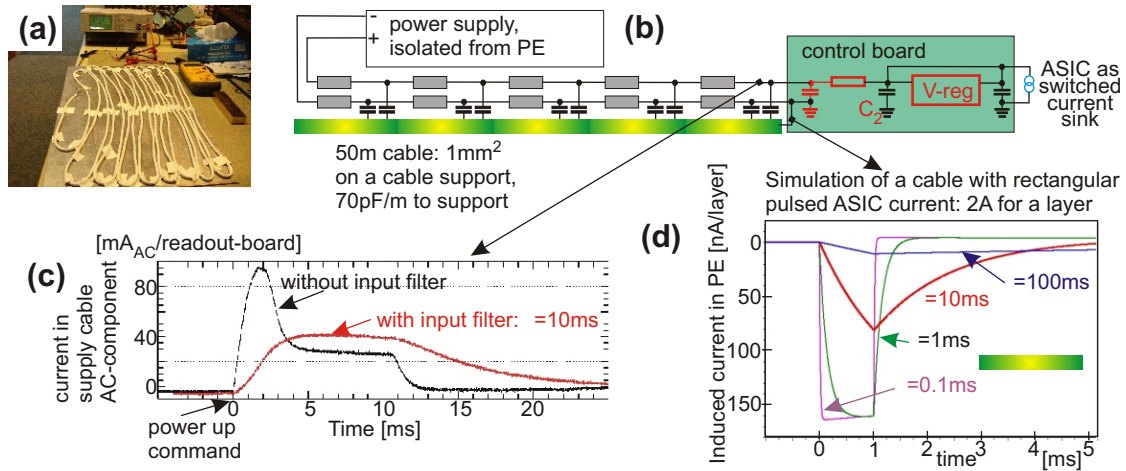


Fig. 7. Effect of the input filter of the control electronics of a layer: (a) Experimental setup to measure the capacitance coupling of a cable to the environmental system, a metal support, (b) the simulation model for the input filter of the layer-control electronics and the cable, (c) measured current in a wire of the cable for supplying a single readout board (one eighteenth of a layer) taken and (d) simulated current transfer to the environmental system (PE).

6. Cabling and power supplies

Since the connection to the environmental ground (PE) is defined at the beginning of the layer and the consumed current fluctuates with the bunch structure of the accelerator, special care has to be taken that large currents are not induced into foreign systems by capacitive coupling, nor large currents loops build up and overlap with own or foreign subsystems. The same risk appears if the currents are introduced into the PE or are not guided parallel to the supply cable. This requires slow slopes in voltages and currents, low couplings by capacitance and by inductance, and a good nearby return path for each current.

Since the last component for the functionality of the layer electronics was a capacitor with a voltage change during the train (0.6 V), see figure 6, the cable should only be connected with a reasonable impedance to that capacitor. Figure 7 demonstrates with a PSPICE/VHDL-AMS simulation[12] the induced currents depending on the time constant of an RC-filter between the cable and the capacitor for charge storing. The power supply was introduced as a voltage source without stray-effects to the PE. Therefore the simulation is idealized with compensating currents in the supply and return line. The major effect is caused by common mode voltage changes due to the different couplings of supply and return line at the control electronics and capacitive coupling of the cable to the metal support, which is needed to guide currents induced by non ideal cable into the environment. The capacitance was measured for a simple cable, $3 \times 1 \text{ mm}^2$, to be 70 pF/m taped to a metal plate, which is a typical value for cables (figure 7).

To estimate the importance of the induced current one has to account for the 1500 layers in the real barrel calorimeter. The result from the simulation shows that the order of magnitude in the total amplitude can be gained at lower frequencies which increases further with increasing frequency. Although the simulation shows very good behavior for the main signal path, one has to keep in mind that all parasitic couplings have been omitted. Therefore this reduction of sensitivity might be needed and realistic EMI-filtering is foreseen by installing an input filter with a long time constant.

The impact for such a powering scheme on the choice of power supply requires that galvanic isolation per channel is needed and that a low coupling to the PE-system would be preferred (whilst keeping its own EMI-impact small). Ideally the layers would remain individually connected to power supply channels and only at the service end bridged to the PE by a low inductance wiring. Minimizing the space requirement whilst ensuring cables remain installable requires techniques for collecting the wires from a set of layers into a common cable. Combining layers has the advantage that fewer wires to the outside infrastructure are required with a corresponding reduction in the number of power supply channels. Disadvantages are that

layers are coupled, impedances of the SiPM to surrounding PE increases and connectors have to be rated for the high current of the group. This concept requires a large number of low power isolated power channels from multi-channel supply instruments or fewer with ferrite decoupled channels located outside the main magnetic field of the ILD.

7. Summary and outlook

First measurements and simulations show that the use of a multilayer PCB structure populated with groups of capacitors allows the fast components from the current switching of the ASIC to be absorbed locally. The total charge for handling a bunch train at ILC can be provided by a voltage regulator and capacitors mounted at the cooled service end of each readout layer. Since the SiPM readout is the most sensitive part in the system electronics ground and the surrounding PE-ground of the steel structure should be connected near to the layer. With the limited space and accessibility it is proposed that the connection be made at the service end of the layer with a short low impedance wire and allowing for slow changes of the voltage between the grounds along the layer. Extrapolations of the tests with a single readout board shows that the supply voltages can be kept stable within 80mV and well stabilized before the train starts. Small currents will be introduced into the stainless structure (2 mA/layer). Most of which will flow back to the nearby connection point of PE-ground and electronics ground. The impact on the design of the power supply system in the electronics rooms are that multi-channel galvanically isolated supplies are required. As a compromise grouping a few channels together with a reasonable large impedance might be possible. For the connection cables a solution has to be found which keeps the cabling well sorted within a minimum on space. Multi wire cables, from which the wires split at the end to the layers, are a technique which looks promising.

Today only individual components of the final system are available, consequently a lot of tests will have to be done whilst the system is growing and when combined with other subdetectors. Additionally simulations and estimations will have to be proven, when the systems gets available. Combining the requirements on the electronics with the constraints from others will lead to compromises requiring proving and testing.

Appendix A. Acknowledgments

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