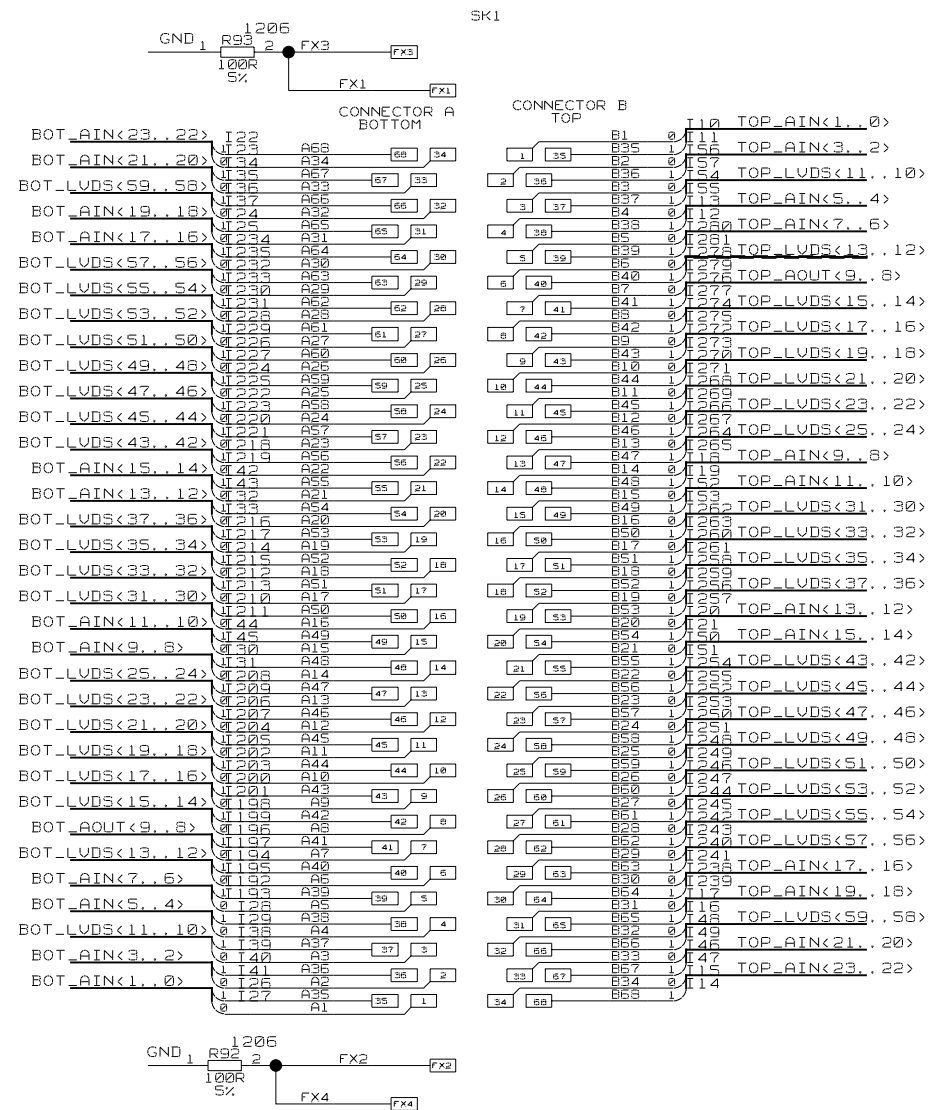
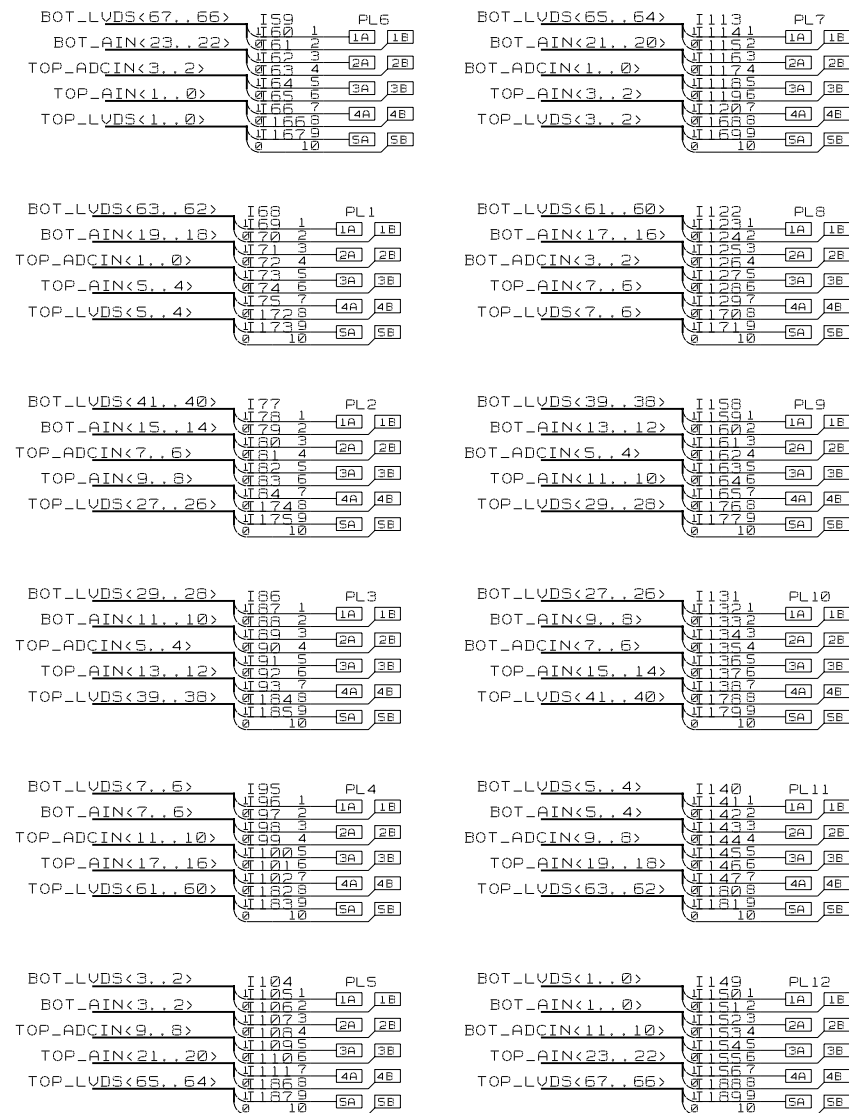


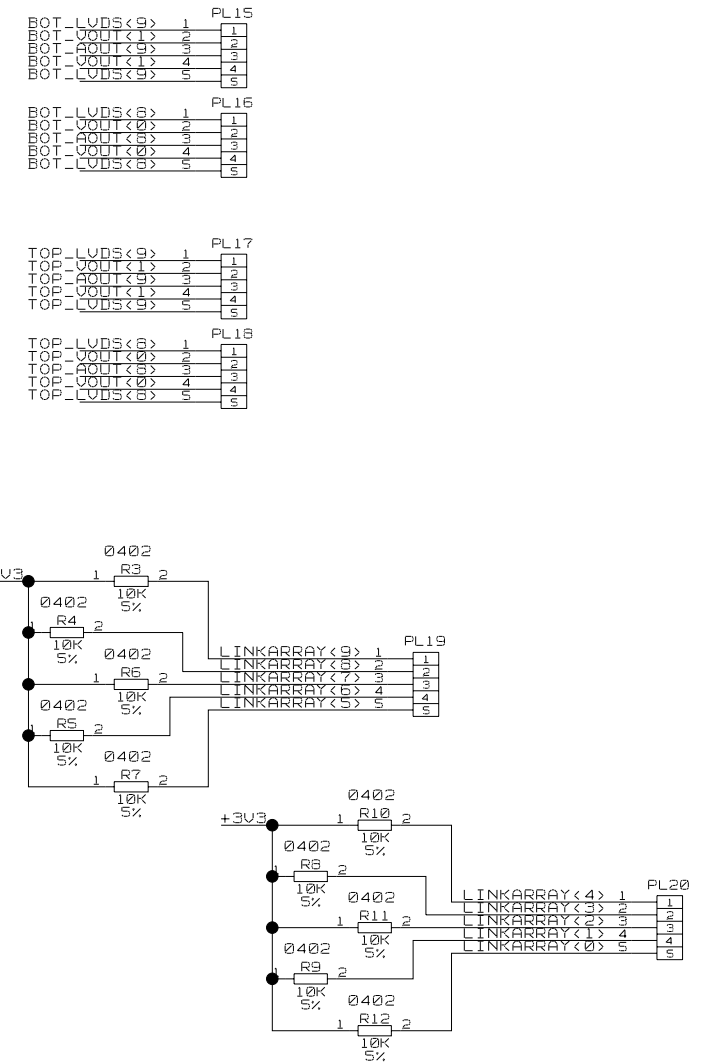
THIS PINOUT HOPEFULLY WILL NOT CHANGE



ANALOGUE INPUT SIGNALS

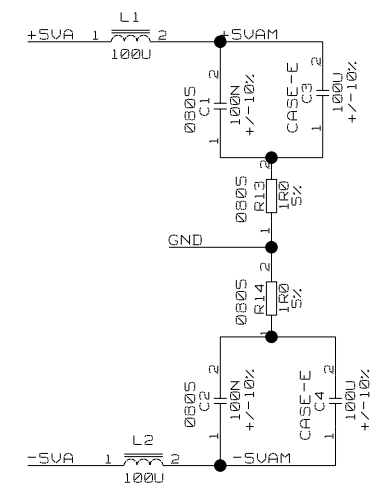
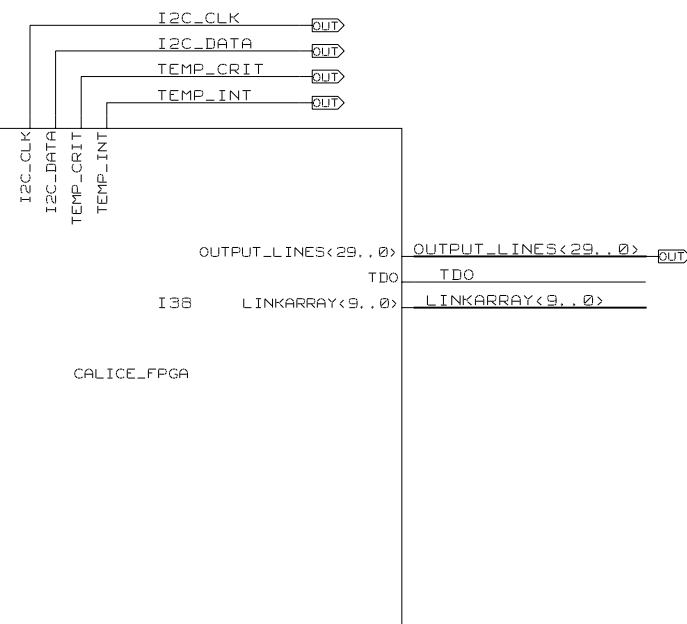
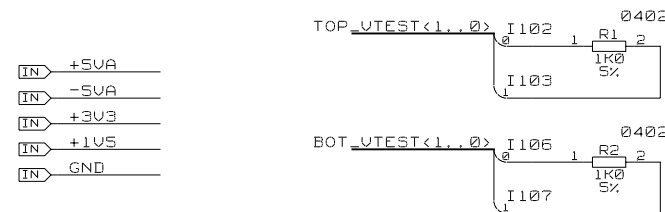
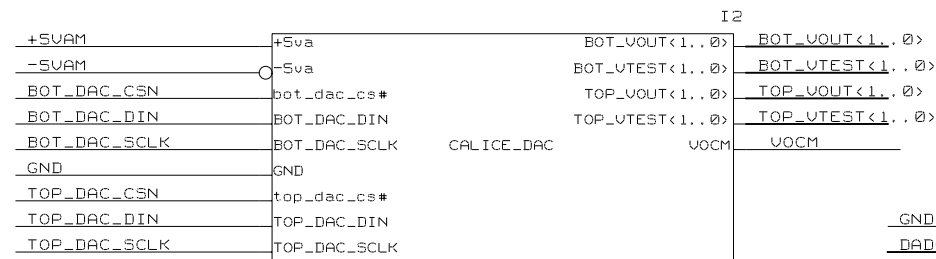
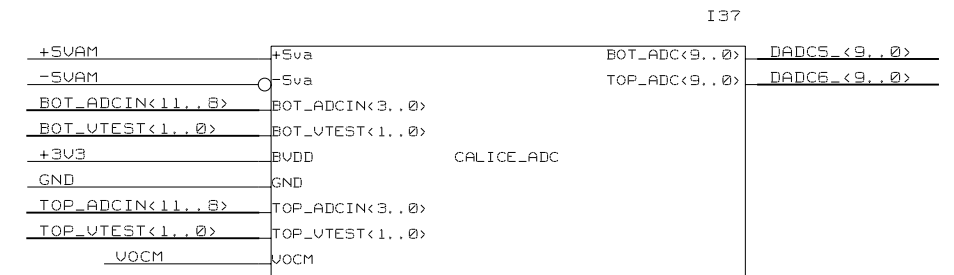
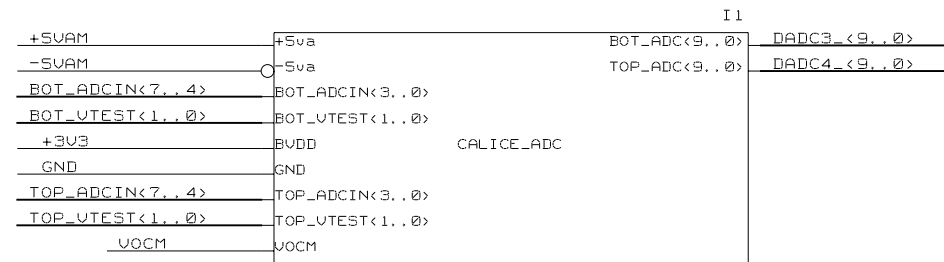
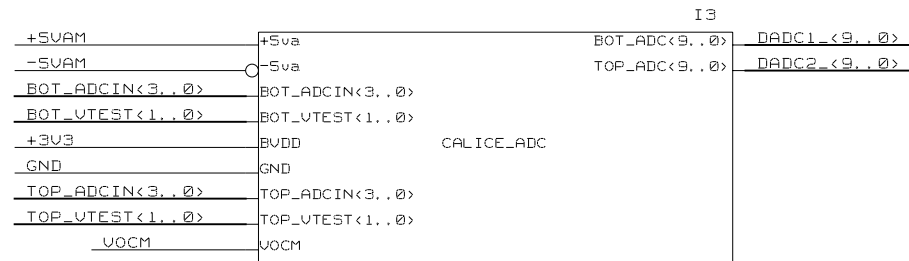


ANALOGUE OUTPUT SIGNALS



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SCSI CONNECTOR AND SELECTION JUMPERS						
A2						



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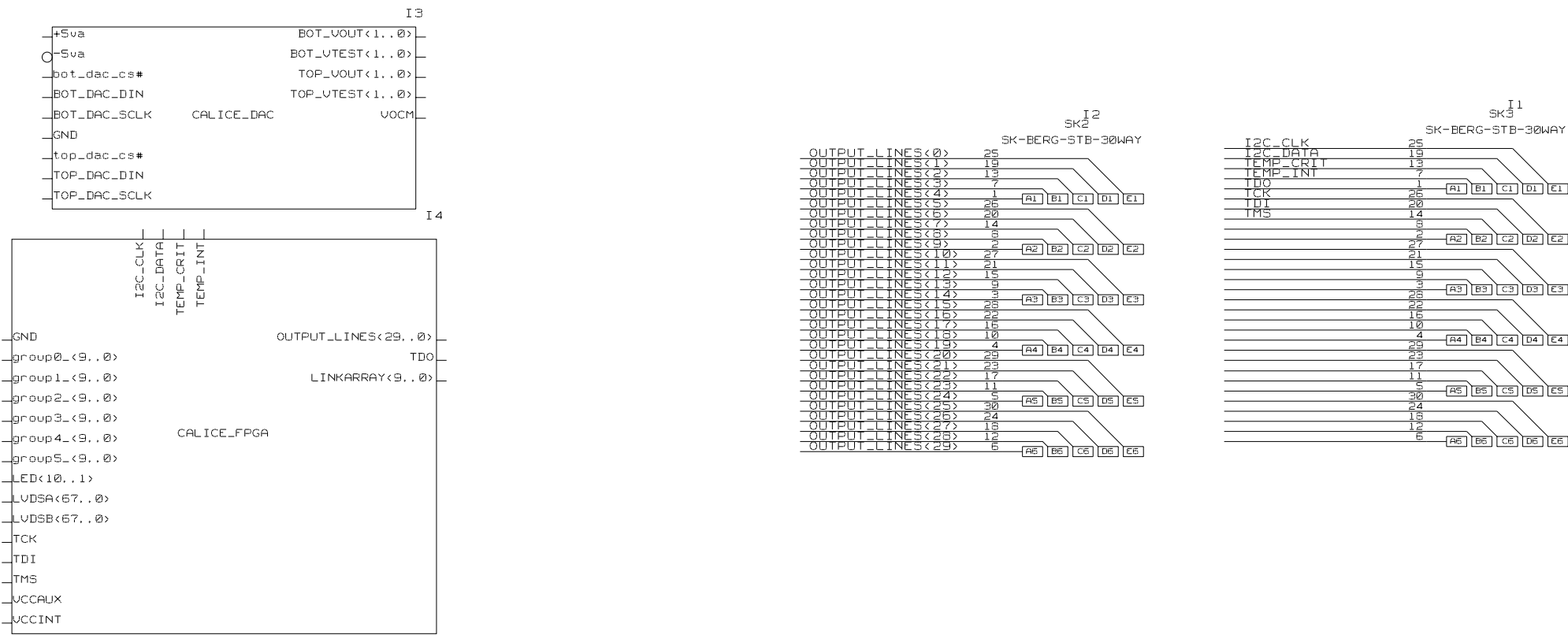
CCLRC
COUNCIL FOR THE CENTRAL LABORATORY
OF THE RESEARCH COUNCILS

TITLE
ALL MODULES

	
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DUMMY COMPONENTS

DUMMY MODULES NOT USED BELOW

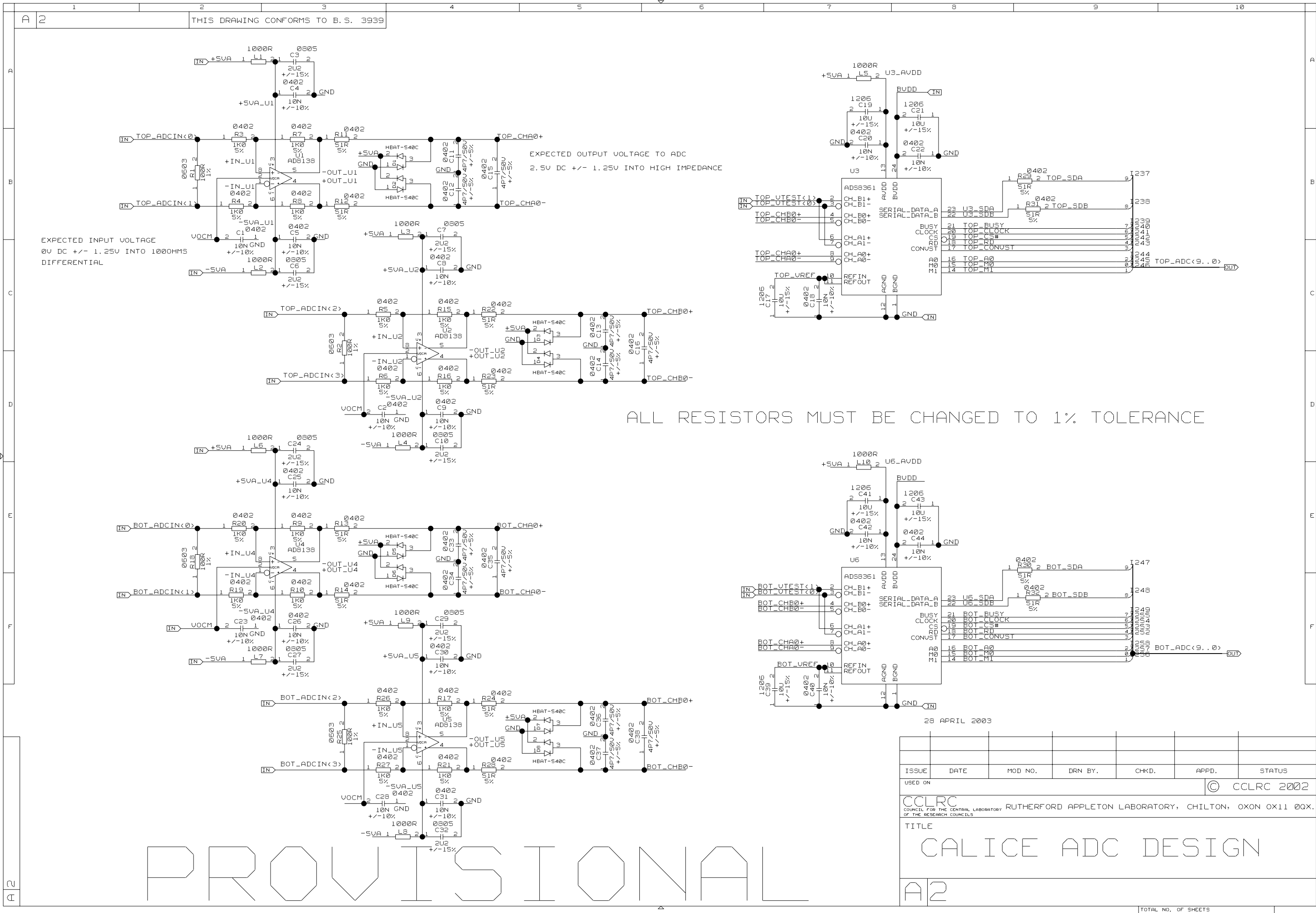


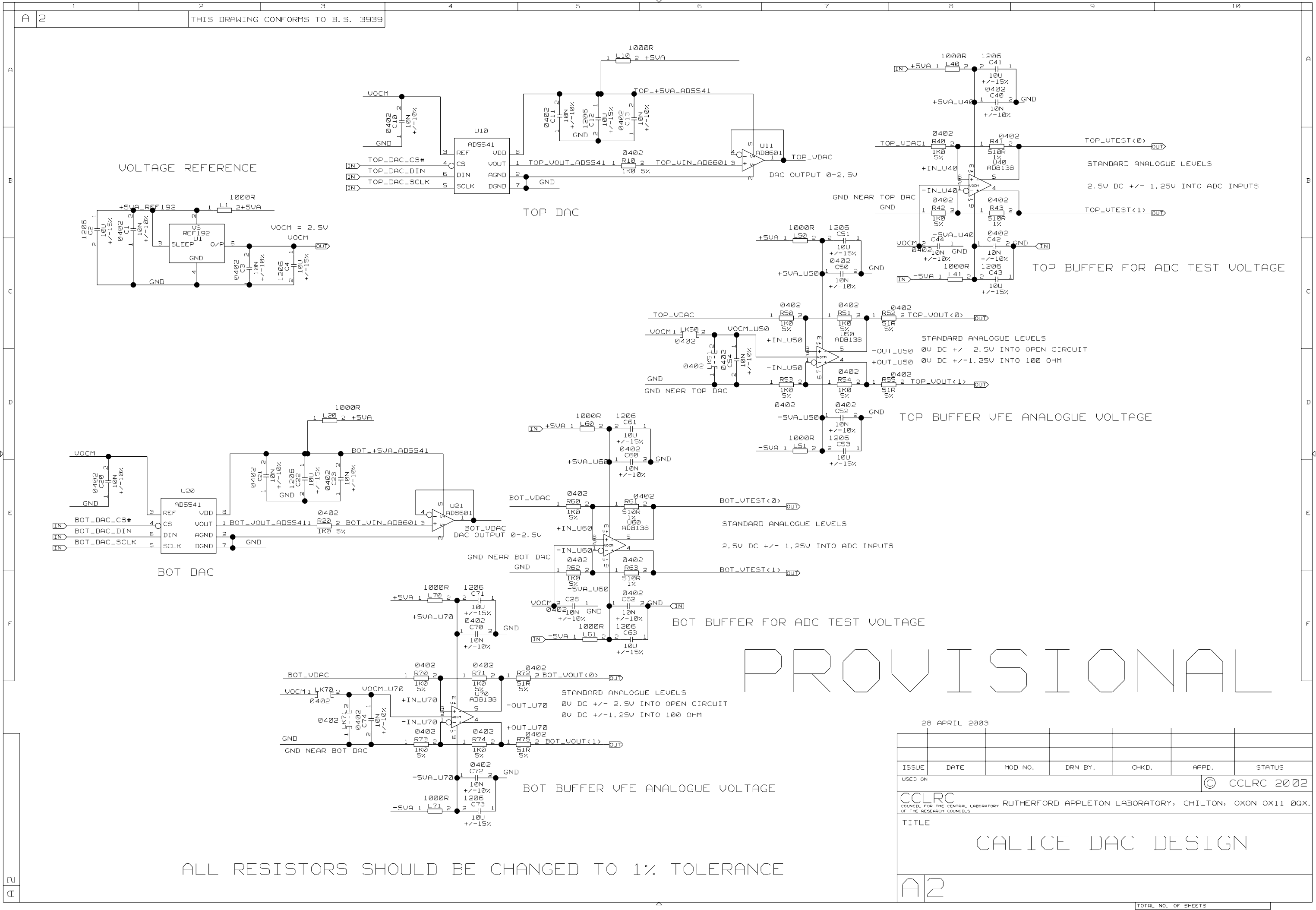
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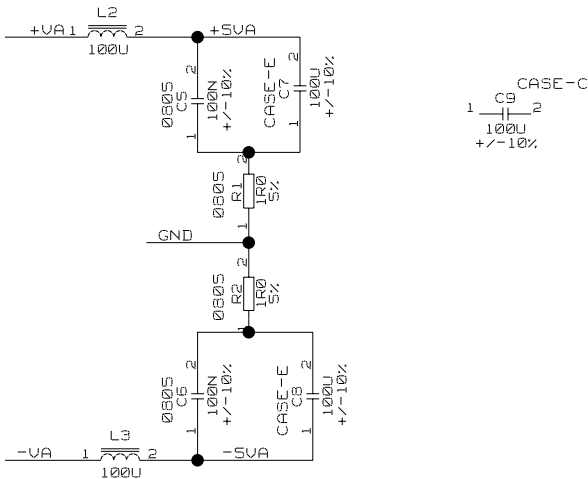
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USED ON						© CCLRC 20
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TITLE						
A2						

TOTAL NO. OF SHEETS





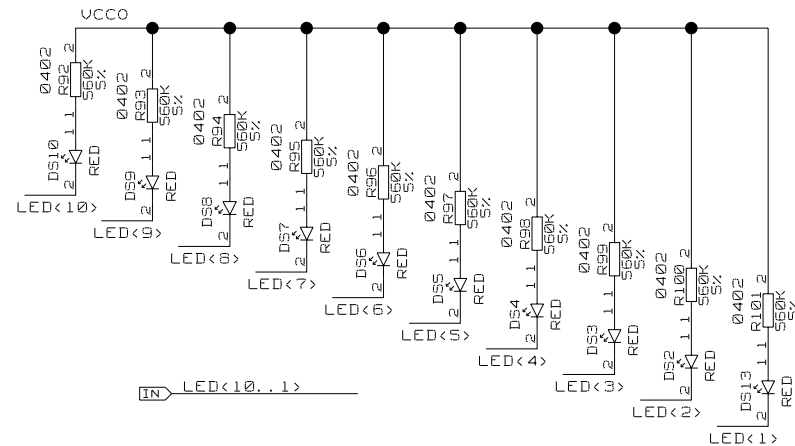
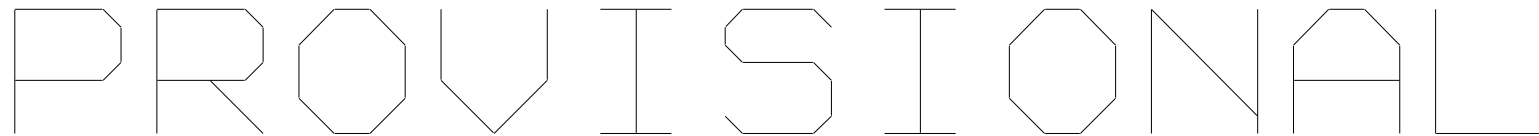
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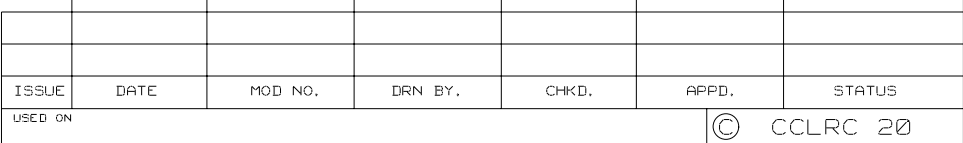
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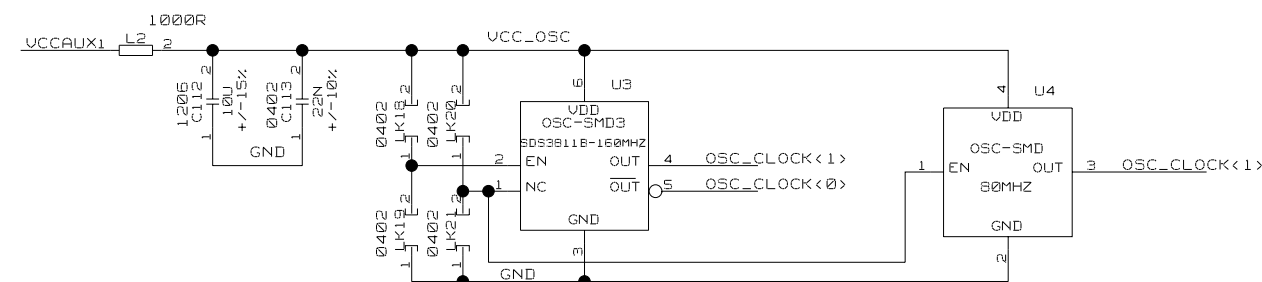
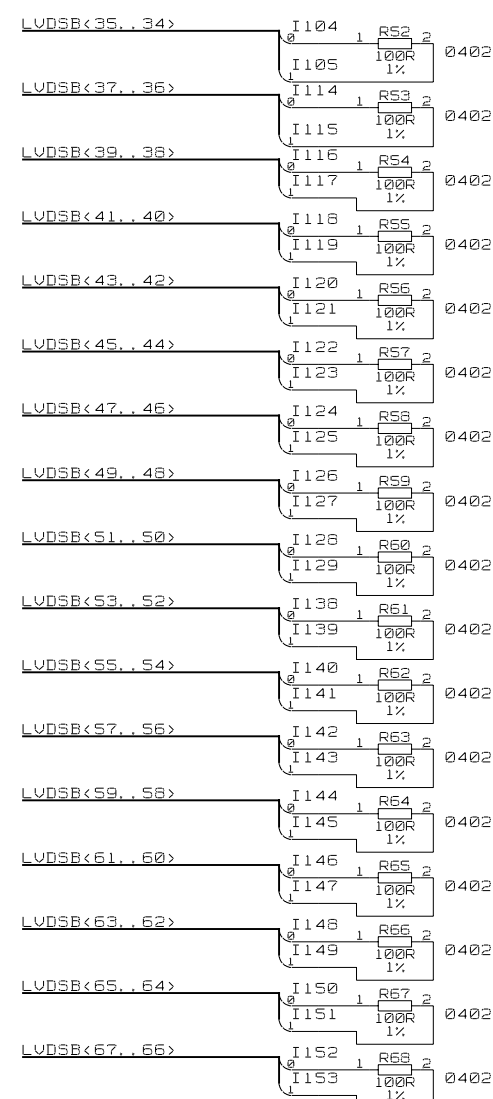
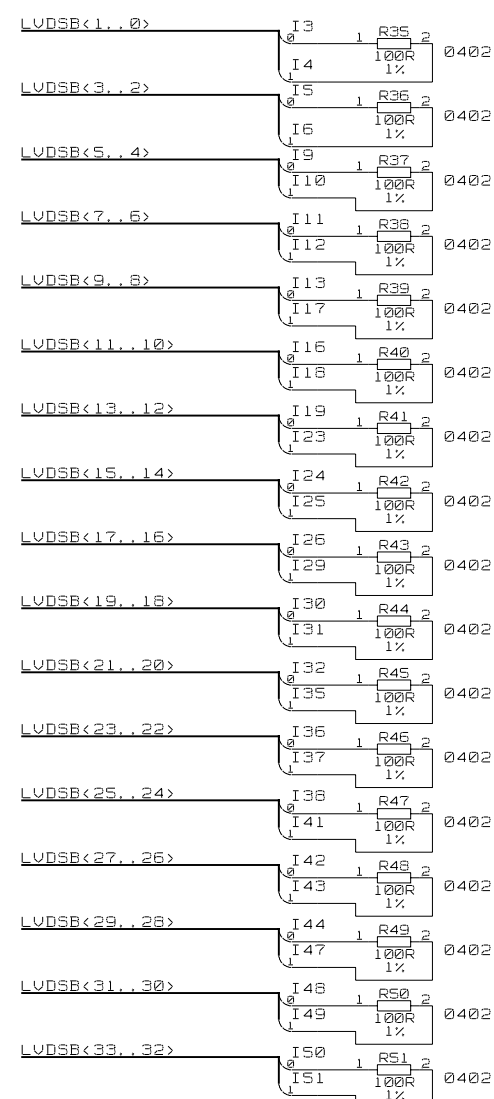
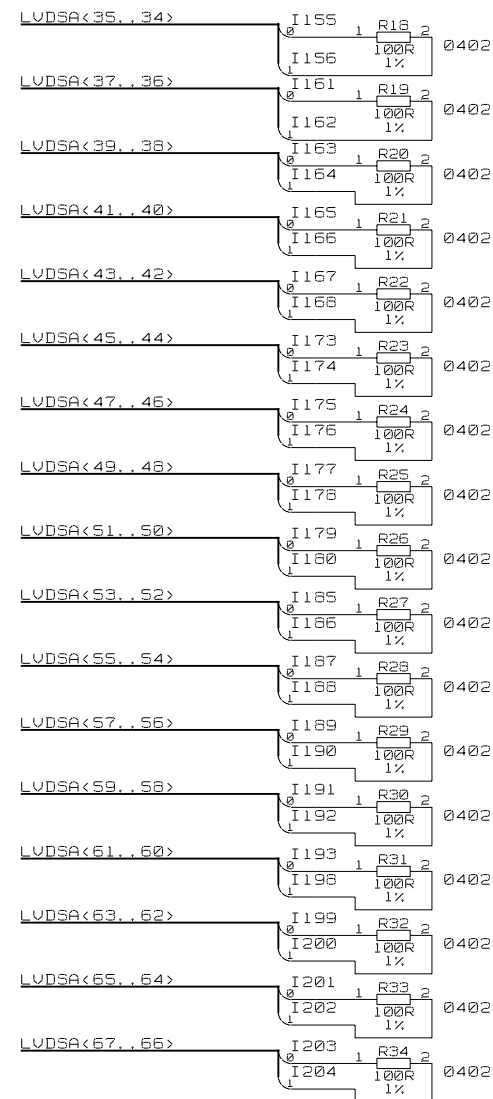
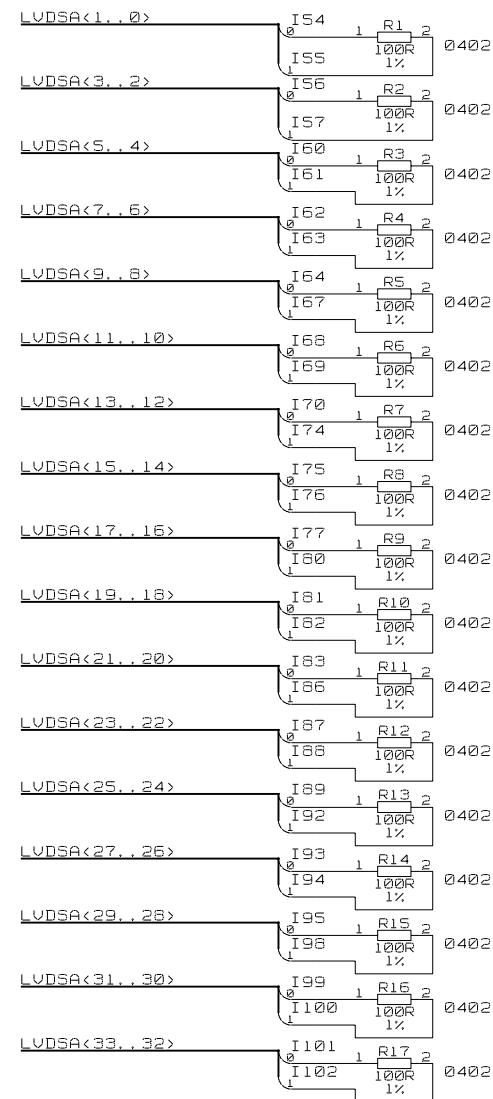
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TITLE						
A2						
TOTAL NO. OF SHEETS						



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TITLE FPGA DECOUPLING AND 2V5 LVDS VCCIO PSU						
A2						



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TITLE LVDS TERMINATIONS							
A2							

A

B

C

D

E

F

2

C

A

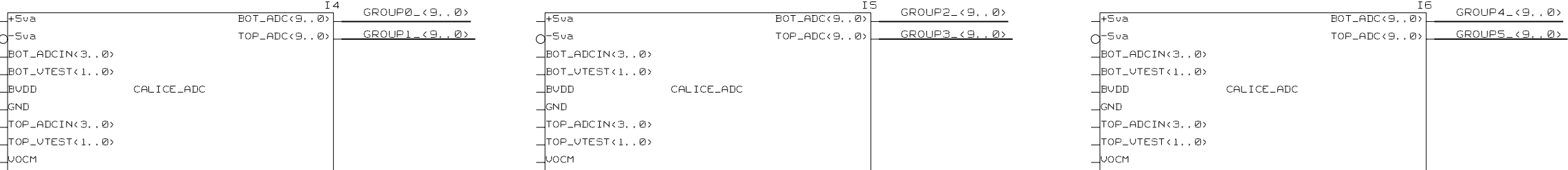
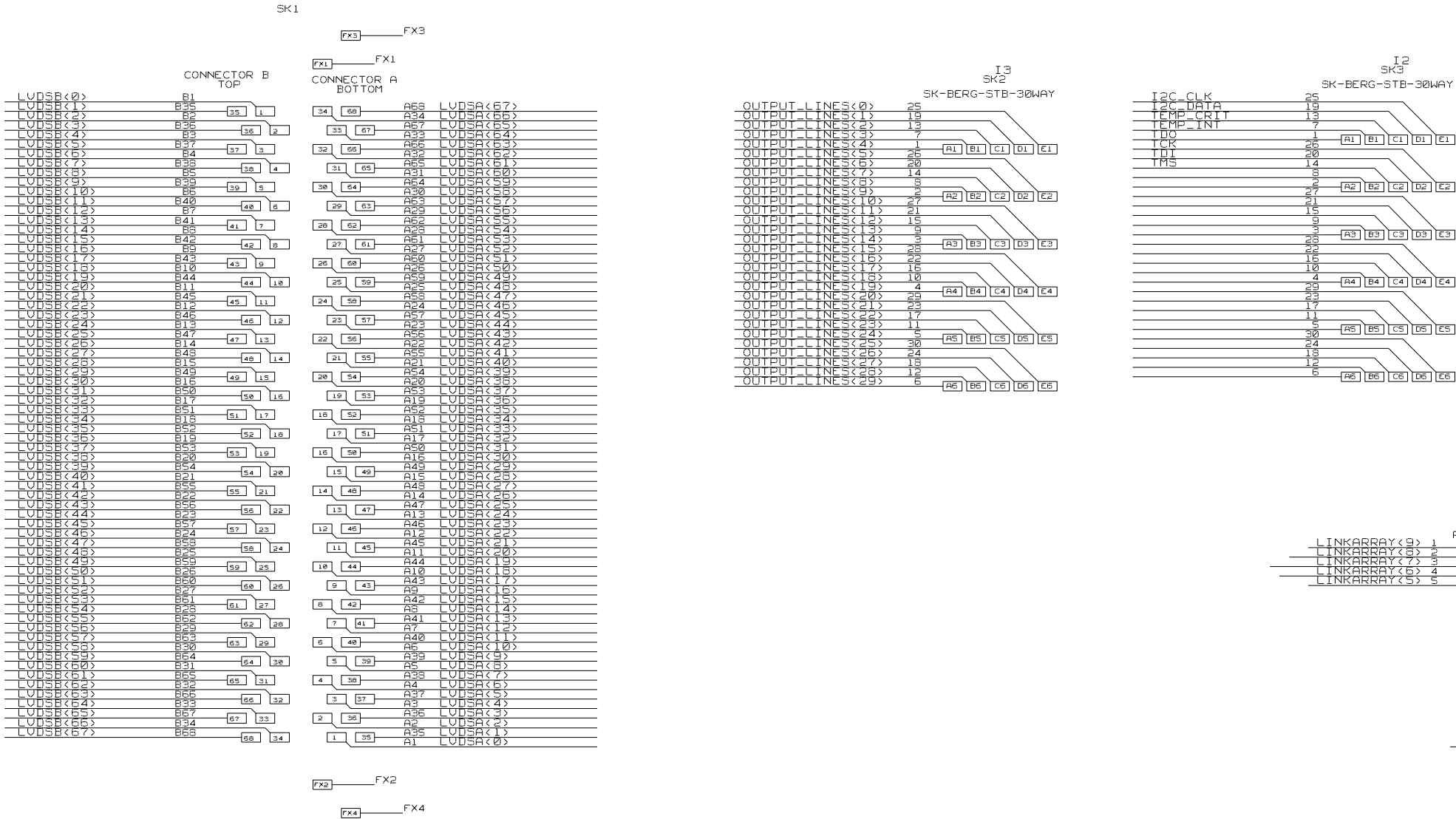
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DUMMY COMPONENTS						
A2						

TOTAL NO. OF SHEETS