Pin requirements (updated 23 May 2003 to indicate my requirements)

These are the basic pins for the ECAL (see table below), all other remaining signals will be connected to the FPGA in suitable LVDS pin pairs to allow the maximum number of signals to be used for the HCAL.

area, function	I/O	-	type	spec 100/120 ohms ?	number	pins	ac V te
Readout scheme	-	-	-	-	-	-	-
output signal	in	.	analogue	differential	12	24	Y
Clock	out	CLOCK	digital	LVDS	1	2	Y
Hold	out	HOLD	digital	LVDS	1	2	Y
Shift Register input	out	SRIN	digital	LVDS	1	2	Y
Shift Register reset	out	RESET	digital	LVDS	1	2	Y
Shift Register out	in	SROUT ?	digital	LVDS	1	2	*Y*
LED driver	out	ADDRESS	digital	LVDS	1	2	Y
gain control 1 or 10	out	GAIN_SW	digital	LVDS	1	2	Y
Calibration scheme	-	-	-	-	-	-	-
input signal	out	VCALIB	analogue	differential	1	2	Y
strobes	out	TCALIB<2..1>	digital	LVDS	2	4	Y
selects	out	ENABLE<6..1>	digital	LVDS	6	12	Y
Card identification	-	-	-	-	-	-	-
project (ECAL/HCAL)	in	.	digital	LVDS	1	2	Y
card ident	in	.	digital	LVDS	3	6	Y
Totals	-	-	-	-	32	64	-

signals to the readout card (in) and from the readout card (out).

All LVDS pairs on the FPGA that are connected to the SCSI connector will have 100R, 0402 termination resistors under the BGA (probably 120R to reduce power dissipation). A choice will then be made at assembly/IP development time as to the direction of the pair and whether or not the termination resistor is required. This approach will allow the VFE-PCB designers some flexibility in choosing the exact pairs used when designing their PCB.

Pin selection

The differential analogue inputs will be spread throughout the length of the connector to match the height profile of the analogue layout.

The circuit on the top of the PCB will be connected to the bottom front connector.

A similar arrangement of connections to those on the connectors will be found on the FPGA but interleaved to minimise vertical routing.