The VFE card (a perspective from the readout card)

The VFE card is expected to be very similar to the block diagram below. It must have interleaved analogue outputs from the VFE chips as shown to ensure that the link array can work with all the expected versions of the card.

The pin numbers are given with the expected orientation of the differential signals. The pins are traced through to there various net names, if the "BOT" is replaced with "TOP" then the top SCSI connection net names are formed.

I have now triple checked, probably more times than that, the link array and scsi connections, sorting out alot of problems. All previous "SCSI CONNECTOR AND SELECTION JUMPER S" circuit are now OUT OF DATE. The latest released top level circuits can be found here with 15 May 2003 as date circuit diagram

see also Calibration channel & position matrix.xls

12 channel VFE card

Expected connection of analogue signals to/from the 12 channel VFE module.

This diagram is a symbolic representation of the VFE board as viewed from the top, it is based upon the 6 channel VFE prototype. The main point to note is that the two groups of analogue outputs must be interleaved as shown to allow the link array to work correctly on the readout card.

The exact SCSI pin numbers are used, note the standard pin numbering on the SCSI connector is not linear, pairs as used are closer together than the pin numbers suggest.