Specification of the readout electronics for the CALICE beam test

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Abstract

The specifications for the readout electronics to be used in the beam test for the CALICE collaboration are presented.

NOTE: This is a working document and is open to change. The specification should be finished by July 2002.

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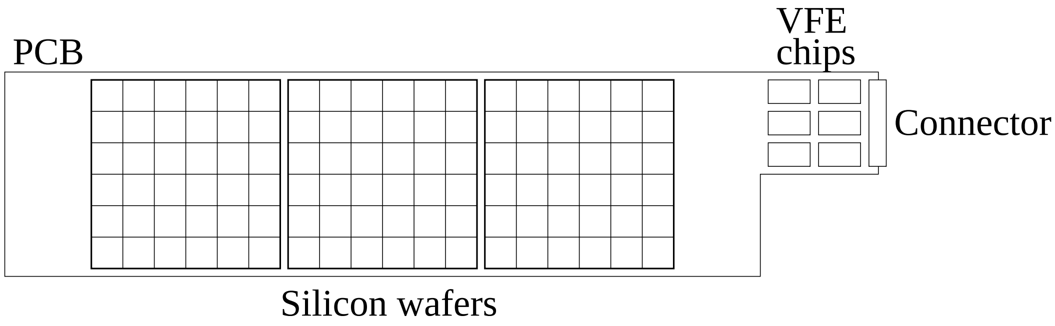

Figure 1: Schematic of one row of three silicon wafers mounted on a PCB with 6 VFE chips.

1 Introduction

The CALICE collaboration plans to test a prototype tungsten-silicon electromagnetic calorimeter (ECAL) with a beam in early 2004. The prototype will have around 10000 channels and the UK hopes to provide the readout electronics and data acquisition for this experiment. There will also be a hadronic calorimeter (HCAL) prototype although the UK is not involved in this side of the project. The eventual aim of this study is to design a calorimeter for the TESLA linear collider.

The prototype calorimeter will consist of 30 layers of silicon diodes. Each layer comprises a 3×3 array of silicon diode wafers, each containing a 6×6 array of diodes. Each diode needs to be read out and so corresponds to a channel. Hence, each wafer contains 36 channels, each layer contains $36 \times 9 = 324$ channels and the whole prototype is $324 \times 30 = 9720$ channels.

The three silicon wafers in a row in each layer will be mounted on PCB's which route the diode signals (without amplification) to the very front end (VFE) chips which provide amplification and shaping. Each layer therefore consists of three such PCB's which are mechanically connected but electrically independent. The schematic structure of one PCB is shown in Fig. 1. The current implementation of the VFE chip, the FLC_PHY1 chip [?], will handle 18 channels and will provide a sample-and-hold on an external trigger for each channel. It will have a single gain and will multiplex the signals from the 18 channels onto a single output line at up to 1 MHz. The VFE chip will also accept a calibration signal which is used to inject a pulse at the chip input.

The diodes, VFE chips, wafer PCB's and their power supplies, as well as the trigger and its logic, will be provide by non-UK groups, while the UK will need to provide all the readout electronics downstream and the DAQ system to read it out. All signals from each PCB are assumed to be routed through a single connector. This will provide the well-defined interface between the two parts of the electronics. The UK will provide any cables needed from this connector.

2 Requirements and interfaces

2.1 Front end requirements

The requirements for the prototype UK readout electronics with regard to the front end electronics are as follows:

- It must digitise and read out all 9720 channels. These are grouped into $6 \times 18 = 108$ channels on each PCB, with 90 PCB's in total.

- With the VFE chips having a single gain, then at least 12 bit, and preferably at least 14 bit, ADC's are needed.
- It must supply the sample-and-hold timing signal to each PCB. The sample time must be adjustable to coincide with the shaped pulse peak, which occurs ~ 180 ns after the charge deposit in the diodes. This could be done in the external (non-UK) trigger logic but it would be useful for this to be software configurable within the UK electronics.
- It must supply the multiplex clocking signal at up to 1 MHz to each PCB to generate the analog signals on each VFE chip output line.
- It must supply adjustable calibration voltage, timing pulse and channel selection signals. The voltage should be adjustable to 16 bits. The subsequent sample-and-hold signal also needs to be adjustable relative to the timing pulse. The channel selection determines to which channels the calibration pulse is applied; $2^6 = 64$ different combinations should be sufficient.
- It must be consistent with the readout of the other parts of the beam test system, namely any beam monitoring detectors, the trigger system and the HCAL detector. Note, these systems are not yet defined. Also, since the development of the readout for the HCAL part of the beam test is significantly undermanned, it would be useful if the UK electronics could be made adaptable and so be used for the HCAL also. This would only be considered if the extra engineering effort and expense required is minor.
- It should be stand-alone as far as possible. The beam test location is not yet known so there is no information about the available infrastructure. Specifically, the readout system should not depend on external networking being provided.
- It should be flexible to deal with unforeseen situations and uses. As many of the settings as possible should be configurable through software.

2.2 PCB connector interface

The UK readout electronics is assumed to have an independent ground from the wafer PCB's. Hence, all signals on the PCB connector which provide the interface to the UK readout are assumed to be differential. All digital signals as assumed to be LVDS. The analog signal specifications are not yet known. The signals on the connector are assumed to be as follows:

- Digital sample-and-hold timing signal. A single signal on the connector is distributed on the PCB to all 6 VFE chips. (However, note comments under trigger interface below.)
- Digital multiplex clock signal. Again a single signal is distributed to all VFE chips so they are read out in parallel.
- Digital multiplex shift register input signal; again distributed to all chips.
- Digital multiplex shift register output signal; this is the logical AND of all six signals returned from the VFE shift registers.
- Analog multiplexed signal output. There must be six lines, one from each VFE chip. The voltage range needs to be specified.
- Analog calibration voltage. A single voltage is applied to several channels as determined by the calibration selection logic on the PCB. The voltage range still needs to be specified.

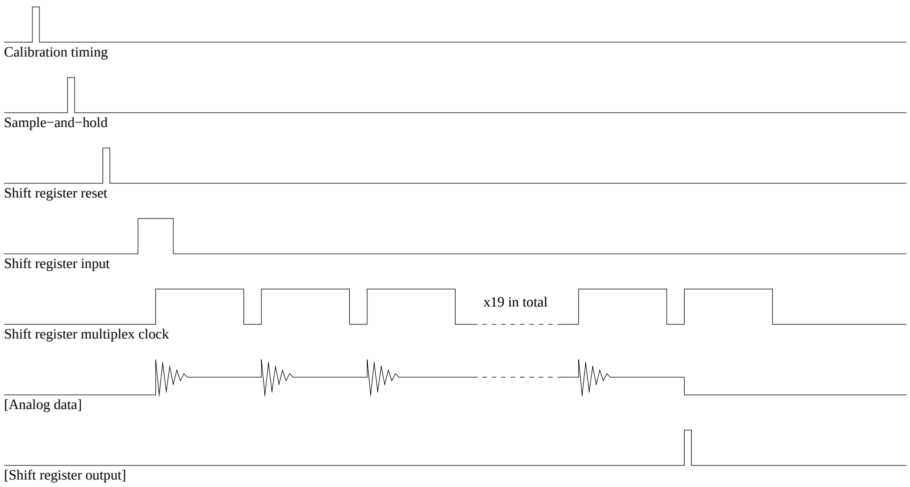

Figure 2: Time-dependent signals on PCB cables.

- Digital calibration pulse timing signal. Again, a single signal is distributed on the PCB as required.
- Digital calibration selection. Six lines are needed for up to 64 different combinations.

The time-dependent signals are shown in Fig. 2; all other signals are constant during data capture and transfer. The total number of signals is then $1 + 1 + 1 + 1 + 6 + 1 + 1 + 6 = 18$, requiring a 36-pin connector on each PCB. The signals are 7 analog and 11 digital, of which 6 analog and 1 digital are input and the rest output.

2.3 Trigger requirements

The trigger interface is not yet well defined as the basic architecture is not chosen. The UK system must be built to accomodate any or all of the following:

- The trigger is sent to the UK system and needs to be adjusted in time to coincide with the shaped pulse peak (which may be a different time for the ECAL and HCAL) to an accuracy $\sim$ 10 ns and within $\sim$ 180 ns. Alternatively, only a "post trigger" may be received, indicating readout is needed.
- Further triggers may need to be vetoed until readout is complete, either within the UK electronics or by outputting a disable trigger signal. Alternatively, a clear signal to the trigger logic may be needed.
- Beam particles close in time to the trigger may cause a trigger to be aborted and the system needs to be able to handle this.
- The trigger signal may need to be distributed to the HCAL through the UK system, even for the digital option, to enable the time adjustment (the first item above) to be implemented.
- Different triggers may be required, so cosmic trigger and beam veto trigger select signals will be needed.
- The trigger logic may generate the calibration signal so a calibration enable signal may need to be supplied.

2.4 Trigger interface

Assuming the trigger logic is implemented in NIM, then the following gives the trigger interface:

- Trigger signal, input, NIM.
- Abort, input, NIM.
- Veto, input, NIM.
- Trigger disable, output, NIM.
- Clear, output, NIM.
- Cosmic trigger select, output, NIM.
- Beam veto trigger select, output, NIM.
- Calibration enable, output, NIM.
- Multiple (?) valid trigger signals, output, LVDS?

2.5 Data output requirements

The data output requirements are quite minor:

- An event output rate of at least 100 Hz is needed although a higher rate is desirable.
- The output format should be machine independent, e.g., ROOT.
- If threshold suppressed, then unsuppressed data should be written out regularly to enable pedestals and noise to be measured for each channel.
- It should consider whether the 2 GBytes file system limit on some operating systems needs to be respected.

2.6 Data output interface

The data output interface is relatively flexible.

- Compact, self-contained data files which can be read on most operating systems.
- Access to all configuration data used for each run.

3 Overview of proposed readout system

The following sections describe the proposed UK readout electronics which satisfies the above requirements. Due to the short timescale, simplicity and robustness were emphasised over high performance or cost reduction.

The proposed system has the cables from the wafer PCB's connecting directly to 6U VME boards, with all the necessary readout electronics on these boards. The system would run triggered and read out each event before allowing the next trigger to occur. This would be controlled by a single VME trigger handling board which distributes the trigger across the backplane. No data reduction is done in hardware, so all 9720 channels are read out for each trigger.

The basic unit of the readout is based on the 90 wafer PCB's. These each hold 108 channels which are multiplexed onto 6 lines. It would be convenient to contain the whole system in a

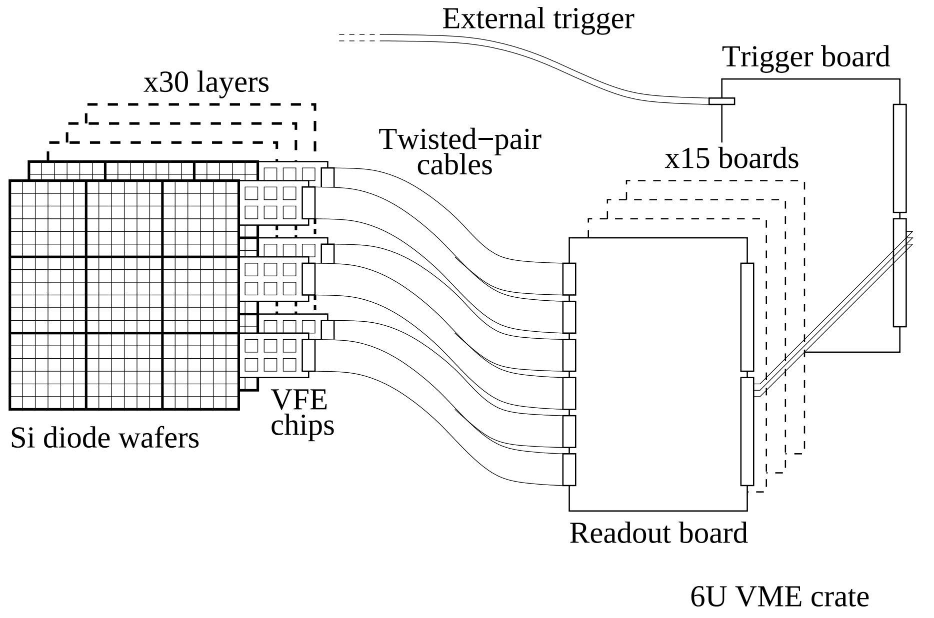

Figure 3: Overview of the proposed ECAL readout system.

single standard VME crate of 21 slots. Assuming a PCI/VME interface card and a single width trigger card, this leaves 19 slots for the readout boards. The obvious division is then 15 readout boards, each handling the signals from 6 wafer PCB's, equivalent to 2 of the 30 layers of the calorimeter. An overview of the proposed ECAL system is shown in Fig. 3.

A further board is required for testing the readout boards during prototype and production. This test board will send and receive the signals to and from a single readout board using the same cables as the wafer PCBs.

4 Readout boards

4.1 Requirements

These are effectively those given for the front end in Sec. 2.1.

4.2 Proposed implementation

A conceptual layout of the proposed implementation of the readout board is shown in Fig. 4. Each readout board must digitise the signals from 6 wafer PCB's, which is therefore $6 \times 6 = 36$ multiplexed VFE chip outputs. It will therefore contain 36 ADC's. The board is controlled by a master FPGA. The board takes in six twisted-pair ribbon cables from the wafer PCB's through its front panel. The signals for each are handled by six slave FPGAs. The master FPGA implements the VME interface and distributes the trigger, and configuration data to the slave FPGAs, while collecting event data from the slaves.

The board has its own ~ 100 MHz clock, which allows timings to be determined to ~ 10 ns divisions. Only the sample-and-hold timing is needed to this accuracy. The rest of the board logic is run at a multiple of the 100 MHz clock, taken to be $\times 8$ or 12.5 MHz here. The trigger signal is taken from unused lines on the crate backplane. The calibration voltages are set by 16-bit DACs.

At any given sample, the ADC's are each outputting a 16-bit digitised sample, so the data volume into the slave FPGAs is 16 bits at up to 1 MHz.

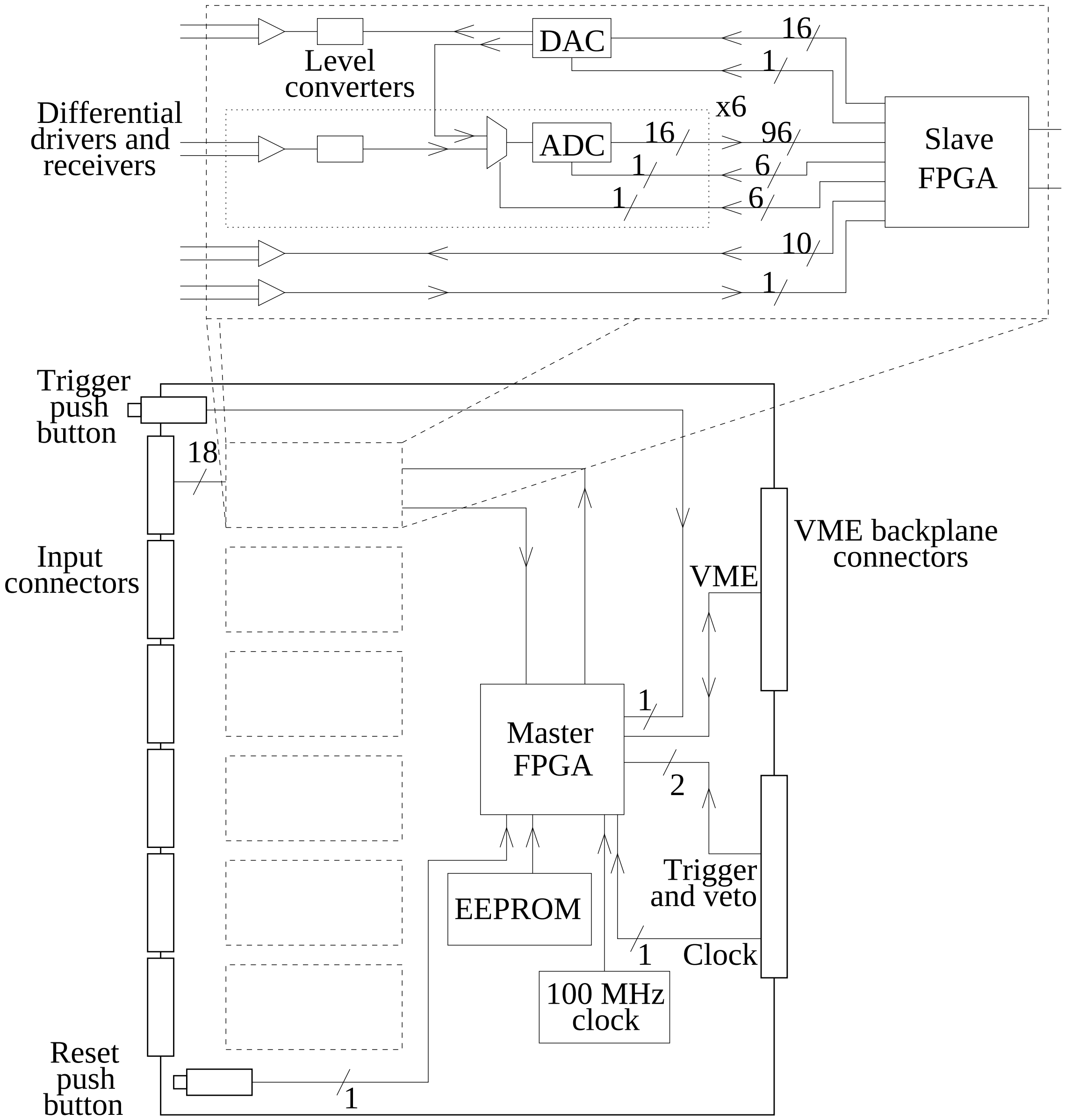

Figure 4: Conceptual layout of the readout board. For clarity, the set of signals to only one of the six connectors is shown.

Each slave FPGA receives data from 108 channels, which is 108×2 bytes $= 216$ bytes and so should be able to be stored within the FPGA. The master FPGA receives data from 648 channels, which is 648×2 bytes $= 1296$ bytes and should also be able to be stored within the FPGA without needing an external memory component. Each event is 9720 channels $\times$ 2 bytes $= 19440$ bytes or 19 kbytes. This will take at least 1 ms to read over VME and so will limit the event rate to a maximum of around 1 kHz, although a realistic estimate is probably more like a few hundred Hz.

4.3 Proposed state machine

The readout sequence is as follows.

1. Receive trigger signal on the backplane.
2. Unset the ready-for-readout flag.
3. If calibration is enabled, wait for a configurable delay and send a calibration timing pulse to the PCBs.
4. Wait for a configurable delay before issuing a sample-and-hold timing signal to PCB's.
5. Wait for another configurable delay to send the shift register input signal is sent to the PCB's.
6. The first multiplex sequence is sent.
7. Go to 5) until all sequences are done (usually 18). The corresponding ADC's are sampled with a configurable phase offset from the multiplex clock. The data from these ADC's are stored in the slave FPGAs.
8. Transfer the data from the slaves to master FPGAs.
9. When all data have been stored in the master FPGA, then set the ready-for-readout flag.
10. Optionally, VME readout is performed, possibly multiple times.
11. Following readout, the board waits for the next trigger and goes to 1). If a trigger arrives during the above sequence, the sequence is immediately restarted at 1).

The calibration voltage settings and selection lines are assumed to have been configured before the start of the calibration sequence, at completion of a configuration write.

4.4 Control and configuration data

The control and configuration values for the board as a whole which need to be loaded onto the board before readout are as follows:

- Clock source (backplane or local), single bit.

The control and configuration values for each slave FPGA which need to be loaded onto the board before readout are as follows:

- Sample-and-hold timing pulse delay, in units of a ~ 10 ns clock period. This allows the sample to be taken at the shaped pulse peak.
- Delay to start of multiplexing sequence, in units of the ~ 80 ns clock period. The time needed for this is unknown and may not need to be non-zero.

- Number of multiplexing sequences, usually 18 for the ECAL.
- Period of multiplexing sequence, in units of the $\sim$ 80 ns clock period. Nominally, this is around 60 to get a 1 MHz multiplex speed.
- Phase offset of ADC sampling w.r.t. multiplex clock, in units of the $\sim$ 80 ns clock period. This allows the ADC sample time to occur at a fixed offset from the multiplex switch time, so avoiding transients.
- Calibration enable flag. Determines if a readout or calibration sequence should occur.
- Calibration selection settings. Separate values should be allowed for each PCB.
- Calibration DACs settings. The 16 bit values to set the DACs.
- Calibration timing pulse delay, in units of the $\sim$ 80 ns clock period.
- DAC loopback selection, 6 bits.

As the time between the trigger and the sample-and-hold is rounded to a 10 ns period, then the trigger time to sample time will jitter by up to this amount. This gives a sample which will not be exactly at the peak. The shape at the peak can be approximated by $1 - x^2/2$, where for a standard CR-RC shape, $x = \delta t/\tau$ with δt the time from the peak and $\tau = 180$ ns for the VFE chips being used. Hence, for t off by a maximum of $\delta t = 10$ ns, then the reduction from the peak is approximately 0.0015, an offset of much less than a percent.

All data are unsigned two-byte words.

4.5 Status and event data

These data will be read out for every event. The status data are:

- Ready-for-readout, single bit.

The event data are:

- Shift register output bit, one per PCB, six bits in total.
- Digitised data, 108 2-byte words per PCB, 648 words or 1296 bytes total.

All data are unsigned two-byte words.

4.6 VME interface

The VME interface needs to allow read and write of all configuration data. It also needs a read-only interface for all the digitised data and board status. However, testibility will be helped by allowing the data to be written before a read. It would be useful for there to also be a read-only board identification, including a unique serial number.

In addition, there are some commands which must be sent using VME. The VME must be able to supply the board with a software trigger. Commands to load the configuration data from master to slave FPGAs and vice versa are needed. A software-driven VME board reset, including a reload of the FPGA firmware, would also be useful; this must not go through the FPGA itself.

It would be useful for all VME data to be of the same type, specifically unsigned 16-bit words, to minimise endian issues on different platforms. All exchanges should be A24/D16 or A32/D16. For speed, the interface should support DMA transfers.

4.7 FPGA tasks

The FPGA gate requirement is relatively low, but the number of pins is high if no serial data transfer from the ADCs is possible. The FPGA could in fact be replaced by several separate components. Each cable has a pin count of 130 signals to the FPGA; using six FPGA's of around 200 pins each, one per cable, would solve this issue without any very high density pin regions. A master FPGA to control the board, VME access and the other (slave) FPGA's would also be required, possibly of a similar type. Each FPGA would need a low gate count and so could be realtively cheap. They are considered separately below, although the functionality may be implemented into a single device.

The master FPGA needs to do the following:

- Handle configuration data read and write on VME.
- Handle configuration data write to slave FPGAs.
- Handle event data read and write on VME.
- Handle event data read from slave FPGAs.
- Handle clock source and distribution over board.
- Write over its boot EEPROM?
- Handle trigger distribution from either the backplane, VME or front panel.

Each slave FPGA needs to do the following:

- Handle the read of the configuration data from the master FPGA. The configuration data should be internally handled as a dual-ported RAM.
- Handle the readout of event data to the master FPGA.
- Handle the readout sequence to its cable, including the counters.
- Write over its boot EEPROM?

The master to slave I/O interface should be kept completely generic so that it can be used for the test board. A conceptual view is shown in Fig. 5. Configuration data for each PCB are written via VME into a dual-ported RAM buffer in the master FPGA. On a VME command, these data are copied to another buffer in the slave FPGA where they are used by the signal sequence generator. Similarly, the event data from the ADCs is stored in the slac FPGA and following the sequence, these are transfered to a buffer in the master FPGA, so readout of data from all PCBs can occur. The two buffers in the master FPGA are both read/write so that the transfer of data in and out using VME can be tested. These reads are non-destructive and can be done an arbitrary number of times. The transfer of configuration data to the slave FPGA is a write-only path from the master FPGA, to prevent contention on the bus and hence simplify the protocol. Similarly, the event data path is write-only from the slave FPGA. To test the transfer, a loopback of the configuration data into the event data buffer is provided. A VME command initiates this loop and a subsequent transfer from slave to master FPGAs, setting the ready-for-readout flag when complete. Following this, a standard VME event buffer readout gives the configuration data.

The protocol between the FPGAs should be kept simple. If the transfer is for all the data in the buffer each time, and not individual words, then no address information is required. The data could then be sent as the number of 16-bit words, followed by the data themselves. All

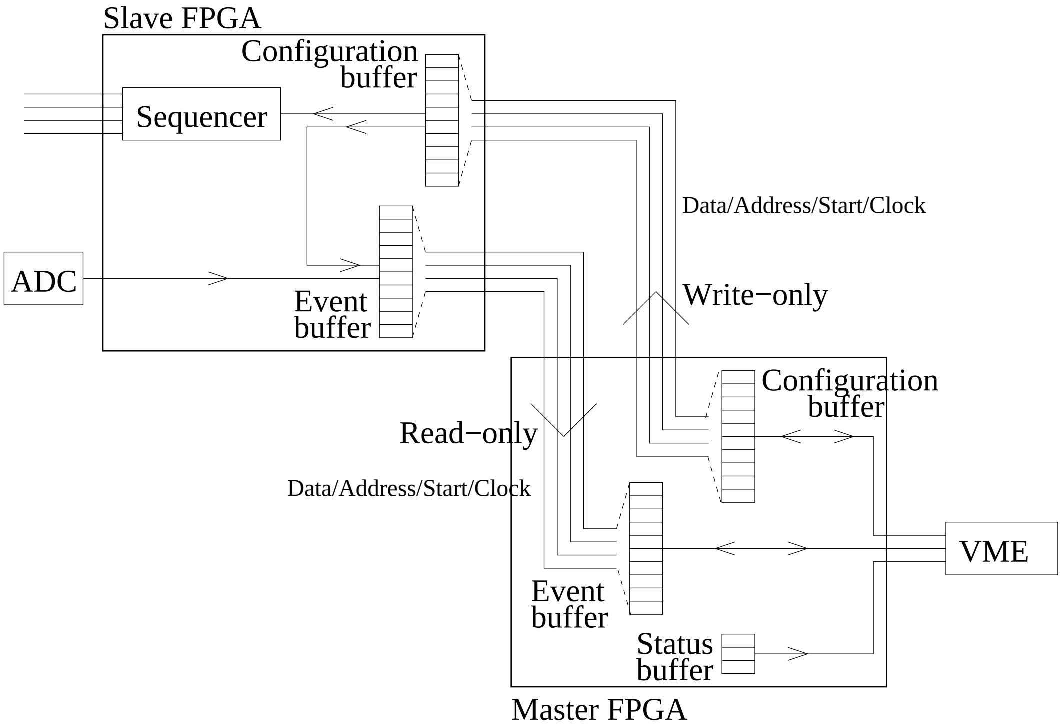

Figure 5: Schematic of data interface between master and slave FPGAs.

data transfers between the FPGAs occurs using the 12.5 MHz clock. Hence, each 16-bit word takes $\sim 1.3\mu$s to transfer serially and the whole 108 channels of event data from each PCB take $\sim 140\mu$s.

The DAC value in the configuration data needs to be acted on at the end of the configuration master-to-slave transfer, so this must be treated as a special case in the slave. However, the master data handling is completely generic and does not depend on the meaning of the data.

4.8 Inputs and outputs

Front panel: six cables, trigger push button, board reset button (recessed).

Backplane: VME, trigger, veto, clock.

4.9 Timing

To achieve 100 Hz, then each event must take a maximum of 10 ms. For 80 kBytes per event, with the digital HCAL, a large proportion of this will be taken by the VME read time, so a sensible target is to take less than 1ms total for the electronics, i.e. from the trigger time to the ready-for-readout being set.

The transfer of event data from slave to master FPGAs will be done in parallel for all six slave FPGAs. This trasnfer is for 216 bytes. Assuming a 12.5 MHz clock with a single serial bit stream, i.e. 1 bit per 80 ns, then 216 bytes will take 140 μs.

This leaves around 0.8 ms for the data capture sequence. This is dominated by the 18 multiplex clocks. These can therefore take a maximum of 45 μs per clock, which is a rate of 23 kHz. Therefore, the ADCs must run at least at 30 kHz, but higher is prefered.

4.10 Power consumption

This needs to be evaluated, but is highly unlikely to exceed the VME crate specification.

4.11 Testability

The master FPGA itself should be self testable. Its buffers will be read/write so simple data transfer can be tested. The data path to the slave FPGAs can also be tested through VME, by reading back the configuration data through the event data buffer.

The DACs can be looped back to input their analog level to the ADCs on the board, either externally using a purpose-wired connector or internally within the board. The latter would allow this test to be done trivially at any time and in situ, without removing or connecting any cables.

Front panel LEDs to help diagnostics could include; VME active, clock present, logical AND of FPGAs booted OK, calibration enabled, triggered and ready-for-readout flags.

The response to the input signals on the cables will be tested by the test board (see below).

4.12 Cost

All the following prices include VAT and are in FY02/03 £.

The NRE costs are estimated at £800. The FPGA set could be six XC2V40-4FG256CES components, each £26, one for each cable, and a further one for the VME interface and board control. ADCs are estimated at £30 each. An Analog AD5543, 0.5 μsec settling time DAC is £33. Other IC components are estimated at £300 and other hardware at £200. The board fabrication and assembly costs are estimated by comparing with similar boards.

A estimated cost per readout board, in addition to the £800 NRE costs, is therefore:

- ADCs; £30 per ADC $\times$ 36 ADCs = £1080.
- FPGA; £26 per FPGA $\times$ 7 FPGAs = £182.
- DACs; £33 per DAC $\times$ 6 DACs = £198.
- Other ICs; total = £300.
- Other hardware; total = £200.
- PCB fabrication and assembly; total = £850.

The total cost per readout board is therefore approximately £2800.

5 Trigger handling board

5.1 Requirements

The given requirements are:

- Receives a TRIGGER from external source
- Outputs this TRIGGER to all ReadOut Boards via J2 backplane bus
- Generates a VETO which stops any further TRIGGERS being output until the VETO is cleared via VME
- Outputs a variably delayed trigger to the HCAL system.

The proposed additional functionality is:

- Stand-alone generation of triggers (from front panel push-button)
- Stand-alone generation of triggers (from on-board programmable (?) oscillator/counter)
- Stand-alone generation of triggers (VME command)
- Output of VETO/BUSY to all ReadOut Boards via J2 backplane bus
- VME registers for STATUS, COMMAND, EXT. INPUTs ENABLEs
- Stand-alone X-tal clock oscillator (12.5 or 100 MHz?)
- Outputs of CLOCK to all ReadOut Boards via J2 backplane bus

5.2 Proposed implementation

This board performs two functions; distribution of the trigger to the readout boards and configuration control of the non-UK trigger logic.

This board provides a simple veto of further triggers until the data from each trigger has been read out. It takes in a single lemo connector on the front panel which provides the trigger signal from the external trigger logic. The trigger signal is sent via unused lines on the crate backplane to all the readout boards.

A trigger latches a veto which prevents and further triggers from being passed on, until cleared via VME. This allows the other parts of the whole system (HCAL, etc.) to be read out without retriggering the ECAL.

- simple 6U-VME slave, A24/32, D16
- 1x PLD or FPGA
- 1x Xtal clock oscillator
- +5V only for logic, −5 V needed for NIM signals.

5.3 Proposed state machine

1. Receive TRIGGER
2. If VETO/BUSY set, go to 6)
3. Assert VETO/BUSY and send to output(s)
4. Disable any further TRIGGER outputs
5. If no VETO/BUSY set, pass TRIGGER to back plane and front panel outputs
6. When any enabled EXTERNAL VETO/BUSY input(s) end, release internally-generated VETO/BUSY output(s) and go to 1)
7. When VETO/BUSY "CLEAR" is received from VME, release internally-generated VETO/BUSY output(s) and go to 1)

5.4 Inputs and outputs

- Front panel EXTERNAL CLOCK input (requires PLL ???)
- 4x front panel outputs of CLOCK
- 4x front panel outputs of TRIGGER
- 4x front panel outputs of VETO/BUSY
- EXTERNAL TRIGGER front panel inputs : 1x differential LVDS 1x TTL 1x NIM (?)
- Front panel push-button TEST TRIGGER
- Front panel push-button VETO/BUSY "CLEAR"
- Front panel push-button O/A RESE
- Recessed front panel push-button board reset.
- J2 back plane TRIGGER output 1x diff. LVDS
- J2 back plane CLOCK output 1x diff. LVDS
- J2 back plane VETO/BUSY output 1x diff. LVDS
- Front panel TRIGGER outputs 32x diff. LVDS
- Front panel VETO/BUSY outputs 4x diff. LVDS
- Front panel VETO/BUSY input 1x diff. LVDS
- Front panel EXT. CLOCK input 1x diff. LVDS
- Front panel EXT. CLOCK outputs 4x diff. LVDS

5.5 VME interface

VME Registers:

- Enables - EnIntTrig output - EnExtClk input - EnExtTrig input - EnExtVeto input

  V/Commands - V/Trigger - V/Veto Clear - V/OAReset
  Status - IntClkOn - ExtClkOn - ExtVetoOn
  Trigger Frequency - 6 bits (?)
  Interupts - on valid trigger.
  All using A24/D16 or A32/D16.
  Readout trigger source.

5.6 Cost

All the following prices include VAT and are in FY02/03 £. An estimated cost per trigger board, in addition to the £400 NRE costs, is therefore:

- FPGAs; total = £180.
- Other ICs; total = £250.
- Other hardware; total = £70.
- PCB fabrication and assembly; total = £700.

The total cost per trigger board is therefore approximately £1200.

5.7 Alternative implementation

A fallback approach which would be less flexible would be to have the trigger board as a simple interface to several pins on the readout board FPGA. A connector on the readout board would allow a small trigger board to be plugged into one of the readout boards using a short cable. This particular readout board would then handle the trigger logic within its FPGA. To identify itself as the trigger board, the cable would hold one of the pins high. The trigger board would then simply have the differential line drivers and receivers for the I/O.

The cable would need to include power, ground, the input trigger signal, the output trigger signals and the reset trigger logic signal.

6 Test board

6.1 Requirements

The given requirements are:

- Output diff. analog signals (voltage levels to be determined) from 16-bit DACs to simulate the output from VFE chips at up to a 1 MHz rate

  - Each VFE chip multiplexes 18 input channels onto 1 output line, - There is 6x VFE chips on each F/E wafer PCB - Each ReadOut Board will accept data from 6x F/E wafer PCBs

  =¿ Test Board requires a total of 6x6 diff. analog outputs to test a complete ReadOut Board

- Receive a single ANALOG CALIBRATION Voltage per each F/E wafer PCB, ie. 6x inputs in total

- Receive a single Sample and Hold signal per each F/E wafer PCB, ie. 6x inputs in total

- Receive a single up to 1 MHz multiplexing clock per each F/E wafer PCB, ie. 6x inputs in total

- Receive a single CAL. PULSE per each F/E wafer PCB, ie. 6x inputs in total

- Receive 6x Digital Calibration Select lines per each F/E wafer PCB, ie. 36x inputs in total

6.2 Proposed implementation

The biggest issue for testing the readout boards will be the input signals in the (assumed) absence of a final wafer PCB with VFE chips mounted. Hence, it would be useful to have a test board which connects directly to an input cable in place of a wafer PCB and generated sufficient signals to test the readout board. This would contain DACs and simple control so as to respond to the sample-and-hold and multiplex signals and put out voltages tothe analog signal lines. The levels could be controlled by the calibration select lines. It is effectively an “inverted” readout board.

A conceptual layout of the test board is shown in Fig. 6.

- Prototype to provide a sufficient outputs/inputs for a single F/E wafer PCB, possibly to be expanded to 6x F/E wafer PCBs later if really required

- 16-bit DACs to provide the diff. analog signal output (voltage levels to be determined) Requires 6x single DACs, or 2x 4-output DACs, or 1x 8-output DAC (CHECK IF/WHAT/WHEN AVAILABLE)

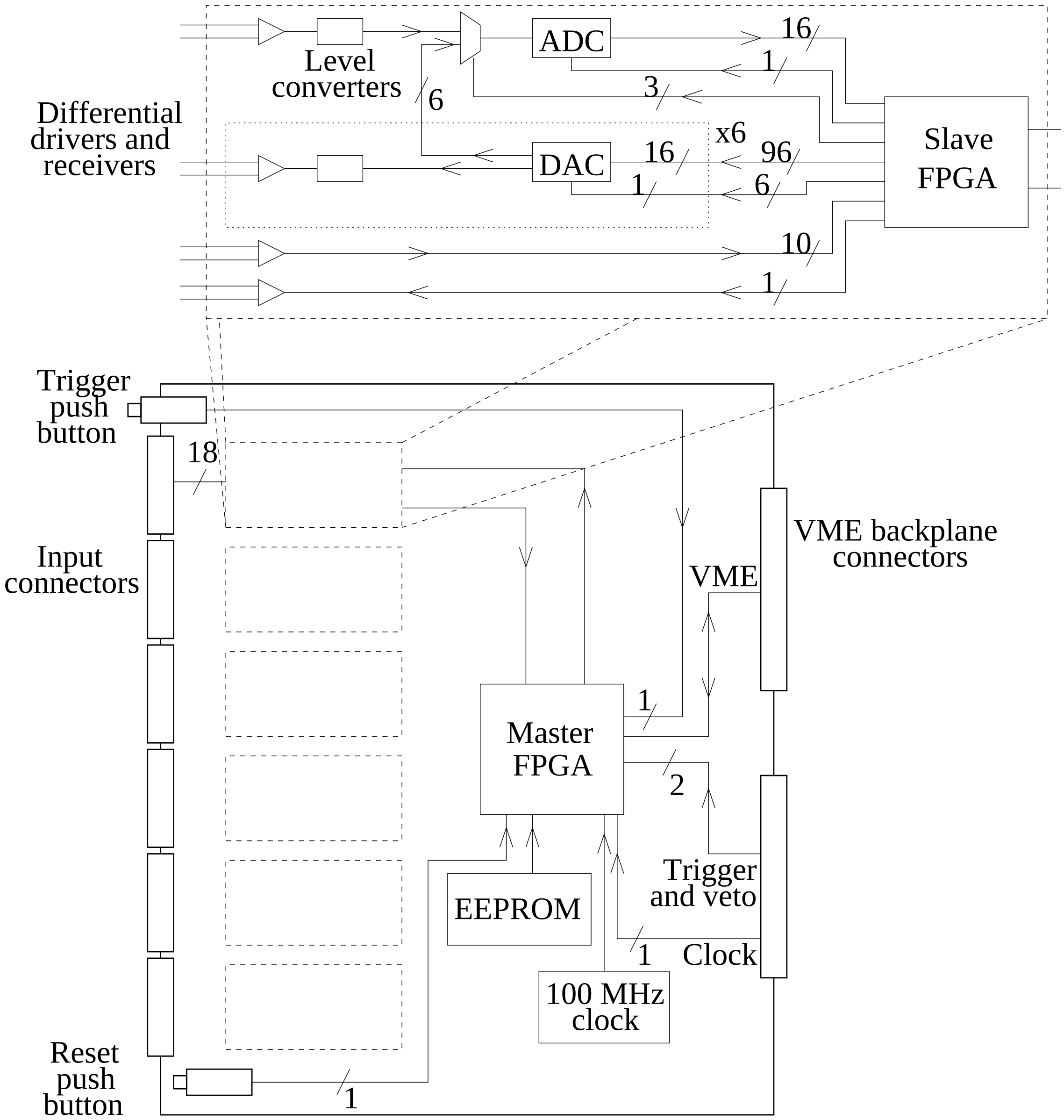

Figure 6: Conceptual layout of the test board. For clarity, the set of signals to only one of the six connectors is shown.

- Provide 3x sources of digital inputs for each DAC : a) - Stand-alone 16-bit RAMP GENERATOR (from received clock and counter ???) b) - 16-bit VME register c) - 16-bit RAM, pre-loadable from VME
- Use input signals (as listed above 2 - 6) to set/calibrate/operate DACs
- Simulate multiplexing of 18x VFE channels at 1MHz
- Requires 1x PLD or FPGA, interfaced to VME

6.3 Proposed state machine

6.4 Control and configuration data

Control and configuration data for each slave FPGA matches the event data for the readout board.

- 108 values for the DAC outputs.
- Number of multiplex clocks seen before generating the shift register output.

6.5 Status and event data

Status and event data match the configuration data for the readout board. All times are measured relative to the trigger time.

- Time of arrival of sample-and-hold, in units of 10 ns.
- Time of arrival of serial register input, in units of 80 ns.
- Time of arrival of first multiplex clock, in units of 80 ns.
- Time of arrival of second multiplex clock, in units of 80 ns.
- Etc.
- Time of arrival of calibration timing pulse, in units of 80 ns.
- Value of calibration selection.
- Value of calibration ADC.
- Number of multiplex clocks seen.

6.6 VME interface

The VME interface is almost identical to that of the readout board.

6.7 FPGA tasks

The master FPGA tasks are almost identical to those of the readout board.

The slave FPGAs need to handle receiving the timing sequence from the readout board and generate the shift register output signal.

6.8 Inputs and outputs

6.9 Alternative implementation

IS IT REALLY NECESSARY to do 6 cables at once??? A cheaper/easier solution is to provide only ONE F/E wafer PCB worth of electronics... SAME APPLIES in 2 - 6 BELOW ...

QUESTION : Would it be possible to use the above ONE F/E ——— - wafer PCB worth of signals and distribute them in parallel to all 6x ONE F/E wafer PCB input connectors ???

Has implications to the feedback/handshaking signals etc.

6.10 Cost

All the following prices include VAT and are in FY02/03 £.

Since the board is very similar to the readout board, most of the costs carry over directly, although the quantities of each component are different.

A estimated cost per test board, in addition to the £800 NRE costs, is therefore:

- ADCs; £30 per ADC $\times$ 6 ADCs = £180.
- FPGA; £26 per FPGA $\times$ 7 FPGAs = £182.
- DACs; £33 per DAC $\times$ 36 DACs = £1188.
- Other ICs; total = £300.
- Other hardware; total = £200.
- PCB fabrication and assembly; total = £850.

The total cost of the test board is therefore approximately £2900.

7 Other issues

7.1 Connectors and cables

The connectors and cables used between the wafer PCBs and the readout electronics depend heavily on external factors, namely the wafer PCBs and the trigger.

The wafer PCBs have a very restricted space for the connector width of only 4.5mm and while in principle different connectors are possible at both ends, this would complicate the test board. The choice of the connector has some impact on the cable used also. Making 100 cables (90 plus 10 spares) by hand which require 36 solder joints at each end would be tedious and error prone.

The trigger has an influence on the cable also. There needs to be a “long” cable run at some point in the readout system so that the data acquisition PC can be operated outside of any radiation area which has restricted access during the beam test. This is assumed to require at least 30 metres of cable. If this were the wafer PCB to readout board cables, then they would presumably need much better sheilding to preserve the analog signal precision and possibly better drivers at each end. The trigger may not allow this option if the $\sim$ 100 ns delay of such cables made the sample-and-hold time at the VFE chips too late. Having a long cable between the PCI card and VME interface, or between the data acquisition PC and a simple terminal for an operator, would reduce the requirements for the now short ($\sim$ 1 metre) cables to the wafer PCBs.

7.2 Event numbers

The main aim of the project is to get precise data on hadronic interactions to compare with simulation. The precision achievable obviously depends on the number of events taken. If it is assumed that a 5% accuracy is needed for a 3σ tail (0.13% of the total) of a distribution, then 400 events are needed in this region. This corresponds to a total of 3×10^5 events.

This number of events is needed for each of several experimental configurations. The quantities varying between the setups are:

- The particle type; at least electrons and pions will be needed, and possibly muons also. Assume 2 variations.
- The beam energy; energies between 1 and 10 GeV are needed, ideally data with 3 or 4 different energies would be taken. Assume 4 variations.
- The HCAL; data with both the tile and digital HCAL options are needed. Assume 2 variations.
- Entrance angle; normal and 45° incidence angles are wanted. Assume 2 variations.
- Preshower; material will be included in front of the ECAL for some data. Assume 2 variations.

Although not all combinations are particularly meaningful, the simple calculation of doing all would give a total of $2 \times 4 \times 2 \times 2 \times 2 = 64$ variations. This would imply a total data sample of around 2×10^7 events.

7.3 Data rates and volumes

The ECAL data will be around 19 kBytes per event. The tile HCAL option has up to 1200 channels, each reading 16 bits, and so corresponds to around 2 kBytes. The digital HCAL option will have 10k channels in each of up to 38 layers, with each channel corresponding to one bit. This gives a total of around 4×10^5 bits or 50 kBytes without any zero suppression. Some beam monitoring and trigger data need to be included also.

Assuming the event sizes are between 30 and 80 kBytes, then the VME backplane speed of around 25 MBytes/s will limit the event rate to between 300 and 1000 Hz maximum. It seems likely than 100 Hz is achievable. At this rate, the time to acquire the 300k events needed for each experimental configuration is 3000 s, or around 1 hour. Even allowing for significant setup time for each configuration, it seems feasible to complete the beam test within a couple of months.

With an average data size of 60 kBytes per event, then the total data sample of 2×10^7 events will be 1.2 TBytes. Calibration and cosmics runs are assumed to be comparatively small and have not been included in this eastimate.

To avoid problems with large file sizes (> 2 GBytes for standard Linux), then the number of events per file (assumed to be a run) would need to be restricted to around 30k events, which would imply a run would last around 300 s or 5 minutes. A single configuration sample would be 10 runs and the total sample would be around 600 runs.

8 Total costs, timescale, effort

8.1 Costs

We assume that we will build 2 prototypes of the readout boards and for production, we need 15 readout boards plus 3 spares. The trigger board will need at most 1 prototype board and, for production, 1 board plus 1 spare. The test board will be produced during prototyping and no production of this is needed.

In addition to the purpose built boards, the system also needs commercially available infrastructure, namely, a PCI/VME interface card, a VME extender, a high-end PC, some disk storage and VME crates and power supplies.

All the following prices include VAT. A VME-PCI8026 PCI/VME interface card set, including a 2m cable, is quoted by National Instruments at £3889. A VXI-MXI-2 extender board, including cable, is quoted at the same location at £2755. A dual Pentium-IV, 2 GHz, 2 Gbytes memory PC, with screen and keyboard, is quoted by Compusys at £3680. For disk, a 1.4 Tbytes array spread over 12 IDE disks with RAID 5 redundancy and a SCSI interface, recently bought by the UCL group, was £8k. CERN-specification, Wes V429, 6U VME crates, including power supplies, are quoted at £4700.

Therefore, an estimated costing of the readout system is:

- Non-recurring design costs; for all electronics = £2k.
- Readout boards; £2800 per board × 22 boards = £62k.
- Trigger board (estimated); £1200 per board × 3 boards = £4k.
- Test board; £2900 per board = £3k.
- Cables (estimated); £30 per cable × 100 cables = £3k.
- PC and disk; £4k for the PC, £8k for 1.4 Tbytes of disk = £12k.
- VME interfaces; £4k for PCI-VME interface, £3k for VME extender = £7k.
- 6U VME crate and power supplies; £5k per crate × 2 crates = £10k.

All values given are in FY02/03 prices and include VAT, so the total cost of the equipment for the project is therefore FY02/03 £103k.

8.2 Timescale

Table 1 shows the milestones for the readout electronics. The system needs to be ready for a

Milestone	Date of completion
Readout electronics specification completed	End June 2002
Prototype readout board design completed	End December 2002
Test readout board design completed	End February 2003
Prototype readout board layout and fabrication completed	End February 2003
Test board layout and fabrication completed	End April 2003
Prototype readout board testing completed	End June 2003
Production readout board design completed	End July 2003
Trigger board design completed	End August 2003
Production readout board layout and fabrication completed	End September 2003
Trigger board layout and fabrication completed	End October 2003
Production readout board testing completed	End December 2003
Trigger board testing completed	End December 2003

Table 1: Milestones for the readout electronics.

beam test in early 2004. It therefore needs to be completed by the end of 2003. Fabrication, testing and data acquisition software development of the full system is likely to require around 6 months, which sets the end of the prototype phase to be mid-2003. Therefore, the time from approval to mid-2002 will be used to complete the specification of the electronics. The rest of 2002 will be used for designing the boards. Prototype fabrication will take place early in 2003 and prototype testing will take the rest of the first half of 2003.

Hence, prototype costs will be incurred in FY02/03 while production will occur in FY03/04. The prototype costs will be for some of the infrastructure (PC, the PCI-VME interface, one VME crate and a few cables), two readout boards and the test board, giving a total of £23k in FY02/03. The remaining infrastructure and board production costs, totalling FY02/03 £80k, will all be incurred in FY03/04.

8.3 Effort

The readout board will require around 18 months of engineering effort in total; 12 months for the board design and 6 for the FPGA firmware. We estimate that 12 months of engineering effort will be required for the design of the test and trigger boards. In addition, 1 month will be needed for layout and fabrication of each of the prototype readout board, the production readout board, the test board and the trigger board. This is a total of 34 months.

We propose to provide 18 months for the readout board design effort, including the FPGA design, and the test and trigger board design effort from University staff. The rest of the effort would then be provided by RAL TD, with 12 months needed for the rest of the board designs and 4 months for the layout and fabrication of all the boards. This effort will be divided approximately equally between FY02/03 and FY03/04, which are the two FYs in which the system is being produced.