Specification of the readout electronics for the CALICE beam test

C. M. Hawkes, S. J. Hillier, R. J. Staley and N. K. Watson
School of Physics and Astronomy,
University of Birmingham,
Birmingham, B15 2TT, UK.

D. R. Ward and M. A. Thomson
The Cavendish Laboratory,
Cambridge University,
Cambridge CB3 0HE, UK.

P. D. Dauncey*
Department of Physics, Blackett Laboratory,
Imperial College of Science, Technology and Medicine,
Prince Consort Road,
London, SW7 2BW, UK.

J. M. Butterworth, D. J. Miller, M. Postranecky and M. Warren
Department of Physics and Astronomy,
University College London,
Gower Street,
London WC1E 6BT, UK.

R. J. Barlow, I. P. Duerdoth, N. M. Malden, D. Mercer and R. J. Thompson
The Department of Physics and Astronomy,
The University of Manchester,
Manchester M13 9PL, UK.

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Abstract

The specifications for the readout electronics to be used in the beam test for the CALICE collaboration are presented.

NOTE: EVERYTHING IN THIS DESCRIPTION IS PRELIMINARY AND IS OPEN TO CHANGE.

*Contact person; email P.Dauncey@ic.ac.uk

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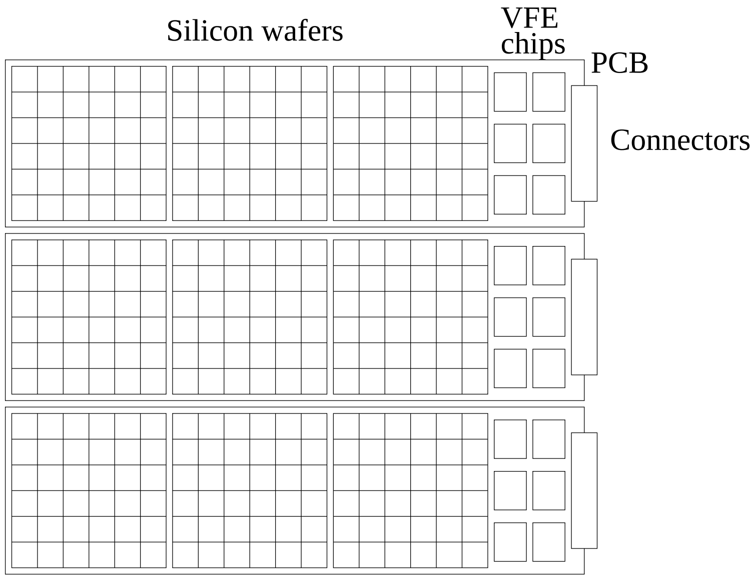

Figure 1: Schematic of one layer of the silicon wafers.

1 Introduction

The CALICE collaboration plans to test a prototype tungsten-silicon electromagnetic calorimeter (ECAL) with a beam in early 2004. The prototype will have around 10000 channels and the UK hopes to provide the readout electronics and data aquisition for this experiment. There will also be a hadronic calorimeter (HCAL) prototype although the UK is not involved in this side of the project. The eventual aim of this study is to design a calorimeter for the TESLA linear collider.

2 Overview of the prototype

The prototype calorimeter will consist of 30 layers of silicon diodes. Each layer comprises a 3×3 array of silicon diode wafers, each containing a 6×6 array of diodes. Each diode needs to be read out and so corresponds to a channel. Hence, each wafer contains 36 channels, each layer contains $36 \times 9 = 324$ channels and the whole prototype is $324 \times 30 = 9720$ channels.

The three silicon wafers in a row in each layer will be mounted on PCB's which route the diode signals (without amplification) to the very front end (VFE) chips which provide amplification and shaping. Each layer therefore consists of three such PCB's which are mechanically connected but electrically independent. The schematic structure of one layer is shown in Fig. 1. The VFE chip will handle 18 channels and will provide a sample-and-hold on an external trigger for each channel. It will have a single gain and will multiplex the signals from the 18 channels onto a single output line at up to 1 MHz. The VFE chip will also accept a calibration signal which is used to inject a pulse at the chip input.

The diodes, VFE chips, wafer PCB's and their power supplies, as well as the trigger and its logic, will be provide by non-UK groups, while the UK will need to provide all the readout electronics downstream and the DAQ system to read it out. All signals from each PCB are assumed to be routed through a single connector. This will provide the well-defined interface between the two parts of the electronics. The UK will provide any cables needed from this connector.

2.1 UK readout system requirements

The requirements for the prototype UK readout electronics are as follows:

- It must digitise and read out all 9720 channels. These are grouped into $6 \times 18 = 108$ channels on each PCB, with 90 PCB's in total.
- With the VFE chips having a single gain, then at least 12 bit, and preferably at least 14 bit, ADC's are needed.
- It must supply the sample-and-hold timing signal to each PCB. The sample time must be adjustable to coincide with the shaped pulse peak, which occurs ~ 150 ns after the charge deposit in the diodes. This could be done in the external (non-UK) trigger logic but it would be useful for this to be software configurable within the UK electronics.
- It must supply the ~ 1 MHz multiplex clocking signal to each PCB to generate the analog signals on each VFE chip output line.
- It must supply an adjustable calibration voltage, timing pulse and channel selection signals. The voltage should be adjustable to 16 bits. The timing pulse also needs to be adjustable relative to the subsequent sample-and-hold signal. The channel selection determines to which channels the calibration pulse is applied; $2^6 = 64$ different combinations should be sufficient.
- It must be consistent with the readout of the other parts of the beam test system, namely any beam monitoring detectors, the trigger system and the HCAL detector. Note, these systems are not yet defined. Also, since the development of the readout for the HCAL part of the beam test is significantly undermanned, it would be useful if the UK electronics could be made adaptable and so be used for the HCAL also. This would only be considered if the extra engineering effort and expense required is minor.

2.2 PCB connector interface

The UK readout electronics is assumed to have an independent ground from the wafer PCB's. Hence, all signals on the PCB connector which provide the interface to the UK readout are assumed to be differential. All digital signals as assumed to be LVDS. The signals on the connector are assumed to be as follows:

- Digital sample-and-hold timing signal. A single signal on the connector is distributed on the PCB to all 6 VFE chips.
- Digital multiplex timing signal. Again a single signal is distributed to all VFE chips so they are read out in parallel.
- Analog multiplexed signal output. There must be six lines, one from each VFE chip. The voltage range needs to be specified.
- Analog calibration voltage. A single voltage is applied to several channels as determined by the calibration selection logic on the PCB. The voltage range still needs to be specified.
- Digital calibration pulse timing signal. Again, a single signal is distributed on the PCB as required.
- Digital calibration selection. Six lines are needed for up to 64 different combinations.

The total number of signals is then $1 + 1 + 6 + 1 + 1 + 6 = 16$, of which 7 are analog and 9 digital, requiring a 32-pin connector on each PCB.

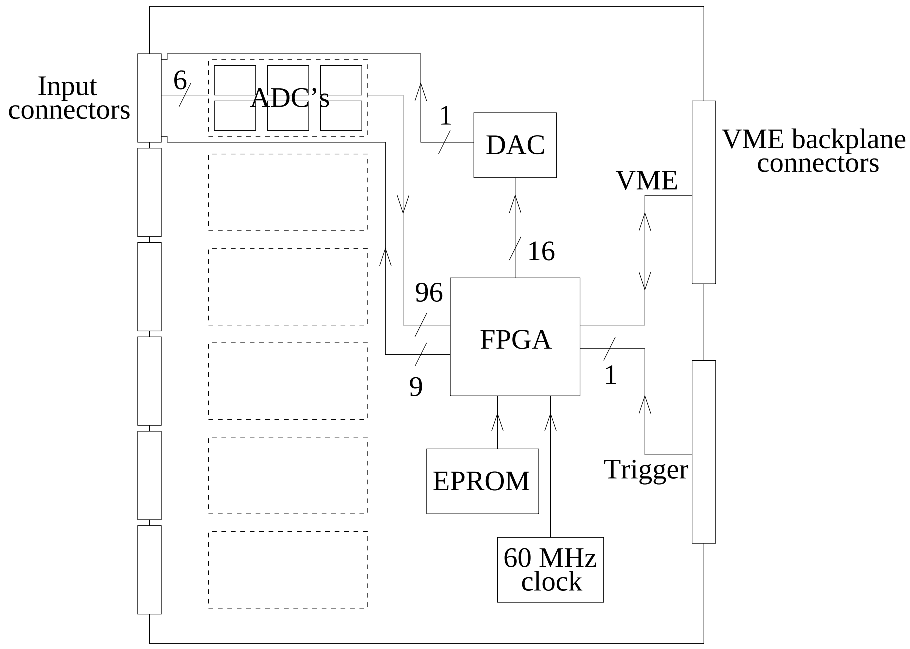

Figure 2: Conceptual layout of the readout board. For clarity, the set of signals to only one of the six connectors is shown.

3 Overview of proposed readout system

The following sections describe the proposed UK readout electronics which satisfies the above requirements. Some issues are unresolved and these are listed in a later section.

The proposed system has the cables from the wafer PCB's connecting directly to 6U VME boards, with all the necessary readout electronics on these boards. The system would run triggered and read out each event before allowing the next trigger to occur. This would be controlled by a single VME trigger handling board which distributes the trigger across the backplane. No data reduction is done in hardware, so all 9720 channels are read out for each trigger.

The basic unit of the readout is based on the 90 wafer PCB's. These each hold 108 channels which are multiplexed onto 6 lines. It would be convenient to contain the whole system in a single standard VME crate of 21 slots. Assuming a PCI/VME interface card and a single width trigger card, this leaves 19 slots for the readout boards. The obvious division is then 15 readout boards, each handling the signals from 6 wafer PCB's, equivalent to 2 of the 30 layers of the calorimeter.

4 Readout boards

A conceptual layout of the readout board is shown in Fig. 2. Each readout board must digitise the signals from 6 wafer PCB's, which is therefore $6 \times 6 = 36$ multiplexed VFE chip outputs. It will therefore contain 36 ADC's. Given that the total number of ADC's in the whole system is now $36 \times 15 = 540$, then the price per ADC is not a major cost driver and 16-bit ADC's can be used. The board is controlled by an FPGA and has its own $\sim$ 60 MHz clock. This allows all timings to be determined to $\sim$ 16 ns divisions. The board takes in 6 twisted-pair ribbon cables from the wafer PCB's through its front panel. The trigger signal is taken from unused lines on the crate backplane. The calibration voltage is set by a 16-bit DAC.

4.1 Standard readout sequence

The readout sequence is as follows. A trigger signal is detected on the backplane. The FPGA waits for a configurable delay before issuing a sample-and-hold timing signal synchronously to all 6 PCB's. After another configurable delay, 18 multiplex signals are sent, with a configurable period to the first PCB. The corresponding ADC's are sampled with a configurable phase offset from the multiplex clock. The data from these ADC's are stored in the FPGA. This sequence is then repeated for the remaining 5 PCB's. When all data have been stored in the FPGA, then VME readout is enabled. Following readout, the board waits for the next trigger. If a trigger arrives during the above sequence, it is immediately restarted.

At any given sample, 6 ADC's are each outputting a 16-bit digitised sample, so the data volume into the FPGA is $16 \times 6 = 96$ bits at 1 MHz.

Each FPGA receives data from 648 channels, which is 648×2 bytes $= 1296$ bytes and so should be able to be stored within the FPGA without needing an external memory component. Each event is 9720 channels $\times$ 2 bytes $=$ 19440 bytes or 19 kbytes. This will take at least 1 ms to read over VME and so will limit the event rate to a maximum of around 1 kHz, although a realistic estimate is probably more like a few hundred Hz.

4.2 Calibration sequence

The calibration sequence is similar to the above. However, on detection of a trigger, then after a configurable delay, a calibration timing pulse is sent. After a further delay, the trigger is sent and the subsequent sequence is identical to the above. The calibration voltage settings and selection lines are assumed to have been configured before the start of the calibration sequence.

4.3 Configuration data

The configurable values which need to be loaded onto the board before readout are as follows:

- Sample-and-hold timing pulse delay, in units of the ~ 16 ns clock period. This allows the sample to be taken at the shaped pulse peak.
- Delay to start of multiplexing sequence, in units of the ~ 16 ns clock period. The time needed for this is unknown and may not need to be non-zero.
- Period of multiplexing sequence, in units of the ~ 16 ns clock period. Nominally, this is around 60 to get a 1 MHz multiplex speed.
- Phase offset of ADC sampling w.r.t. multiplex clock, in units of the ~ 16 ns clock period. This allows the ADC sample time to occur at a fixed offset from the multiplex switch time, so avoiding transients.
- Delay between PCB reads, in units of the ~ 16 ns clock period.
- Calibration enable flag. Determines if a readout or calibration sequence should occur.
- Calibration selection settings. Separate values should be allowed for each PCB.
- Calibration DAC setting. The 16 bit value to set the DAC.
- Calibration timing pulse delay, in units of the ~ 16 ns clock period.

As all signals are rounded to a 16 ns period, then the trigger time to sample time will jitter by up to this amount. This gives a sample which will not be exactly at the peak. The shape at the peak can be approximated by $1 - x^2/2$, where for a standard CR-RC shape, $x = \delta t/\tau$ with

δt the time from the peak and $\tau = 150$ ns for the VFE chips being used. Hence, for t off by a maximum of $\delta t = 16$ ns, then the reduction from the peak is approximately 0.006, an offset of less than a percent.

4.4 VME interface

The VME interface needs to allow read and write of all configuration data. It also needs a read-only interface for all the digitised data. It would be useful for there to also be a read-only board identification, including a unique serial number. A software-driven board reset, including a reload of the FPGA firmware, would also be useful.

It would be useful for all VME data to be of the same type, specifically unsigned 16-bit words.

4.5 Power consumption

This needs to be evaluated.

4.6 Testability

The biggest issue for testing the readout boards will be the input signals in the (assumed) absence of a final wafer PCB with VFE chips mounted. Hence, it would be useful to have a test board which connects directly to an input cable in place of a wafer PCB and generated sufficient signals to test the readout board. This would contain a DAC and simple control so as to respond to the sample-and-hold and multiplex signals and put out voltages to the analog signal lines. The levels could be controlled by the calibration select lines. The details of such a board need to be defined when the PCB connector interface is fully specified.

4.7 Cost

A very rough costing of the readout board is:

- ADC's; £20 per ADC $\times$ 36 ADC's = £720.
- FPGA; £100 per FPGA = £100.
- DAC; £30 per DAC = £30.
- PCB manufacturing, mounting and minor components; £1000 per board = £1000.

The total cost per readout board is therefore approximately £1850.

5 Trigger handling board

This board provides a simple veto of further triggers until the data from each trigger has been read out. It takes in a single lemo connector on the front panel which provides the trigger signal from the external trigger logic. The trigger signal is sent via unused lines on the crate backplane to all the readout boards.

A trigger latches a veto which prevents and further triggers from being passed on, until cleared via VME. This allows the other parts of the whole system (HCAL, etc.) to be read out without retriggering the ECAL.

5.1 VME interface

5.2 Cost

A very rough costing of the trigger board is:

- PCB manufacturing, mounting and minor components; £1000 per board = £1000.

The total cost per trigger board is therefore approximately £1000.

6 Total costs, timescale, effort

6.1 Costs

We assume that we will build 2 prototypes of the readout boards and for production, we need 15 readout boards plus 3 spares. The trigger board will need at most 1 prototype board and, for production, 1 board plus 1 spare. The PCB connector test board will be produced during prototyping and no production of this is needed. In addition to the purpose built boards, the system also needs commercially available infrastructure, namely, a PCI/VME interface card, a high-end PC and some storage disk. Therefore, a very rough costing of the readout system is:

- Readout boards; £1850 per board $\times$ 20 boards = £37k.
- Trigger board; £1000 per board $\times$ 3 boards = £3k.
- Test board; £2000 per board = £2k.
- Cables; £10 per cable $\times$ 90 cables = £1k.
- PC and VME interface; £8k total = £8k.
- Disk; £1000 per 100 GByte disk $\times$ 10 disks = £10k.
- 6U VME crate and power supplies; £10k total = £10k.

The total cost of the project is therefore approximately £71k.

6.2 Timescale

The system needs to be ready for a beam test in early 2004. It therefore needs to be completed by at latest end 2003. Production, testing and data acquisition software development of the full system is likely to require around 6 months, which sets the end of the prototype phase to be mid 2003. Therefore, from the time of approval to the end of 2002 will be used for designing the boards. Prototype fabrication will take place early in 2003 and prototype testing will take the rest of the first half of 2003.

Hence, prototype costs will be incurred in FY02/03 while production will occur in FY03/04. The prototype costs will be for the most of the infrastructure (PC, VME interface, crate, one disk and a few cables) and some of each of the boards, giving a total of £26k in FY02/03. The remaining disk, cable and board production costs, totalling £45k, will all be incurred in FY03/04.

6.3 Effort

The two boards will take a full time equivalent engineer for the time of approval up until the system is complete, i.e. end 2003. This is likely to be around 18 months, half in FY02/03 and half in FY03/04. This gives a total engineering requirement of 0.75SY for FY02/03 and 0.75SY for FY03/04, making a total of 1.5SY, with cost equivalent roughly £120k.

7 Remaining issues

- The PCB connector specifications need to be finalised. In particular, the voltage ranges for the analog voltages need to be specified.
- Can 6 connectors fit onto the front panel of one 6U single width readout board? If not, should the boards be 9U (with a consequent increase in cost)? Should be use 9U and fit more channels onto each board anyway, e.g. 3 ECAl layers per readout board, giving 10 in total? This would give more space for HCAL, etc. readout boards.
- Do the readout boards need to be synchronised? The above proposal has each with its own 60 MHz clock, so they are all independently clocked.
- Should PCB's be read in series or should ADC's be multiplexed into FPGA? The delay of reading the PCB's in series is small compared to the time to read the data over VME.
- Should FPGA firmware be downloadable over VME and/or from the EPROM/flash memory?
- How soon will the other parts of the overall beam test system be defined? How restricted are we until then?
- Is a separate trigger board really required? For just the ECAL, it would not be necessary, but it retains flexibility for the other parts of the system.
- What are the overheads of putting other VME crates for the rest of the system into the DAQ? This makes the trigger handling more complicated.
- How much engineering effort will be required from RAL?
- Is the readout board sufficiently complex that it will require layout at the RAL TD drawing office?