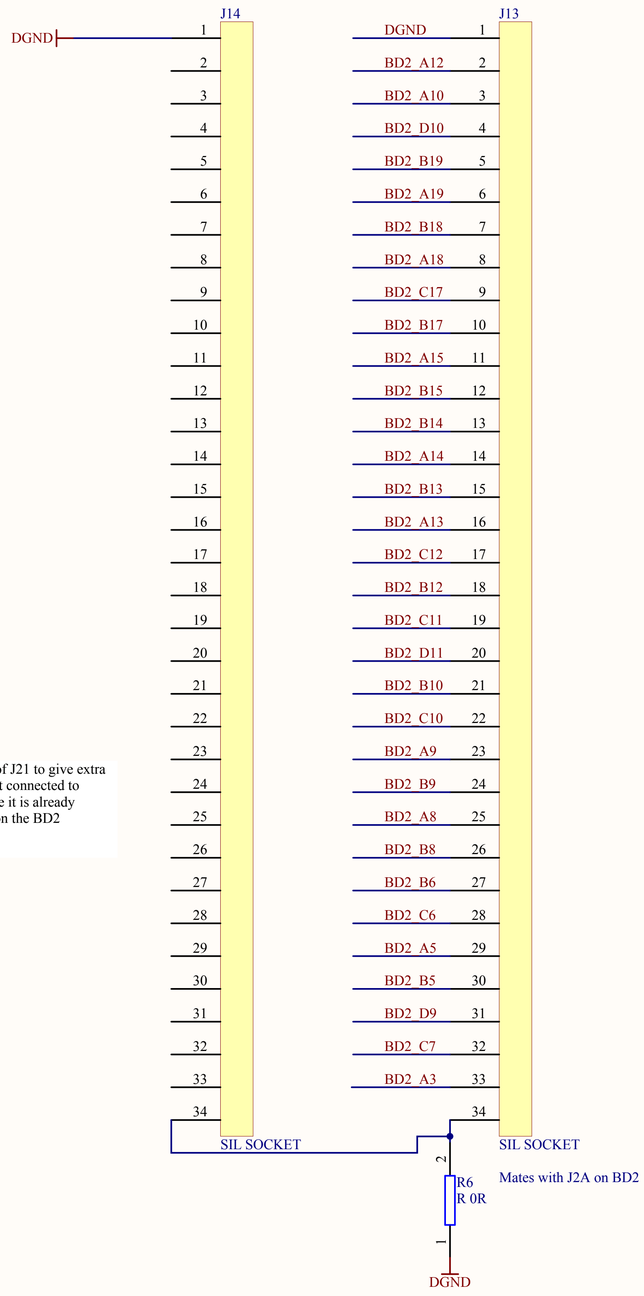
This goes just inside J22 pins 33-34 for improved location

THE HDMI BOARD SPANS FROM THE LHS OF J2 ON THE BROADDOWN2 TO J11. THIS IS A DISTANCE OF 1.6 INCHES OR 40.32MM BETWEEN HOLE CENTRES



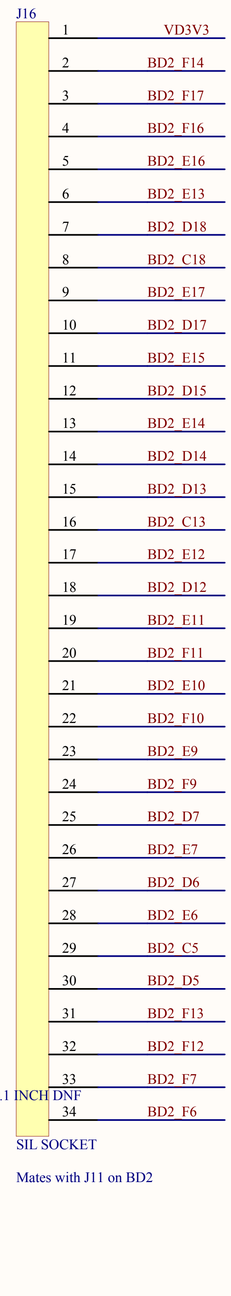
The following BD2 IOs are available here but are also used on the Serial card (MU2):

B19 (USER_LED1)
A19 (USER_LED2)
B18 (USER_LED3)
A18 (USER_LED4)

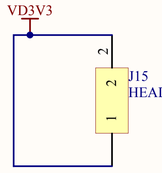
F17 (USB_CNTL_1)
F16 (USB_CNTL_0)
E16 (USB_DATA_0)
C12 (125MHZ)
E13 (USB_DATA_1)
F13 (USB_DATA_2)
F12 (USB_DATA_3)

D6(USB_DATA_7)
E6 (USB_DATA_6)
C5 (USB_DATA_5)
D5 (USB_DATA_4)

This header goes to the right of J21 to give extra mechanical strength, but is not connected to anything on this board because it is already connected pin-for-pin to J21 on the BD2



F14 IS ONLY AVAILABLE ON BD2 1000 AND ABOVE



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Size A3	Number *	Revision *
Date: 02/06/2008 *		Sheet of *
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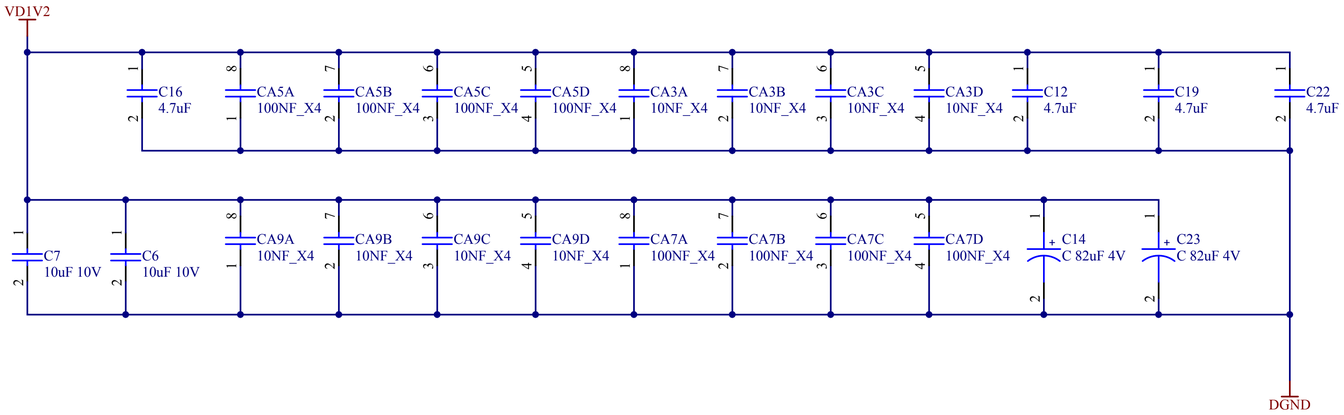

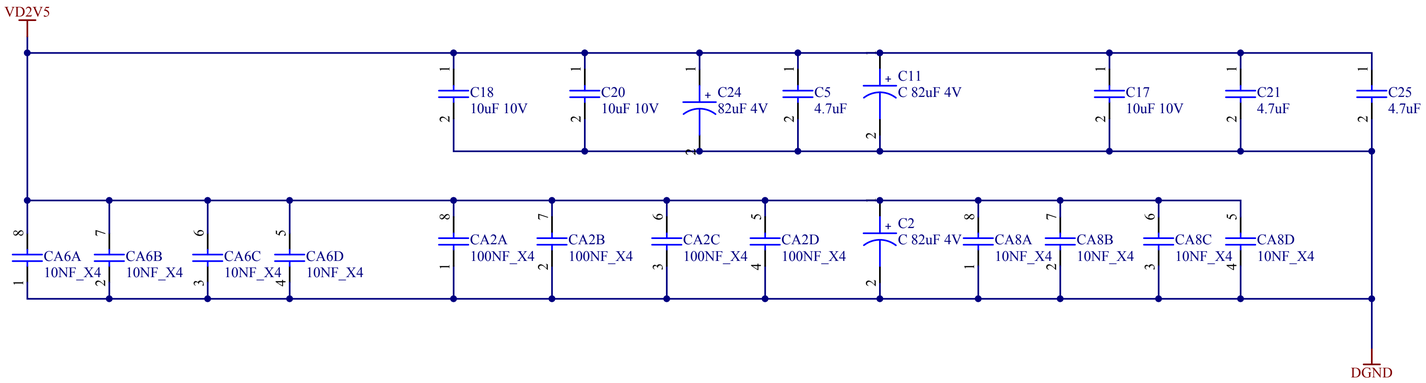

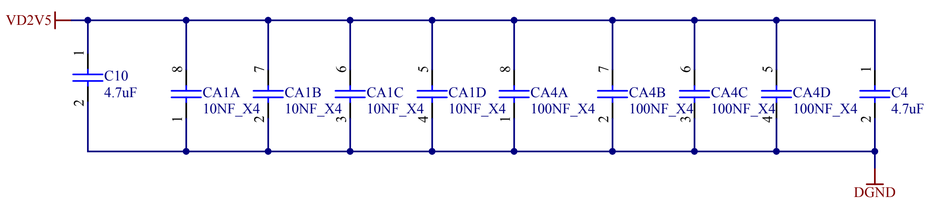

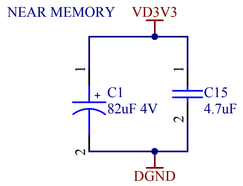

Project Title: Manchester University 1		Sheet Size: A3
Sheet Title: DECOUPLING.SCHDOC		Revision: 1.0
Date: 02/06/2008	Sheet: 1 of 9	
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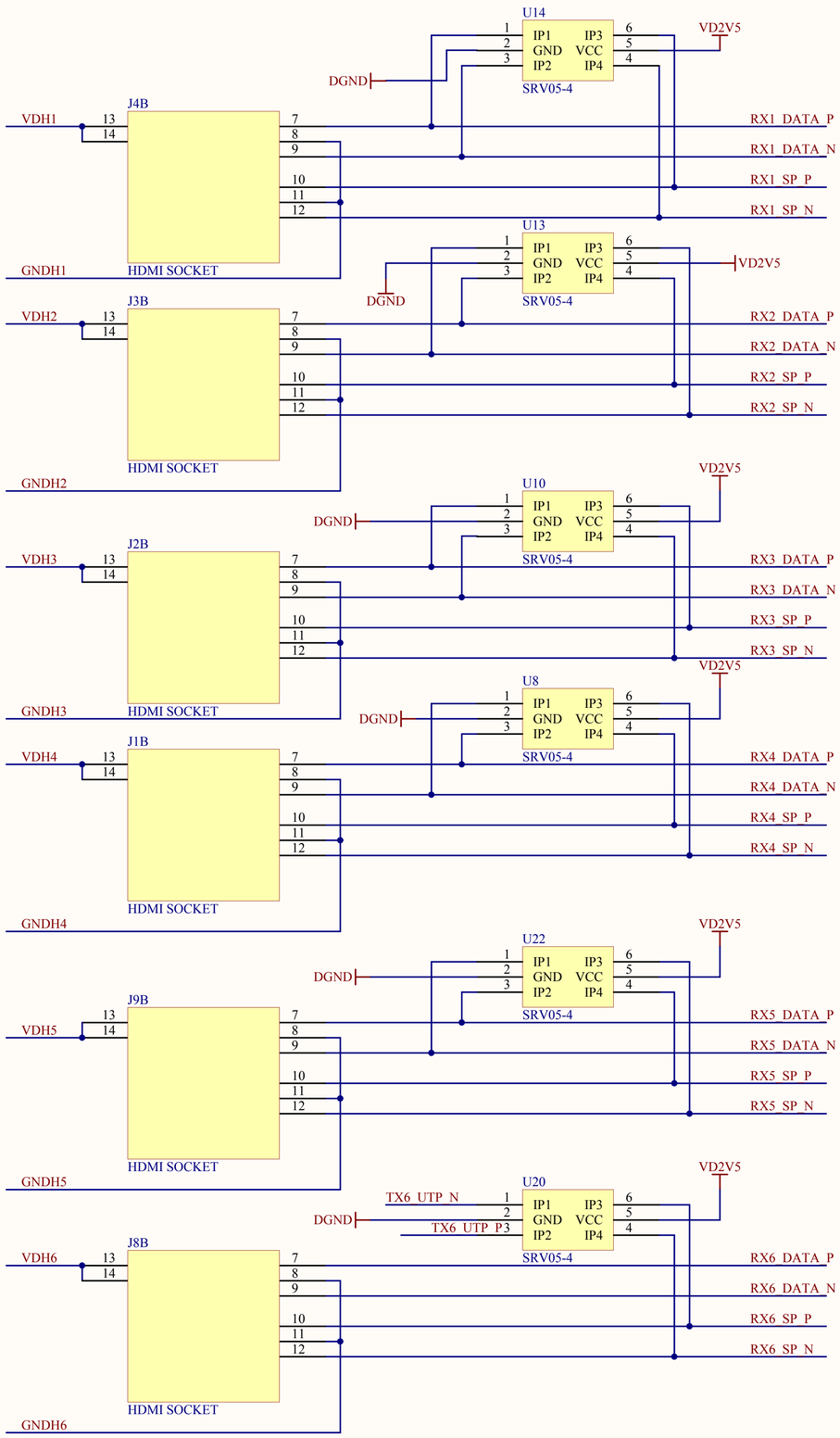
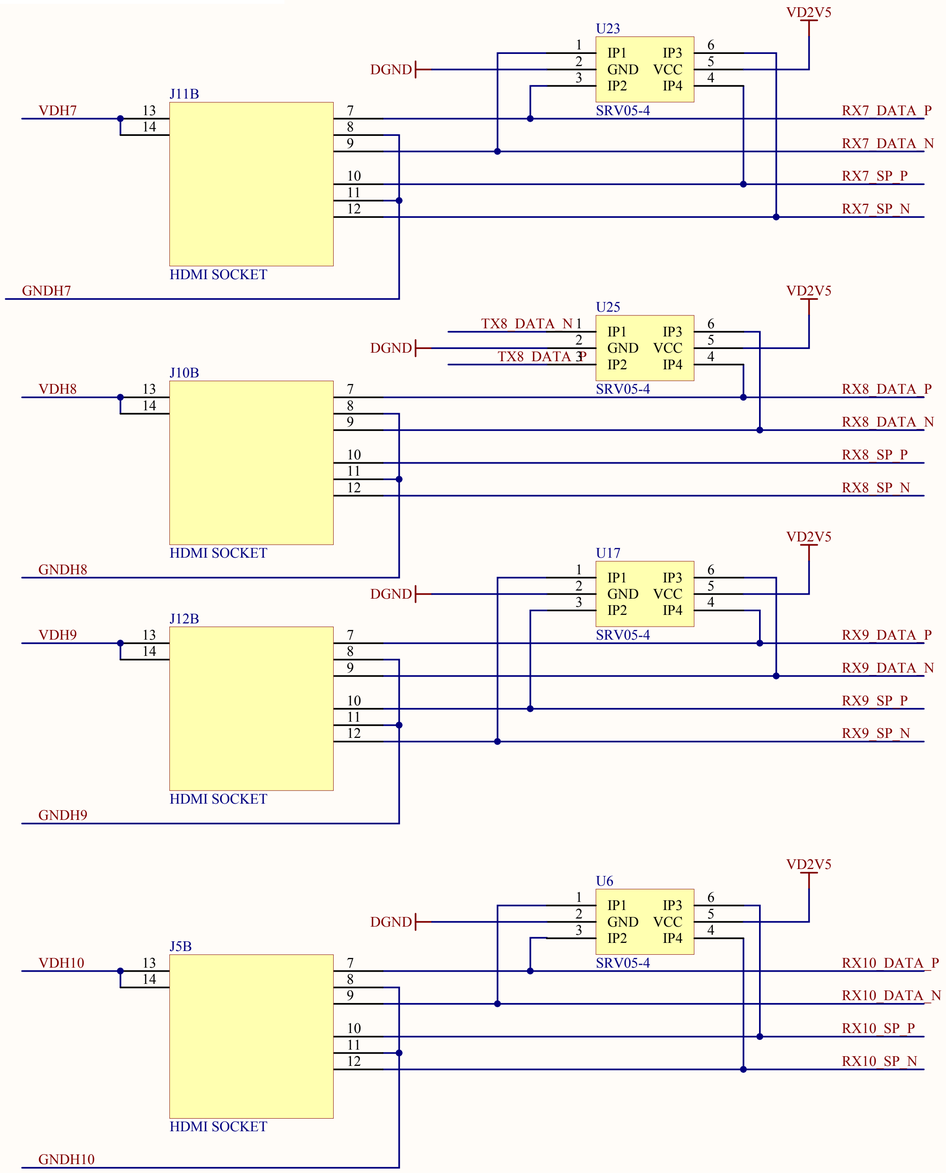
REMEMBER THE HDMI SOCKETS HAVE TO BE AT LEAST 22MM APART OTHERWISE THEY WON'T BE ABLE TO PLUG THE CABLES IN.





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Size: A3	Number: HDMI INPUTS	Revision: 1.0
Date: 02/06/2008	Sheet 3 of 9	
File: E:\PROJECT_ARCHIVES\..\HDMI_INPUTS.SchDoc	Drawn By: BC	

BANK4

U12E

IO	U16	BD2_E14
IO	U17	BD2_D14
IO	W13	
IO	W14	
IO	AB13	BD2_F12
IO/VREF_4	V18	BD2_C13
IO/VREF_4	Y16	BD2_F9
IO/VREF_4	AA20	VRP4
IO_L01N_4/VRP_4	AB20	VRN4
IO_L01P_4/VRN_4	AA19	
XC3S1000/IO_L05N_4	AB19	
XC3S1000/IO_L05P_4	W18	BD2_E12
IO_L06N_4/VREF_4	Y18	BD2_D12
IO_L06P_4	AA18	BD2_F10
IO_L09N_4	AB18	BD2_E9
IO_L09P_4	V17	BD2_D13
IO_L10N_4	W17	BD2_E11
IO_L10P_4	Y17	BD2_E10
IO_L15N_4	AA17	BD2_E6
IO_L15P_4	V16	BD2_D7
IO_L16N_4	W16	BD2_F13
IO_L16P_4	AA16	
XC3S1000/IO_L19N_4	AB16	
XC3S1000/IO_L19P_4	V15	
XC3S1000/L22N_4/VREF4	W15	
XC3S1000/IO_L22P_4	AA15	BD2_E7
IO_L24N_4	AB15	BD2_D6
IO_L24P_4	U14	
IO_L25N_4	V14	
IO_L25P_4	AA14	SERIAL_DIN
IO_L27N_4/DIN/D0	AB14	BD2_C5
IO_L27P_4/D1	U13	
IO_L28N_4	V13	
IO_L28P_4	Y13	
IO_L29N_4	AA13	BD2_D5
IO_L29P_4	U12	
IO_L30N_4/D2	V12	
IO_L30P_4/D3	W12	INIT_B
IO_L31N_4/INIT_B	Y12	
IO_L31P_4/DOUT/BUSY	AA12	BD2_F7
IO_L32N_4/GCLK1	AB12	BD2_F6
IO_L32P_4/GCLK0	T12	
VCCO_4	T13	
VCCO_4	T14	
VCCO_4	U15	
VCCO_4	Y15	
VCCO_4		

SPARTAN3_FG456

VD2V5

BANK5

U12F

IO	U7	
XC3S1000/IO	U9	
IO	U10	
IO	U11	
IO	V7	BD2_C10
IO	V10	
IO	AB11	BD2_A3
IO/VREF_5	U6	
IO/VREF_5	Y4	RX4_SP_N
IO_L01N_5/RDWR_B	AA3	RX4_SP_P
IO_L01P_5/CS_B	AB4	BD2_B13
IO_L06N_5	AA4	BD2_A14
IO_L06P_5	Y5	TX4_UTP_N
IO_L09N_5	W5	TX4_UTP_P
IO_L09P_5	AB5	VRP5
IO_L10N_5/VRP_5	AA5	VRN5
IO_L10P_5/VRN_5	W6	BD2_C12
IO_L15N_5	V6	BD2_A13
IO_L15P_5	AA6	BD2_B12
IO_L16N_5	Y6	BD2_C11
IO_L16P_5	Y7	
XC3S1000/IO_L19N_5	W7	
XC3S1000/L19P_5/VREF5	AB7	
XC3S1000/IO_L22N_5	AA7	
XC3S1000/IO_L22P	W8	BD2_D11
IO_L24N_5	V8	BD2_B10
IO_L24P_5	AB8	BD2_A9
IO_L25N_5	AA8	BD2_B9
IO_L25P_5	W9	
IO_L27N_5/VREF_5	V9	
IO_L27P_5	AB9	BD2_B8
IO_L28N_5/D6	AA9	BD2_A8
IO_L28P_5/D7	Y10	BD2_B6
IO_L29N_5	W10	
IO_L29P_5/VREF_5	AB10	BD2_A5
IO_L30N_5	AA10	BD2_C6
IO_L30P_5	W11	BD2_D9
IO_L31N_5/D4	V11	
IO_L31P_5/D5	AA11	BD2_C7
IO_L32N_5/GCLK3	Y11	BD2_B5
IO_L32P_5/GCLK2	T9	
VCCO_5	T10	
VCCO_5	T11	
VCCO_5	U8	
VCCO_5	Y8	
VCCO_5		

SPARTAN3_FG456

VD2V5

RHS BANK6

U12G

IO	Y1	
IO_L01N_6/VRP_6	Y3	VRP6
IO_L01P_6/VRN_6	Y2	VRN6
IO_L16N_6	W4	TX4_DATA_N
IO_L16P_6	W3	TX4_DATA_P
IO_L17N_6	W2	RX4_DATA_N
IO_L17P_6/VREF_6	W1	RX4_DATA_P
IO_L19N_6	V5	RX2_SP_N
IO_L19P_6	U5	RX2_SP_P
IO_L20N_6	V4	/CK4
IO_L20P_6	V3	CK4
IO_L21N_6	V2	TX3_UTP_N
IO_L21P_6	V1	TX3_UTP_P
IO_L22N_6	T6	TX2_DATA_N
IO_L22P_6	T5	TX2_DATA_P
IO_L23N_6	U4	RX3_DATA_N
IO_L23P_6	T4	RX3_DATA_P
IO_L24N_6/VREF_6	U3	TX2_UTP_N
IO_L24P_6	U2	TX2_UTP_P
XC3S1000/IO_L26N_6	T3	
XC3S1000/IO_L26P_6	R4	
IO_L27N_6	T2	RX3_SP_N
IO_L27P_6	T1	RX3_SP_P
XC3S1000/IO_L28N_6	R5	
XC3S1000/IO_L28P_6	P6	
XC3S1000/IO_L29N_6	R2	
XC3S1000/IO_L29P_6	R1	
XC3S1000/IO_L31N_6	P5	
XC3S1000/IO_L31P_6	P4	
XC3S1000/IO_L32N_6	P2	
XC3S1000/IO_L32P_6	P1	
XC3S1000/IO_L33N_6	N6	
XC3S1000/IO_L33P_6	N5	
IO_L34N_6/VREF_6	N4	TX3_DATA_N
IO_L34P_6	N3	TX3_DATA_P
IO_L35N_6	N2	/CK3
IO_L35P_6	N1	CK3
IO_L38N_6	M6	RX2_DATA_N
IO_L38P_6	M5	RX2_DATA_P
IO_L39N_6	M4	TX1_UTP_N
IO_L39P_6	M3	TX1_UTP_P
IO_L40N_6	M2	/CK2
IO_L40P_6/VREF_6	M1	CK2
VCCO_6	M7	
VCCO_6	N7	
VCCO_6	P7	
VCCO_6	R3	
VCCO_6	R6	

SPARTAN3_FG456

VD2V5

RHS BANK7

U12H

IO	C2	
IO_L01N_7/VRP_7	C3	VRP7
IO_L01P_7/VRN_7	C4	VRN7
IO_L16N_7	D1	/CK10
IO_L16P_7/VREF_7	C1	CK10
IO_L17N_7	E4	
IO_L17P_7	D4	
IO_L19N_7/VREF_7	D3	
IO_L19P_7	D2	
IO_L20N_7	F4	RX10_SP_P
IO_L20P_7	E3	RX10_SP_N
IO_L21N_7	E1	TX10_UTP_N
IO_L21P_7	E2	TX10_UTP_P
IO_L22N_7	G6	
IO_L22P_7	F5	
IO_L23N_7	F2	
IO_L23P_7	F3	
IO_L24N_7	H5	
IO_L24P_7	G5	
XC3S1000/IO_L26N_7	G3	
XC3S1000/IO_L26P_7	G4	
IO_L27N_7	G1	TX10_DATA_N
IO_L27P_7/VREF_7	G2	TX10_DATA_P
XC3S1000/IO_L28N_7	H1	
XC3S1000/IO_L28P_7	H2	
XC3S1000/IO_L29N_7	J4	
XC3S1000/IO_L29P_7	H4	
XC3S1000/IO_L31N_7	J5	
XC3S1000/IO_L31P_7	J6	
XC3S1000/IO_L32N_7	J1	
XC3S1000/IO_L32P_7	J2	
XC3S1000/IO_L33N_7	K5	
XC3S1000/IO_L33P_7	K6	
IO_L34N_7	K3	RX10_DATA_N
IO_L34P_7	K4	RX10_DATA_P
IO_L35N_7	K1	/CK1
IO_L35P_7	K2	CK1
IO_L38N_7	L5	TX1_DATA_N
IO_L38P_7	L6	TX1_DATA_P
IO_L39N_7	L3	RX1_SP_N
IO_L39P_7	L4	RX1_SP_P
IO_L40N_7/VREF_7	L1	RX1_DATA_N
IO_L40P_7	L2	RX1_DATA_P
VCCO_7	H3	
VCCO_7	H6	
VCCO_7	J7	
VCCO_7	K7	
VCCO_7	L7	

SPARTAN3_FG456

VD2V5

Project Title: Manchester University 1		Sheet Size: A3
Sheet Title: FPGA2.SCHDOC		Revision: 1.0
Date: 02/06/2008	Sheet: 4 of 9	
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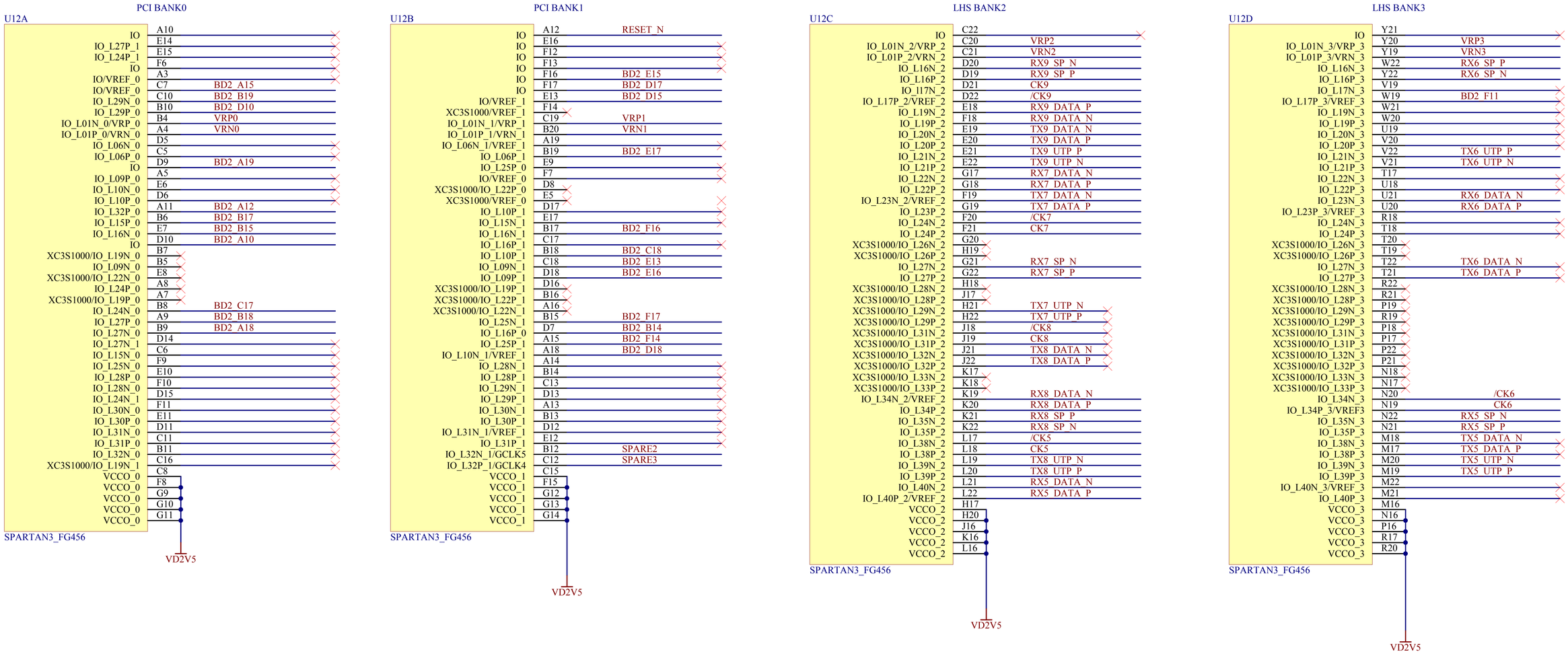

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Date: 02/06/2008	Sheet: 5 of 9	
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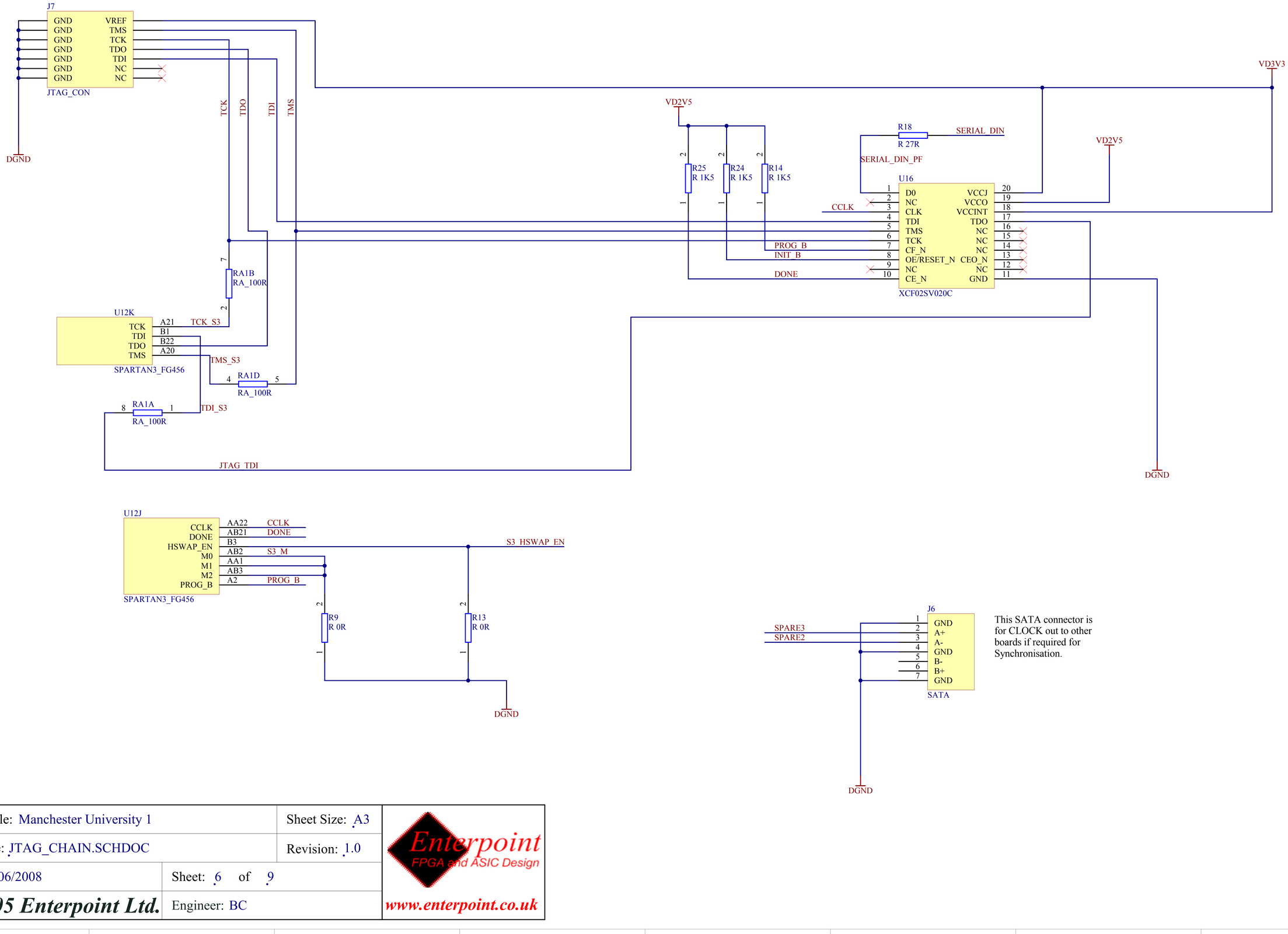

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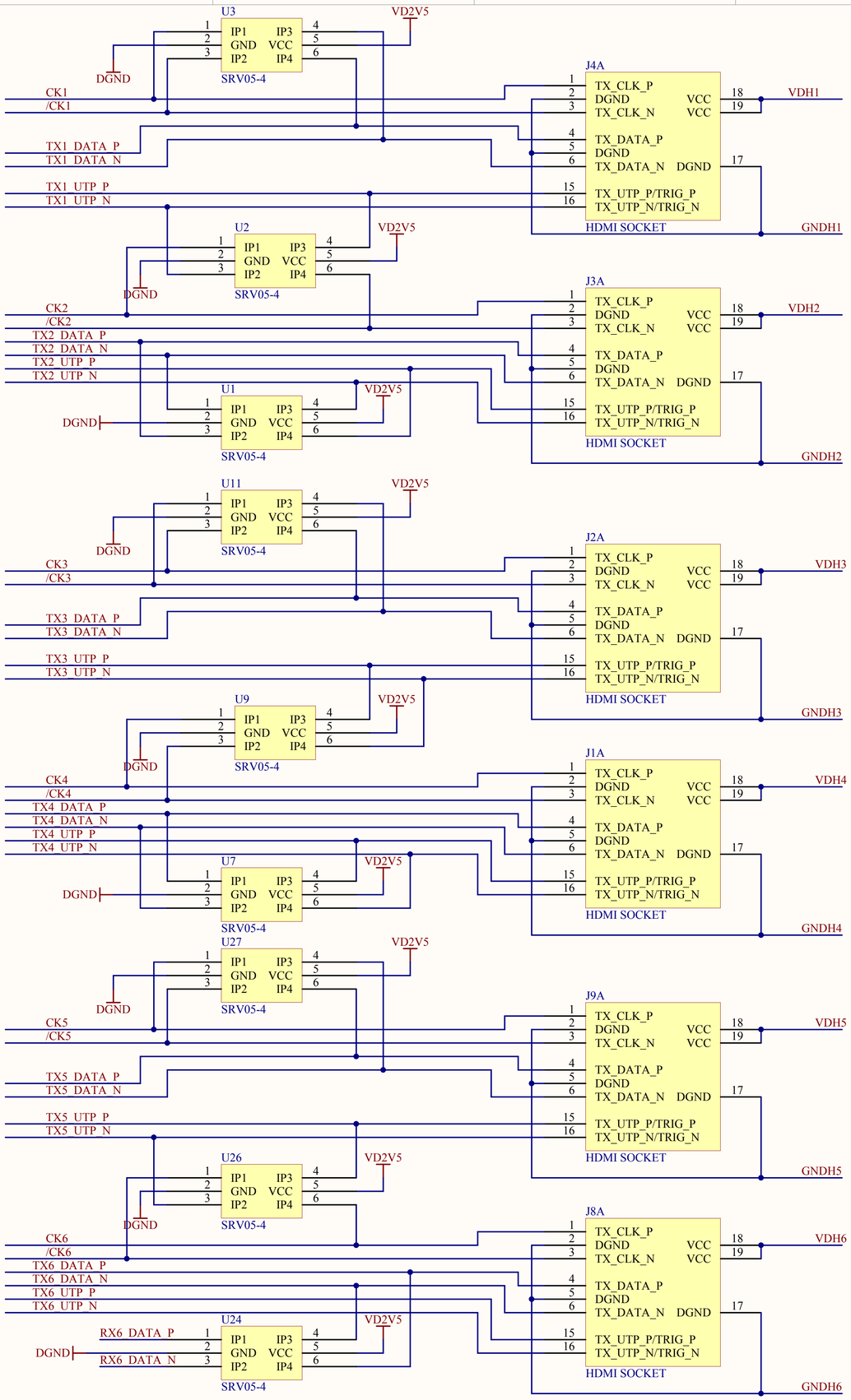

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Date: 02/06/2008	Sheet 7 of 9	
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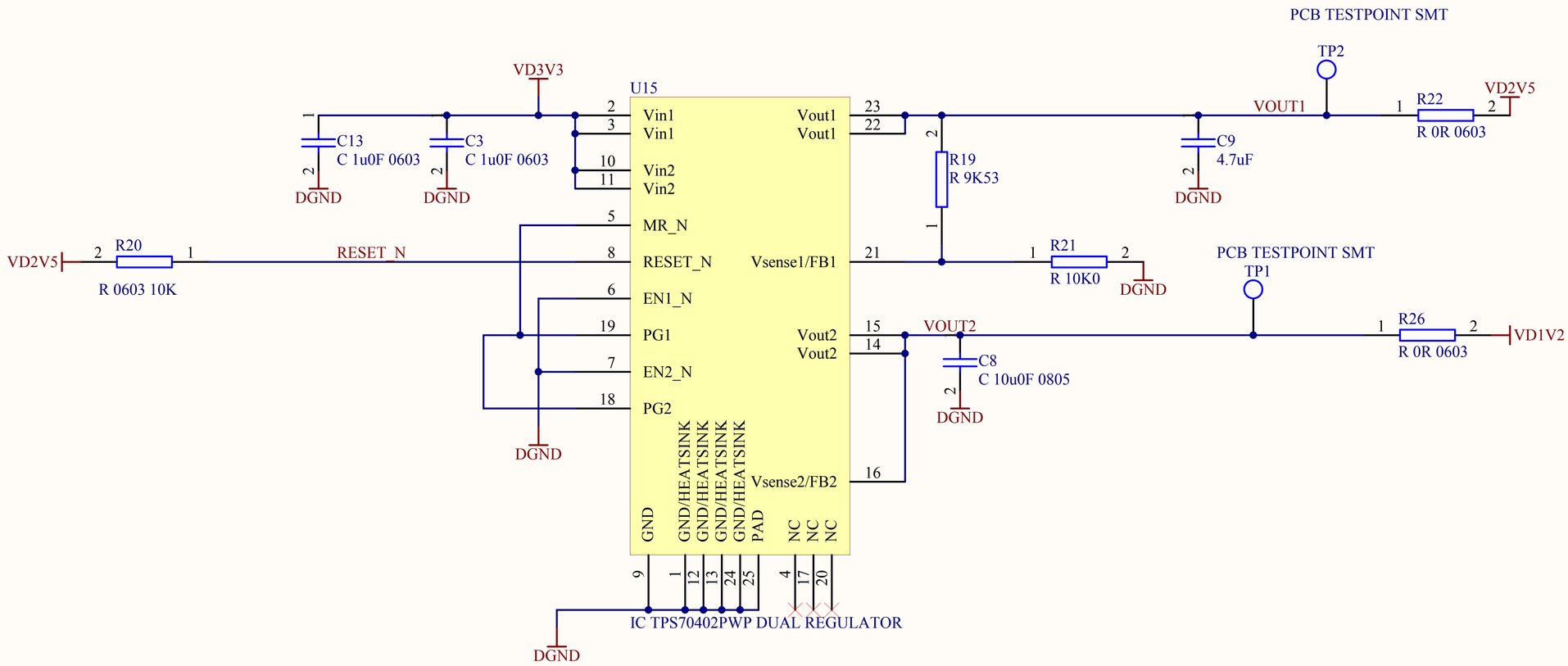

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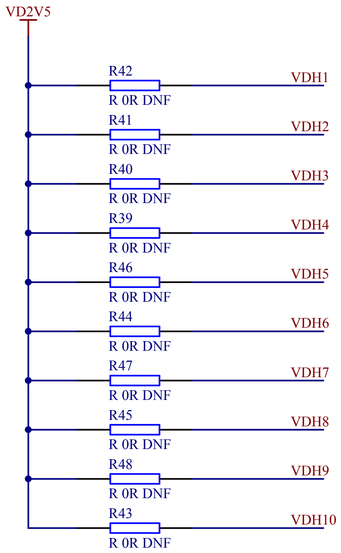

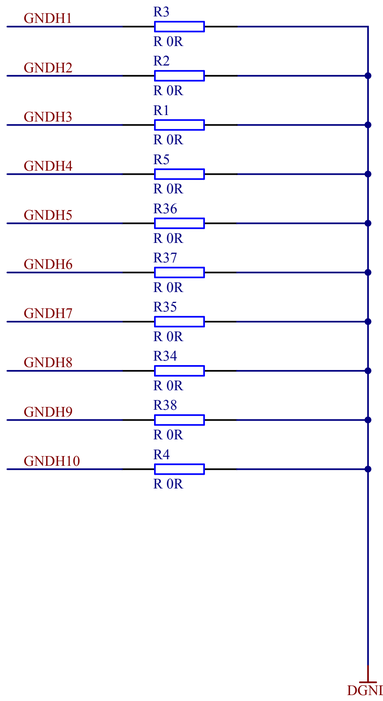

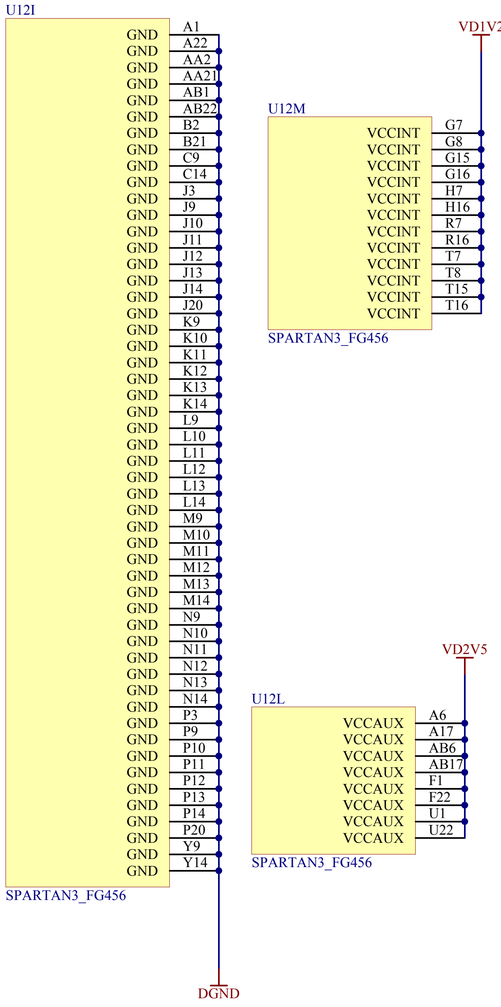

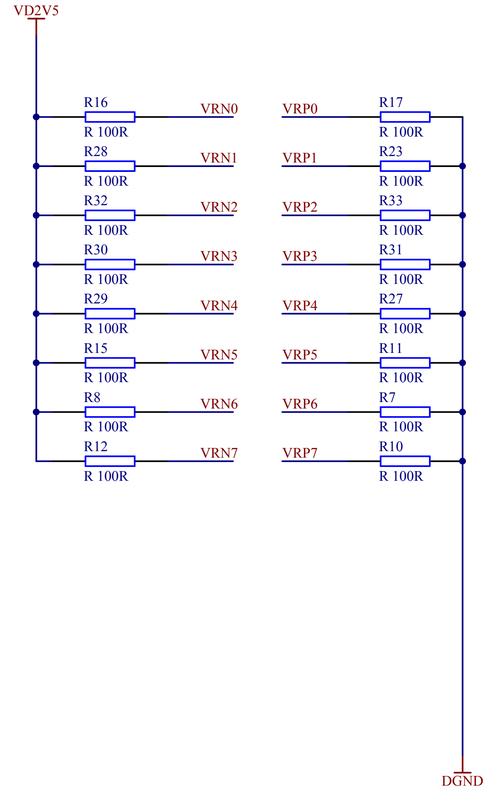

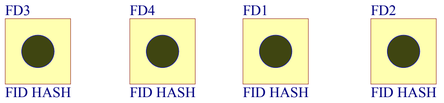

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Sheet Title: FPGA_POWER_ETC.SCHDOC	Revision: 1.0	
Date: 02/06/2008	Sheet: 9 of 9	
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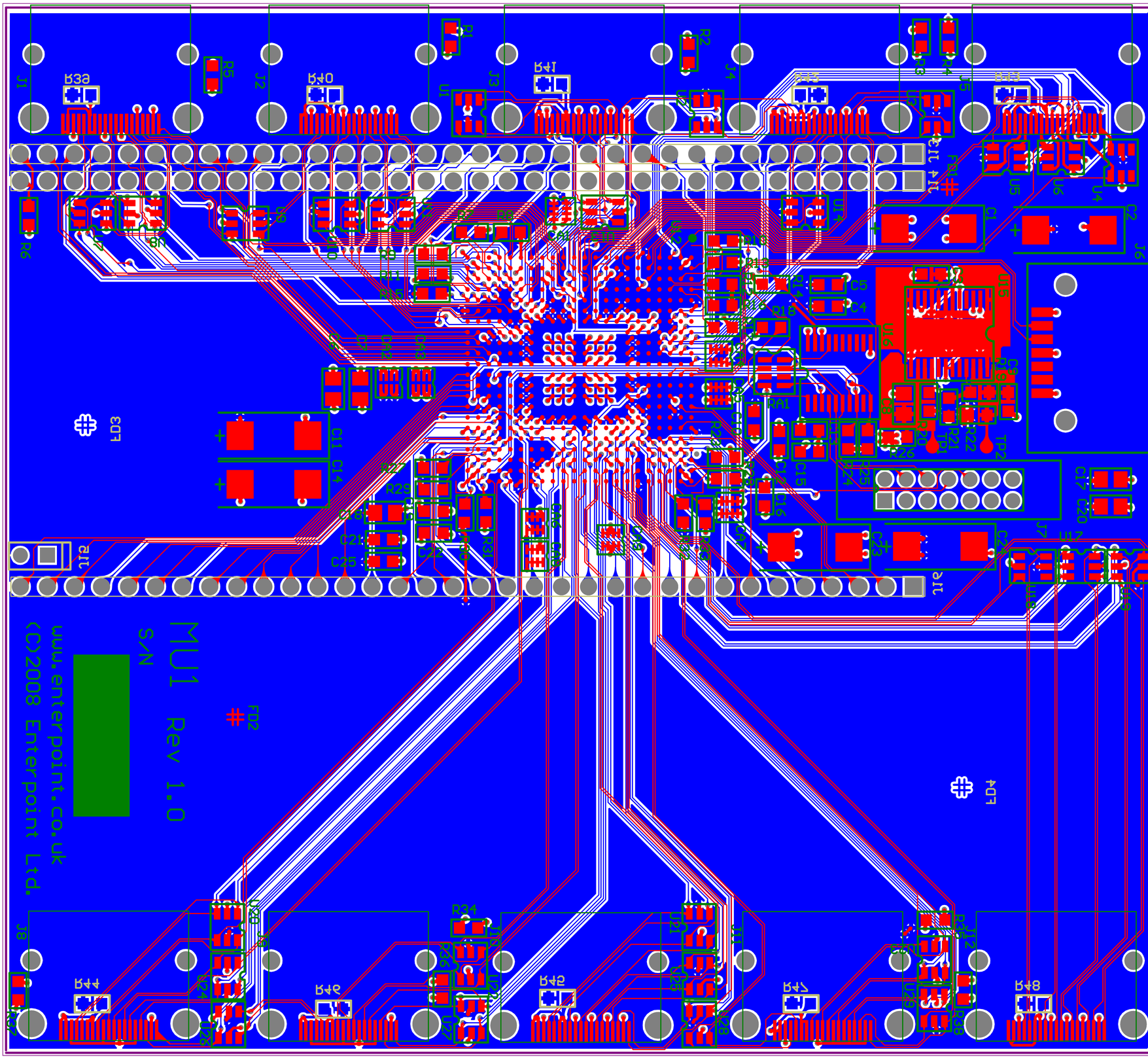
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