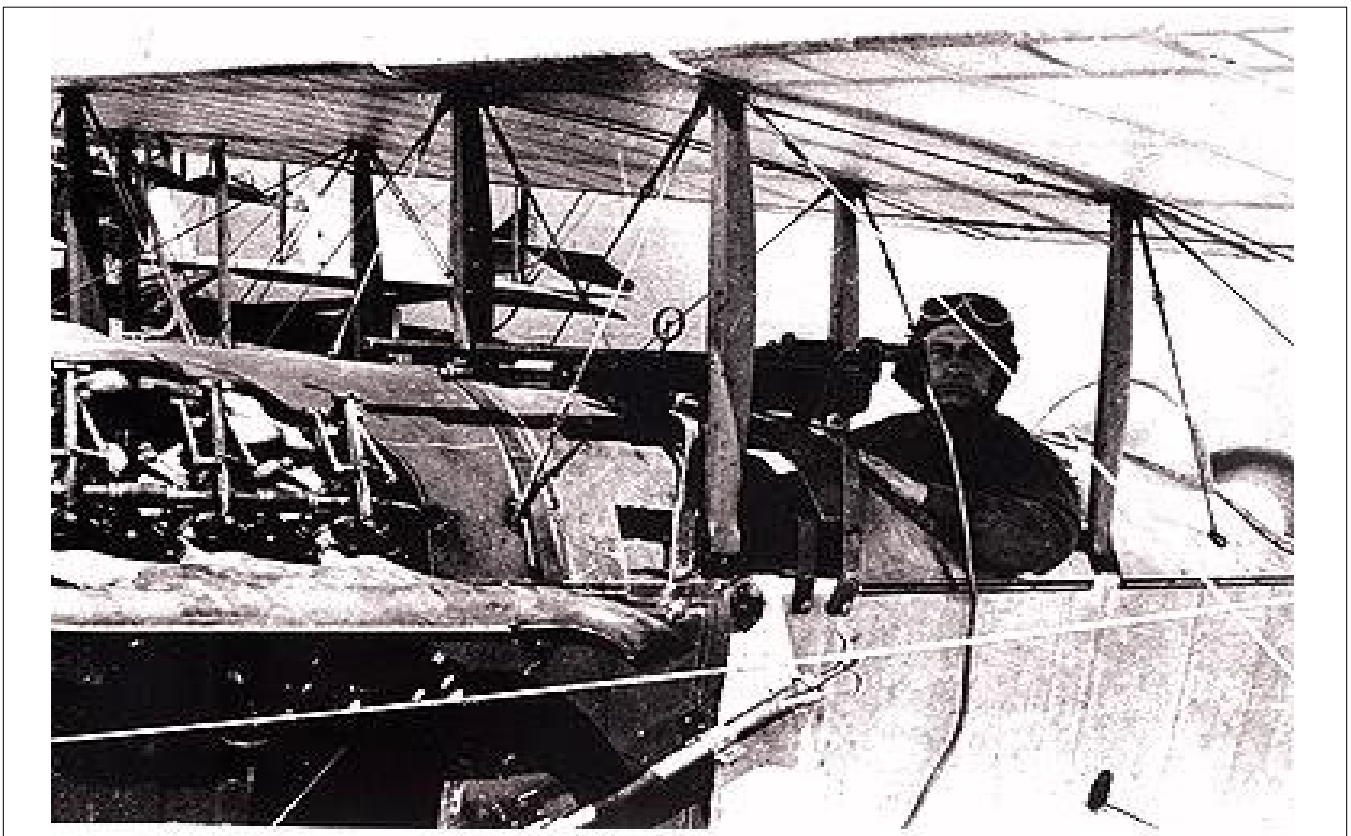


Oscillator Jitter FAQ



Jitter, in the sense of timing error, was a life-or-death matter for WWI aircraft armed with synchronized machine guns. The machine gun's firing mechanisms was timed to fire rounds through the whirling propeller blades. Too often, timing errors caused the gun to 'remodel' the propeller, with untoward results.

Fortunately, jitter in electronics circuits is usually less dire. In an emergency, of course, loss of communications can nonetheless become a very serious matter. This JITTER FAQ discusses some of the obvious aspects of communications circuit jitter, and draws the reader's attention to some of jitter's less than obvious consequences.

By:

Dan Nehring, V-P Engineering
MF Electronics Corp
10 Commerce Drive
New Rochelle, NY 10801

Tel: 800 331 1236
Fax: 914-712-2290
Internet: <http://www.mfelectronics.com>
email: dan@mfelectronics.com

Oscillator Jitter FAQ

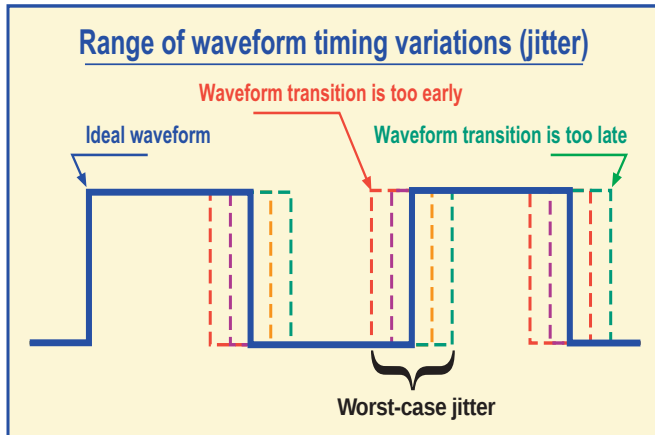
Jitter is a heightened concern for wireless systems, especially as frequency and data rate push ineluctably upwards. From the standpoint of a oscillator manufacturer, there are aspects of clock and data signal waveform jitter that merit particular attention. The following Jitter FAQ discussion highlights some of them. Hopefully, the answers to the jitter questions will provide guideposts for minimizing jitter-induced data error.

SUMMARY

- Q1 What is jitter?
- Q2 What causes jitter?
- Q3 How are ONE and ZERO values read?
- Q4 How does *data* jitter compromise readability?
- Q5 How do *data* & *clock* jitter together cause unreadability?
- Q6 Why is jitter an increasing concern at higher frequencies?
- Q7 Why is data signal rise rate important?
- Q8 Why should *clock* signals have fast rise time?
- Q9 Why is clock waveform symmetry important?
- Q10 What's the benefit of dual complementary logic?
- Q11 What clock oscillator parameters besides jitter are important?
- Q12 How do you measure jitter?

Introduction

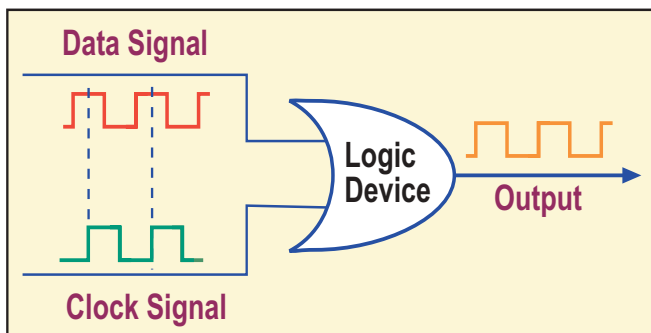
Rapid growth of the wireless infrastructure has elevated jitter from an obscure circuit characteristic to a priority specification. This is especially true for clock oscillators and VCXOs, which provide time and frequency references for today's wireless systems.



Q1—What Is Jitter? Jitter refers to a waveform's timing uncertainty. Successive waveforms—although at fixed frequency—don't arrive at the expected intervals. Historically, when digital systems operated in the kilohertz frequency range, jitter was largely inconsequential. At today's frequencies, a few nanoseconds timing uncertainty can amount to a substantial fraction of the cycle's total duration.

Q1—What is Jitter? In simplest terms, jitter refers to the uncertainty, or variability, of waveform timing.

Q1 illustration presents the general idea of a “jittery” waveform. Successive cycles of the waveform (shown as perfect squarewaves) arrive at their destination slightly late, or slightly early. In wireless communications, such waveforms will typically convey logic ONE or ZERO values,



Q1A—The clock signal's rising edge is synchronized with the center of the data waveform to initiate the reading of ONE or ZERO data values. Excessive jitter alters timing of the clock or data signal (or both), increasing the likelihood of a reading error. (See Figures Q3 thru Q5 for discussion).

which subsequent circuits will decode.

A clock oscillator's signal is used to initiate the data interrogation process. That is, it times the reading of ONE or ZERO values. The clock's rising edge “views” the center of the data waveform. (Ringing and rise time transients have subsided by this time). Illustration Q1A shows how the clock waveform's leading edge is aligned with the center of a data signal. Jitter that causes the waveform to be late or early (relative to the clock's center-waveform timing), can displace the interrogation “window” beyond the point of data readability.

Q2— What Causes Jitter? The ubiquitous noise associated with all semiconductor circuits is one source of waveform triggering uncertainty (jitter). Wireless applications expose communications circuits to a wider range of interference. Radio signals are susceptible to atmospheric effects, lightning, RFI, and reflections from nearby structures. Cell phones and mobile wireless systems are vulnerable to signal multipaths, making the system especially vulnerable to jitter's information corrupting effects. Power supply transients and faulty connections also take their toll.

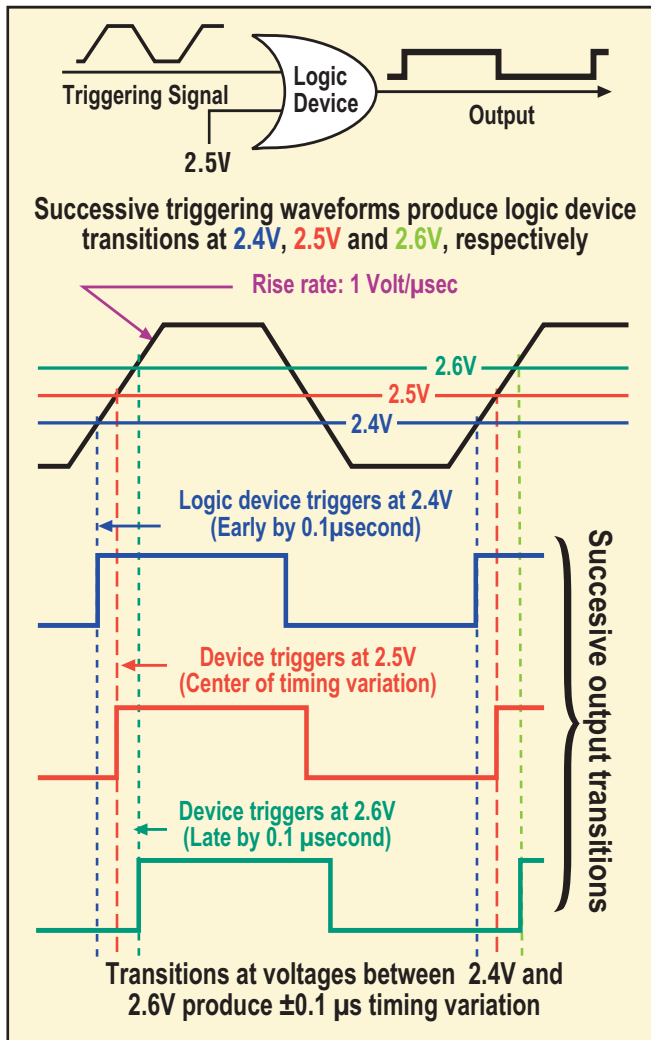
Illustration Q2 shows how a logic gate's noise creates variable triggering. In this example, the circuit's vulnerability to thermal and other noise is exaggerated for simplicity of explanation.

The logic gate is designed to make a transition whenever the rising edge of the triggering waveform reaches approximately 2.5V. That is $V_{dd}/2$ for 5V systems. Circuit designers are actually less concerned with absolute triggering voltage than consistency of triggering at some voltage *near* this 2.5V value.

The gate of Q2 will rarely respond to the triggering waveform at exactly 2.5V. In normal circumstances, there will be a Gaussian distribution of triggering thresholds around the 2.5V level.

To highlight the jitter creating mechanisms, con-

sider how Q2 logic gate responds to three successive input waveforms at 2.4V, 2.5V and 2.6V. Actual trigger voltage span is then -0.1V to +0.1V.



Q2—What causes jitter? (One cause of jitter is a logic device's variable triggering threshold. Instead of switching between ONE and ZERO values when the triggering voltage rises to 2.5V (for instance), the logic circuit responds to various triggering voltages around this 2.5V threshold. In this example, the logic circuit responds when successive triggering waveforms reach 2.4V, 2.5V and 2.6V. A triggering voltage rise rate of 1 volt per microsecond produces logic device transitions with $\pm 0.1V$ variability around the 2.5 nominal triggering level. Waveform timing uncertainty (jitter) is then $\pm 0.1 \mu s$.

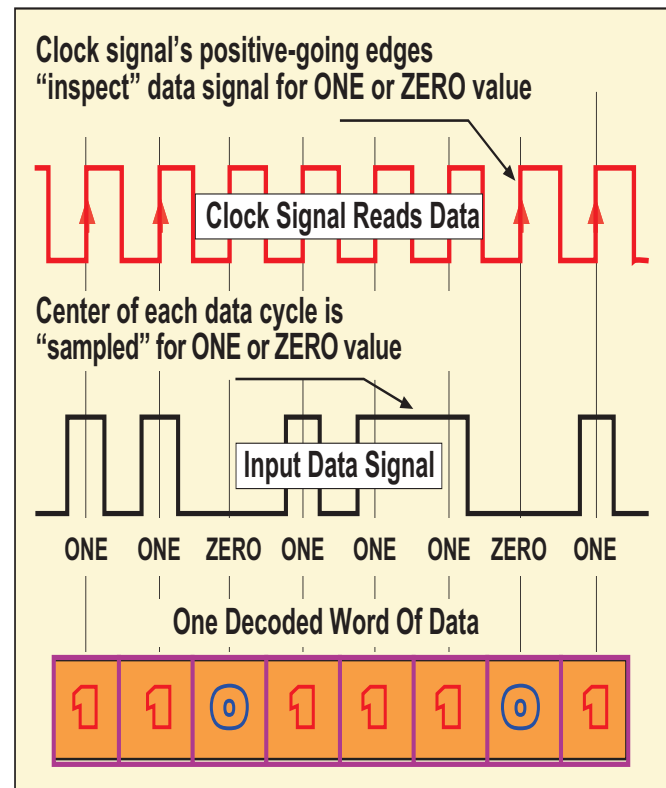
(Typically, the range of triggering voltages would be much smaller).

Suppose the input waveform rises at the rate of 1 volt per microsecond. The $\pm 0.1V$ triggering variability leads in turn to a $\pm 0.1V \div 1V/\mu s = \pm 0.1\mu s$ range of triggering uncertainty. In other words, jitter extends from $-0.1\mu s$ to $+0.1\mu s$.

Jitter between successive signal cycles is referred to as *cycle-to-cycle jitter*. This is typically not the critical measure of jitter. In most instances, many random waveforms are sampled for period duration. Jitter is then analyzed over the entire population of waveform duration measurement. The result is known as *period jitter* measurements.

Q3—How are ONE and ZERO values read?

Communications and digital processing depend on the ability to decode and “read” the ONE and ZERO values of logic waveforms. In illustration

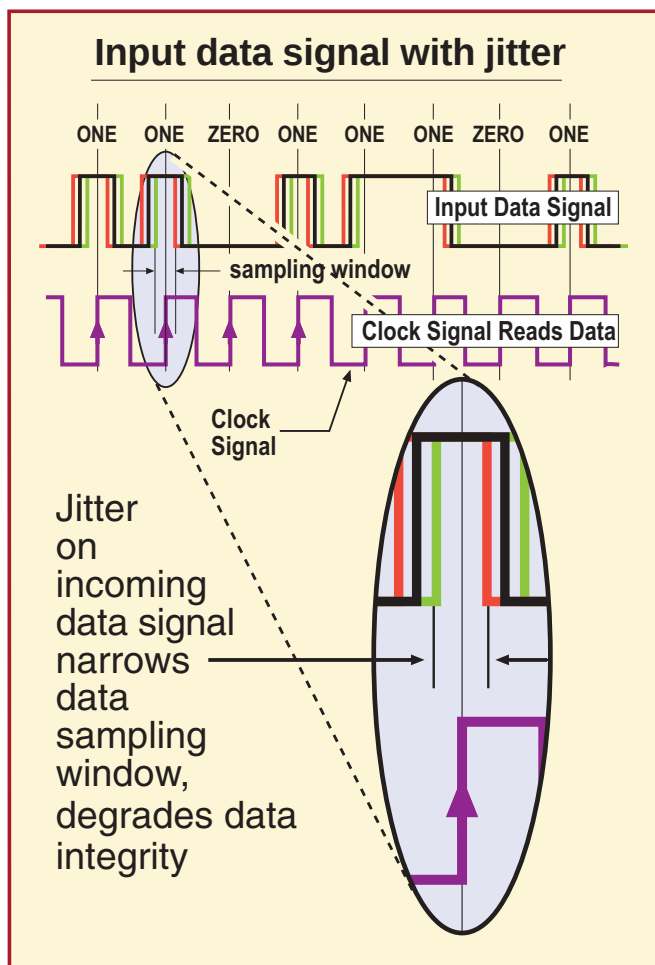


Q3—How are ONE and ZERO values read? This simplified diagram presents a jitter-free data signal, plus a clock signal that initiates the data reading process. Full scale signal voltage occurs at the center of the data waveform, so that's where the clock signal's leading edge “looks” at the data. (The waveform's ONE or ZERO state is expressed least ambiguously at this full scale signal voltage). Output circuits reproduce the ONE or ZERO data values that the clock signal “sees.”

Q3, the leading edge of the clock waveform initiates the data signal inspection process. It “looks at” the data signal to determine whether there are ONE or ZERO logic values.

Inspection, in this example, is undertaken at the center of the data signal. This region of the data

waveform is least ambiguously a ONE or a ZERO. (Ringing or other distortions will have settled down by the center of that region).



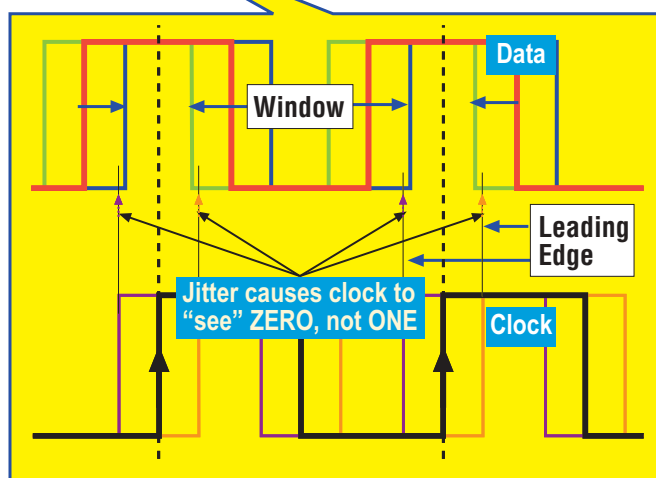
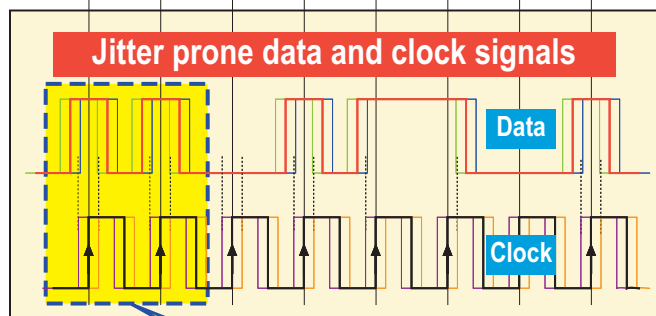
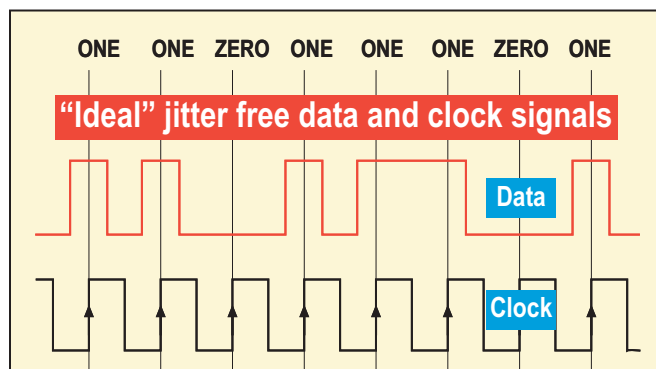
Q4—How does data signal jitter compromise readability? Jitter on the data signal reduces the width of the effective “window” available for determining ONE or ZERO values. See the expanded region for clarity.

Q4—How Does Data Signal Jitter Compromise Readability? Jitter on the data signal reduces the usable width of the center-waveform “window” available for monitoring logic values. The result can be an indecipherable message.

Designers of today’s wireless systems demand the use of low jitter circuit components and topology. Critical timing components, such as clock oscillators and VCXOs, are required to have rigorous control over jitter performance.

Q5—How do simultaneous data and clock signal jitter prevent readability? Illustrations Q5 (top) shows data and clock free of jitter. The center

panel shows jitter on both data and clock signals. The bottom panel is an expanded view of the resulting data reading process. Jitter imposes a twofold penalty. First, data signal jitter narrows the viewing window for determining ONE or ZERO values. Second, jitter on the clock signal displaces the rising edge from the center of the data “window.” In this bottom Q5 view, excessive data and clock signal jitter cause the clock’s leading edge to

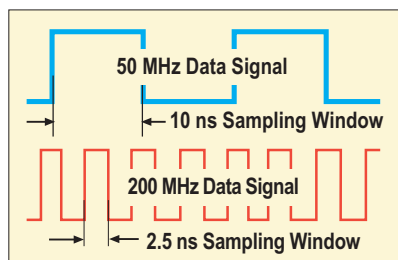


Q5—How do simultaneous data and clock jitter prevent readability? In this illustration—disastrously! The “early” clock signals coincide with “late” data signals to read ZERO when actual value is ONE. Conversely, the late clock signals look at early data signals, again “seeing” ZERO when the true value is ONE. The net result is unequivocally a reading error.

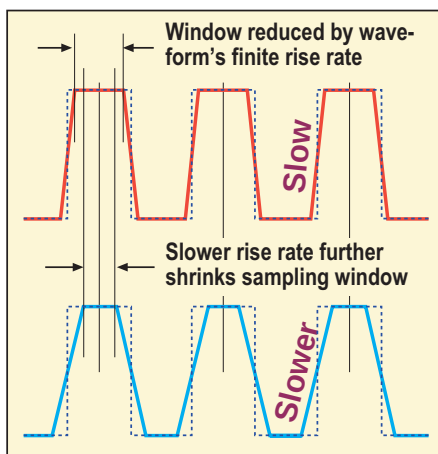
“see” a ZERO value when ONE is the true information content.

Q6—Why is jitter an increasing concern at higher frequencies? For each doubling of frequency, the maximum “window” available for reading ONE or ZERO data values is halved. (Diagram Q6). Jitter then amounts to a proportionately

larger fraction of the ONE or ZERO waveform duration. The *effective* window for data reading therefore shrinks significantly with increasing frequency.



Q 6—Why is jitter an increasing concern as frequency rises? For every doubling of frequency, the window for determining a signal's ONE or ZERO value is halved. At 50 MHz the window duration is 10 nanoseconds. At 200 MHz, it shrinks to 2.5 ns. Jitter of ± 100 picoseconds peak-peak amounts to 1% of of the window duration at 50 MHz. At 200, jitter is 4% of the maximum sampling window. At gigahertz frequencies, ± 100 ps jitter becomes completely unacceptable!



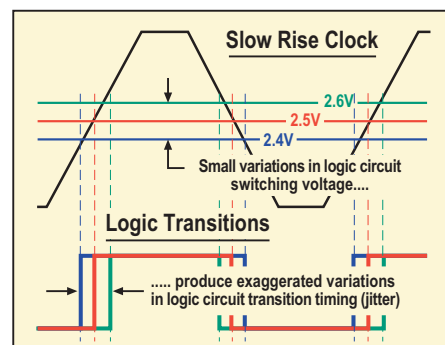
Q7—Why is data signal rise rate important? Slow-rise waveforms reduce the period of full scale signal voltage. (The most unambiguous window for reading ONE or ZERO data values). Reduction of the usable sampling window makes the signal increasingly susceptible to reading error caused by jitter and other distortions

the maximum period of full scale voltage. (In other words, the “window” for determining ONE and ZERO values is reduced).

The upper and lower waveforms of illustration Q7 demonstrate how progressively slower signal rise rate cuts into the data sampling window. Put

differently, jitter becomes a progressively larger proportion of the data monitoring window.

Q8—Why should clock signals have fast rise rates. Slow clock oscillator rise rate paves the way for variability in data signal sampling. (The clock signal's rising edge initiates the reading of data values). But with a slow-rise clock,



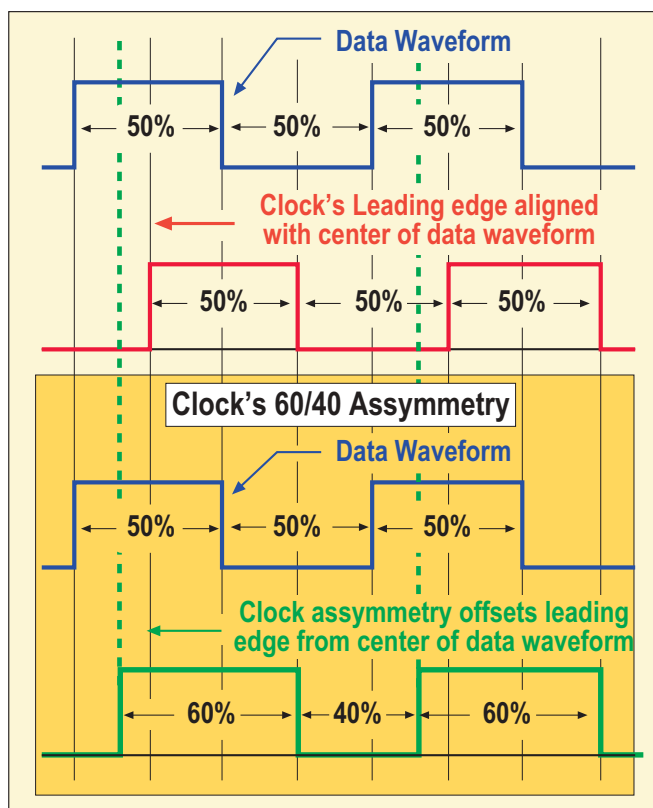
Q8—Why Should Clock Signals Have Fast Rise Rate? The clock signal initiates a logic transition when its voltage rises to a critical threshold. (To nominal 2.5V in this example). Variations in this transition voltage will advance or delay the logic circuit's transition. Slow-rise clock waveforms exaggerate the effect of triggering voltage variations. At 1 volt per microsecond clock rise rate, a +0.1V deviation from nominal 2.5V triggering voltage delays the logic transition by 0.1 microsecond. At 0.5V/ μ s rise rate, the same +0.1V triggering voltage variation doubles the transition delay.

where exactly is the waveform's leading edge? In fact, the functional leading edge is the actual voltage threshold that initiates data determination. Illustration Q8 shows how logic circuit triggering thresholds vary from one data cycle to the next. Variable timing leads to advancing or retarding the logic transitions. That is, slow clock rise rates increase the potential for clock jitter. The slower the rise rate, the more exaggerated the timing variation (jitter) becomes.

Q9—Why is waveform symmetry important? Communications circuits use leading and trailing edges of their waveforms to trigger subsequent logic events. Such triggering processes require system-wide synchronism between all the triggering functions. Otherwise, the triggering edge of one waveform will not coincide with the window awaiting its triggering stimulus. Ideal logic waveforms have 50%/50% symmetry. That is, both waveform half cycles have the same duration. Actual waveforms, of course, depart from this ideal.

Illustration Q9 demonstrates the need for wave-

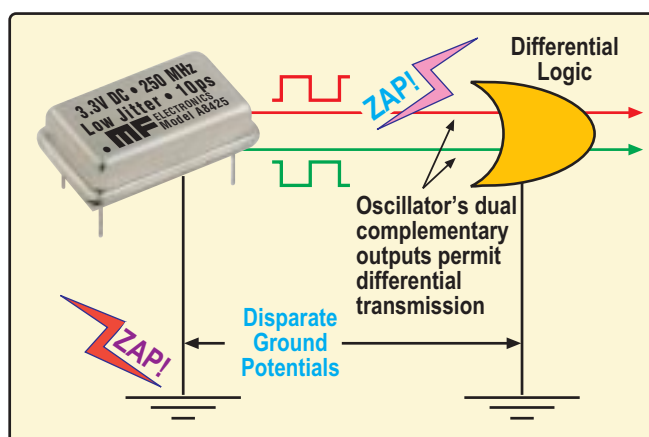
form symmetry. As discussed earlier, the midpoint of each data waveform provides an interrogating window. Clock signals (top panel), aligned with window centers, initiate the ONE or ZERO data reading process.



Q9—Why is clock waveform symmetry important? Rising and trailing edges of 50%/50% symmetry clock waveforms are easily synchronized with data reading “windows” (top). Asymmetrical clock waveforms (bottom), displace either the leading or trailing edges away from the center of the data windows

The bottom panel of Q9 illustrates the effect of clock waveform asymmetry. The mark-space ratio is no longer 50%/50%. Lack of waveform symmetry offsets the clock’s rising edge from the center of the data window. Data reading then becomes susceptible to jitter and other distortions.

Q10—What’s the jitter resisting benefit of dual complementary logic? Signal traffic traveling in all directions on a printed circuit board brings to mind a busy railroad switching yard. Some of the PCB traces carry data signals, others haul DC supplies, and most traces are potential receivers or transmitters of transients and noise.



Q10—What’s The Benefit Of Differential Transmission? Differential logic circuits respond to signals *between* the input connections, not between a single input and ground. Accordingly, differential transmission through parallel PCB traces provides immunity to transients capacitively or inductively coupled from nearby circuits. Transients injected into the ground plane are likewise ignored.

The analog signal world has long exploited differential transmission to minimize interference. With rising frequency, and RFI everywhere, so too are wireless technologies.

Differential clock and signal transmission across circuit board traces provides significant protection against pickup from neighboring circuits. This is because interference tends to be coupled into *both* conductors simultaneously. Differential logic devices respond to the signal *difference* be-

tween inputs, not to signals between input and ground. Put more technically, crosstalk and noise become common-mode and are ignored in proportion to the device’s common mode rejection ratio (CMRR).

Clock Oscillator Specs

(Jitter related specs)

Jitter
Output rise/fall times
Output symmetry
Dual complementary output

(General specs)

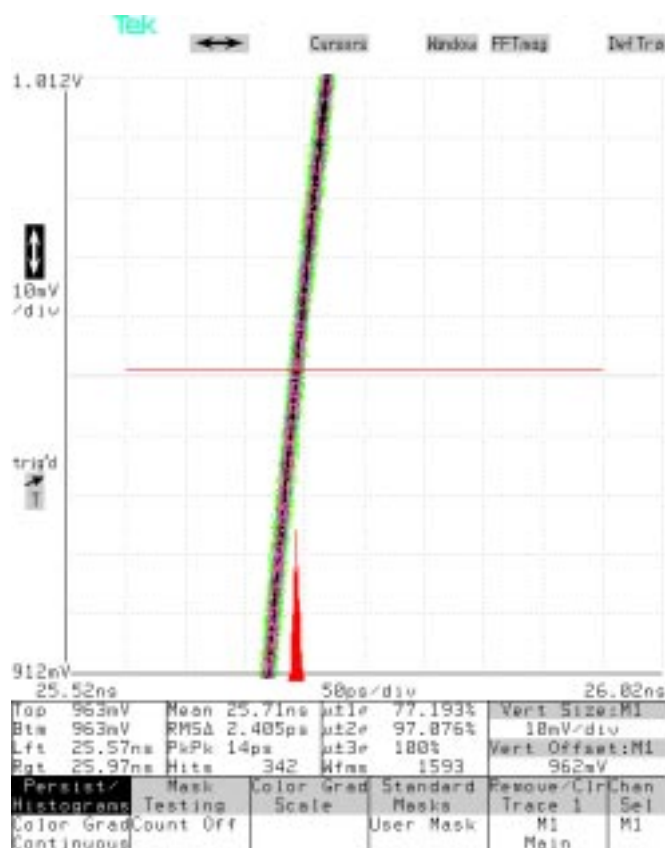
Frequency
Logic type
Thermal stability
Aging
Operating voltage
Maximum load current
Package type, size

Q11—What clock oscillator parameters besides jitter are important? Output rise/fall rate and waveform symmetry have a direct role in minimizing the effect of jitter. So can dual complementary outputs. Good engineering practice matches the remaining specifications to the job.

Q11—What clock oscillator parameters besides jitter are important. This FAQ article has already highlighted several important oscillator parameters. They include low jitter (typically below 10 picoseconds RMS) Q1, fast rise rate Q8, and waveform symmetry Q9. Dual complementary outputs Q10 may be a luxury or a necessity, depending on the need for noise immunity.

Additional oscillator specifications of importance include frequency, thermal stability, and long-term stability. The operating voltage needs to be specified, as well as maximum load current. Oscillators come in a variety of through hole and surface mount packages—a further variable that needs to be pinned-down.

Q12—How do you measure jitter? Several



Q12—How do you measure jitter? Typical jitter instrumentation permits a section of the waveform to be selected and viewed in detail. In this display, the jitter characteristics of a clock oscillator's rising edge are analyzed. The instrument presents a section of the waveform (diagonal line) as it crosses a fixed threshold voltage. The display includes a histogram of jitter behavior (red) for the selected waveform section. In addition, the instrument determines signal rise rate, peak-to-peak and RMS jitter values, plus additional analytical information

instrument manufacturers offer communications signal analyzers or oscilloscope-based systems for jitter measurement and analysis. Among them: Agilent, Tektronix, LeCroy and Wavecrest. Typical jitter measuring instruments present a composite picture of waveform and jitter characteristics and statistics.

The instrument analyzes the user-selected portion of a waveform, or measures the periods of a signal. Illustration Q12 shows the rising edge of a high speed, low jitter clock oscillator output. Clock waveform jitter is measured as each rising cycle crosses a fixed voltage threshold. Many successive clock waveforms are superimposed on one another to "spread" the plot. The broader the jitter span, the thicker the plot. The instrument then plots a histogram of jitter characteristics in red (center, bottom).

The jitter histogram affords insight into the waveform's behavior. Does it exhibit multiple peaks? If so, it is likely that a dominant factor, such as power supply ripple, is modulating the clock. Alternatively, you may be measuring a clock with significant amounts of sub-harmonic energy. Is the histogram tall and narrow or short and fat? Tall and narrow is usually the desired result, implying a tight control over jitter.

A short and fat jitter distribution pattern, but symmetrical about its peak, indicates a clock oscillator that is inherently noisy. Or maybe the clock's spectrum has been purposely "spread" to enhance EMI compliance.

Is the jitter distribution notably asymmetrical? Of particular concern would be a histogram where there are unexplained outliers from a normal distribution. The outliers would cause "large displacement" timing failures, and wreak havoc on bit error rates in wireless systems.

END