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Jitter Measurements for CLK Generators or Synthesizers

Clock (CLK) generators and synthesizers form the pulse of a complex digital system and errors in a clock's signal quality can have wide-ranging effect.

One of the most important performance measurements is clock jitter. Jitter is defined as "the short-term variation of a signal with respect to its ideal position in time." In a clock generator chip, there are many factors which contribute to output clock jitter, such as the device noise, supply variation, jitter in the reference clock, loading condition, and interference coupled from nearby circuitry.

Jitter can be measured in different ways, including period jitter J_{PER}, cycle-to-cycle jitter J_{CC}, and accumulated jitter J_{ACC}. In general, jitter consists of the deterministic jitter and random jitter. Since the deterministic jitter in most digital systems is introduced frommany different bit patterns from the digital data, clock signal jitter can usually be considered to be just random jitter. In this application note, we will go over the definitions and introduce test setups for making measurements.

Jitter Definitions

Period Jitter: J_{PER}

Jitter J_{PER} is the most popular jitter measure. It is the time difference between a measured cycle period and the ideal cycle period. Due to its random nature, this jitter can be measured as Peak-to-Peak or by Root Mean Square (RMS). Let's define the clock rising edge crossing point at the threshold V_{TH} as $T_{PER}(n)$, where n is the time domain index, as shown in Fig. 1. Mathematically, we can describe J_{PER} as

$$\text{Period Jitter:}\quad J_{PER} = T_{PER}(1) - T_0 \qquad \text{Eq. 01}$$

where T_0 is the ideal clock cycle. Fig. 1 shows the relation between J_{PER} and T_{PER} in a clock waveform.

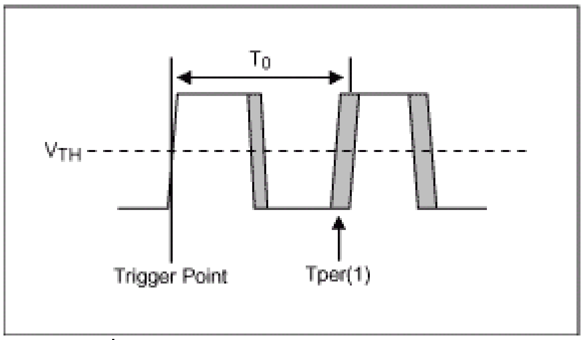

Figure 1. Period Jitter Measurement.

Cycle to Cycle Jitter: Jcc

Jitter Jcc is the time difference of two adjacent clock periods. This is also called "Short Term Jitter." It depends only on the adjacent clock cycles.

For some digital circuits, Jcc is more meaningful than J_{PER}. Jcc is the right parameter for calculating the margins for set-up time and hold-on time. If only J_{PER} is employed in the calculation, the result is often too conservative. As an extreme example, to a spread spectrum (SS) clock, Jcc can be relatively small, but its J_{PER} can be very large when the measuring time is comparable to the spreading period.

Jcc is measured by its Peak-to-Peak value in a given time period. It is mathematically defined as

$$\text{Cycle-to-Cycle Jitter:}\quad Jcc = \max\{T_{PER}(n) - T_{PER}(n+1)\} \quad \text{for } n <= N \qquad \text{Eq. 02}$$

where n is a cycle index and N is a number for a given period. Fig. 2 shows the relation between Jcc and $T_{PER}(n)$ in a clock waveform.

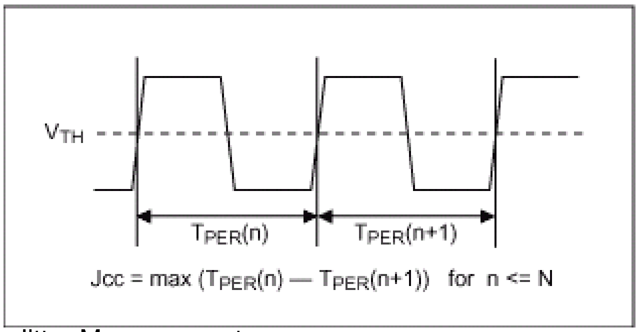

Figure 2. Cycle-to-Cycle Jitter Measurement.

Accumulated Jitter: $J_{AC}(n)$
Jitter $J_{AC}(n)$ is the time displacement of the edges of a clock relative to the triggering edge of the same clock. This jitter is a function of n and it is the general case of J_{PER}. It is measured by its Peak-to-Peak value or RMS. It gives the maximum discrepancy between two clock rising edges n cycles apart. For a digital system with synchronized packet data, this jitter measure may be the right one for system timing analysis. Its mathematic form is given as

$$\text{Accumulated Jitter:}\quad J_{AC}(n) = T_{PER}(n) - nT_0 \qquad \text{Eq. 03}$$

It is noted that $J_{AC}(n)$ is dependent on the cycle index n. Fig. 3 depicts how to measure $J_{AC}(n)$ from a clock signal

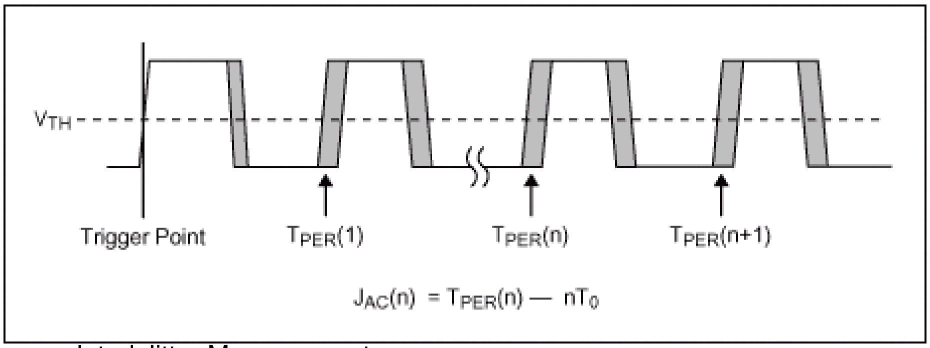

Figure 3. Accumulated Jitter Measurement.

Jitter Measurement

Time Domain Jitter Measurement
A high precision digital oscilloscope is commonly used to measure jitter. When the clock jitter is 10 times or larger than the triggering jitter of the oscilloscope, the clock jitter can be measured by triggering at a rising edge of the clock signal and measuring the jitter at the next rising edge.

SEMI (Semiconductor Equipment and Materials International) [1] has specified a more accurate method for measuring the period jitter of high-speed clock. As shown Fig. 4, the trigger is generated by the clock to be tested. This eliminates the internal jitter due to the clock source in digital oscilloscope.

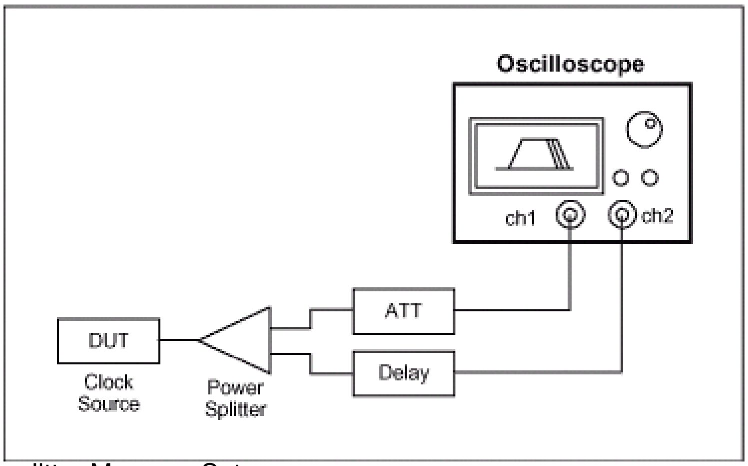

Figure 4. Self-trigger Jitter Measure Setup.

These two approaches are also called the "cursor technique" for jitter measurement. The advantages of these methods are that they are easy to understand and perform. They are good for a first-order estimate.

The concerns are that this technique is susceptible to trigger jitter, can be unreliable or misleading for accumulated jitter measurement, and lack statistical information that describe jitter characteristics.

More accurate measuring methods have been employed. Most of them use a post-sampling process of measured data using a high-speed digital oscilloscope to estimate all three jitters according to their mathematic definitions in Eqs. 1-3. This post-sampling approach provides precise results, but it can only be performed by certain high-end digital oscilloscopes from Tektronix [2] or LeCroy [3].

Frequency Domain Jitter Measurement

Jitter can also be viewed as scaled phase noise. A sinusoid signal with phase noise can be written as

$$C(t) = A\sin(\omega_c t + \theta(t)) = A\sin\left(\omega_c\left(t + \frac{\theta(t)}{\omega_c}\right)\right) \qquad \text{Eq. 04}$$

and

$$J_{PER} = \frac{\theta(t)}{\omega_c} \qquad \text{Eq. 05}$$

From Eq. 4 we see that the sinusoid signal is phase modulated by the phase noise $\Theta(t)$. Using Fourier series expansion, it can show that a square wave clock signal has the same jitter behavior as that of its base harmonic sinusoid signal. This reveals a fact that we can quantize the jitter of the clock signal through examining the phase modulation of its first harmonic sinusoid, which lays the foundation for measuring jitter in frequency domain. Since the phase noise is always small comparing to $\pi/2$, Eq. 4 can be approximated as

$$C(t) = A\sin(\omega_c t) + A\theta(t)\cos(\omega_c t) \qquad \text{Eq. 06}$$

Assuming that the jitter is a stationary random process, the mean square (MS) of the clock can be written as

$$\left\langle C(t)^2 \right\rangle = \frac{A^2}{2} + \frac{A^2}{2}\left\langle \theta(t)^2 \right\rangle \qquad \text{Eq. 07}$$

In frequency domain, we know that the sin and cos functions in Eq. (6) will generate tones at $-\omega c$ and ωc. Therefore, if we take the tones off the power spectrum of C(t), what left is the power spectrum of the phase noise, indicated by $P_\Theta(f-f_C)$, as shown in Fig. 5.

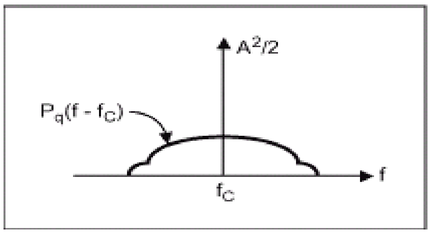

Figure 5. Power Spectrum of base Harmonic of a Clock Signal.

According to the Wiener-Khintchine theorem [5] we can obtain the MS of Θ (t) by integrating $P_{\Theta}(f - f_C)$ in frequency domain as

$$\langle \theta(t)^2 \rangle = \frac{4}{A^2} \int_0^{\infty} P_\theta(f)df \qquad \text{Eq. 08}$$

From Eq. (5), we can get the root of MS (RMS) of the period jitter J_{PER} by

$$\text{RMS of } J_{PER} = \frac{2}{A\omega_c} \sqrt{\int_0^{\infty} P_\theta(f)df} \qquad \text{Eq. 09}$$

Result shown in Eq. (9) is the essential equation used in measuring RMS jitter in frequency domain. Because of the relation of power spectrums of the clock signal and the phase noise, shown in Fig. 5, designers often use the compression (in dB) from the power of the tone to the envelope of the noise power spectrum at a certain frequency apart from fC to measure the quality of a clock signal.

Summary

This application serves two purposes. First, it described the jitter definitions and their relations. Then, it introduced the methods for measuring the RMS period jitter in both time and frequency domains, as well as the connection of the two approaches. In this note, we only briefly mentioned how to measure the cycle-to-cycle jitter and accumulated jitter in time domain, due to the fact that those jitters can only be done in high-end digital oscilloscope with specific software. For this regard, the interested readers can find more information from [2] and [3].

Reference

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