FREQUENTLY ASKED QUESTIONS (FAQ) ABOUT THE QS5919 AND TURBOCLOCK FAMILIES

APPLICATION NOTE AN-46

The following is a list of the most commonly asked questions about the Phase-Locked Loop (PLL) clock drivers. These answers provide a brief explanation to each question. More complete explanations to some of the questions in this application note are covered in separate notes. Please refer to our website for further information.

1. What is the propagation delay of the input clock when the PLL is in Test Mode?

Propagation delays can vary depending on the configuration of the PLL. The PROPAGATION DELAY table shows the typical values of the selected popular PLLs with different configurations. These values will change slightly depending on the variation of the supply voltage and ambient temperature. For propagation delays on Turboclocks, please refer to Application Note 45: Turboclock Test Mode.

2. What happens to the outputs if the input clock and/or the feedback signal are gated high, low, or are allowed to float (lost signal)?

The device makes no distinction between an input which is held (or gated) high or low, or left to float. All will be regarded as a zero frequency input by the phase/frequency detector. A number of possibilities exist, depending on whether the input clock or the feedback signal (or both) are gated or interrupted.

If the clock input signal is held high or low while the feedback signal remains connected to one of the package outputs, the VCO will slew down in frequency in an attempt to lock to zero frequency. Typical slew rates are given in the table below. For the Turboclock family, the VCO will eventually settle at a frequency below the specified minimum operating frequency for the FS setting. For the QS5919 family, the VCO will settle at a very low frequency and may even stop.

If the feedback signal is interrupted while the clock input signal remains valid, the VCO frequency will increase. Typical slew rates are given in the table below. The VCO will eventually stabilize at a frequency above the specified maximum operating frequency for the FS input.

Should both the clock and feedback signals be simultaneously held high or low, the response of the VCO is not predictable. It may slew quickly or slowly, either up or down in frequency, depending on the state of the phase/frequency detector at the time that these signals are lost.

PROPAGATION DELAYS(1)

Part Number	Propagation Delay		
	FS = LOW	FS = MID	FS = HIGH
QS5919	8ns	N/A	7ns
QS5919T	8ns	N/A	7ns
QS5LV919	10ns	N/A	8ns
QS5931	8ns	N/A	7ns
QS5931T	8ns	N/A	7ns
QS5LV931	10ns	N/A	8ns
59910A (TEST = Mid)	44ns	44ns	26ns
59920A (TEST = Mid)	44ns	44ns	26ns
59910A (TEST = High)	12ns	12ns	9ns
59920A (TEST = High)	12ns	12ns	9ns

NOTE:
1. Under nominal supply voltage and room temperature at 25°C.

TYPICAL SLEW RATES(1)

Part Number	Slew Rate		
	FS = LOW	FS = MID	FS = HIGH
QS5919	6.3MHz/us	N/A	12.7MHz/us
QS5919T	6.3MHz/us	N/A	12.7MHz/us
QS5LV919	5.5 - 11MHz/us	N/A	11-22MHz/us
QS5931	6.3MHz/us	N/A	12.7MHz/us
QS5931T	6.3MHz/us	N/A	12.7MHz/us
QS5LV931	5.5 - 11MHz/us	N/A	11-22MHz/us
5991A	4.5MHz/us	7.5MHz/us	12.2MHz/us
5992A	4.5MHz/us	7.5MHz/us	12.2MHz/us
5993A	4.5MHz/us	7.5MHz/us	12.2MHz/us
59910A	4.5MHz/us	7.5MHz/us	12.2MHz/us
59920A	4.3MHz/us	7.2MHz/us	11.7MHz/us
5V991A	4.3MHz/us	7.2MHz/us	11.7MHz/us

NOTE:
1. Under nominal supply voltage and room temperature at 25°C.

3. How long will the PLL take to lock, given the same frequency but different phase?

Assume the PLL has locked onto an incoming clock signal. If this incoming clock signal suddenly changes phase, but not frequency, then the phase/frequency detector may produce a "pump down" signal for the charge pump and pull current out of the loop filter (see figure 1). Because of the series resistor in the loop filter, the VCO control voltage suddenly steps down by a certain amount (depending on the pump current and resistor value), and therefore suddenly reduces the frequency of the VCO (depending on the gain of the VCO). This allows the input clock to accumulate phase faster than the output. At some number of clock cycles later, the phase error has reduced to zero and the VCO control voltage returns to its original value. The number of clock cycles it takes to reduce the phase error is much less than the time required for the loop filter capacitor to slew significantly. Therefore, the final VCO control voltage is very similar to the initial control voltage. The number of clock cycles it takes to re-lock depends on the frequency of the input and the amount of phase misalignment. For example, a QS5919 configured with 2xQ as the feedback, and with a 100MHz input clock, can re-align a 180° phase shift in around 20 clock cycles.

If the phase change results in the input clock's synchronizing edge to lead the feedback's synchronizing edge, then the VCO frequency will increase. The phase will re-align a number of clock cycles later and then return to its original frequency.

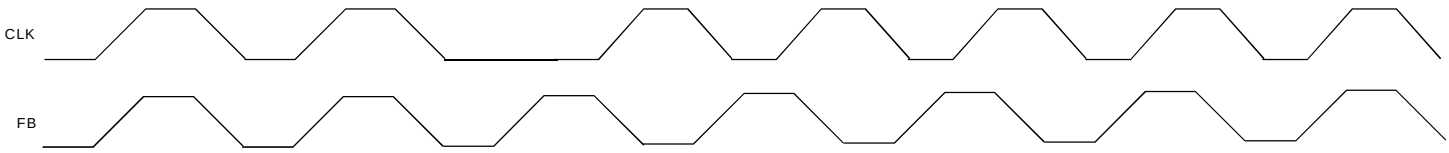

Figure 1. Example Phase Realignment of PLL

4. How does jitter at the input affect the output? Side effects when cascading PLLs?

Input jitter at certain frequencies can be a problem when cascading PLLs. The resulting jitter at the output can have little or no effect on system performance, or it can render the system completely unusable.

The magnitude of the closed-loop system response represents the jitter transfer characteristic of the system. The magnitude of this response exceeds unity (or 0dB) over some range of frequencies due to the closed-loop zero of the loop filter at a frequency lower than that of the poles. For the PLLs, the amount of peaking, and the frequency band at which this occurs, depends mainly on the loop filter characteristic and the configuration of the PLL. The effect of this peaking on cascaded PLLs is that any jitter in this spectrum will grow exponentially from one stage to the next. The –3dB closed-loop frequencies for PLLs in different configurations are shown in the LOOP FILTER CHARACTERISTIC FREQUENCIES table. Refer to figure 2 for the jitter transfer characteristic.

LOOP FILTER CHARACTERISTIC FREQUENCIES

Part Number	-3dB Frequency			Feedback
	FS = LOW	FS = MID	FS = HIGH	
QS5919/QS5919T QS5931/QS5931T	2.4MHz	N/A	4.6MHz	2xQ
	1.1MHz	N/A	2.4MHz	Q_0 - Q_5
	600kHz	N/A	1.1MHz	Q/2
QS5LV919/QS5LV931	4MHz	N/A	7.1MHz	2xQ
	2MHz	N/A	4MHz	Q_0 - Q_5
	1MHz	N/A	2MHz	Q/2
5991A/5992A 5993A/59910A	880kHz	1.5MHz	1.5MHz	3F0:1 = LL
	1.8MHz	3.2MHz	3.2MHz	3F0:1 = LM, LH, ML, MM, MH, HL, or HM
	500kHz	730kHz	770kHz	3F0:1 = HH
5V991A/5V993A	870kHz	1.4MHz	1.4MHz	3F0:1 = LL
	1.7MHz	3MHz	3.1MHz	3F0:1 = LM, LH, ML, MM, MH, HL, or HM
	430kHz	680kHz	720kHz	3F0:1 = HH

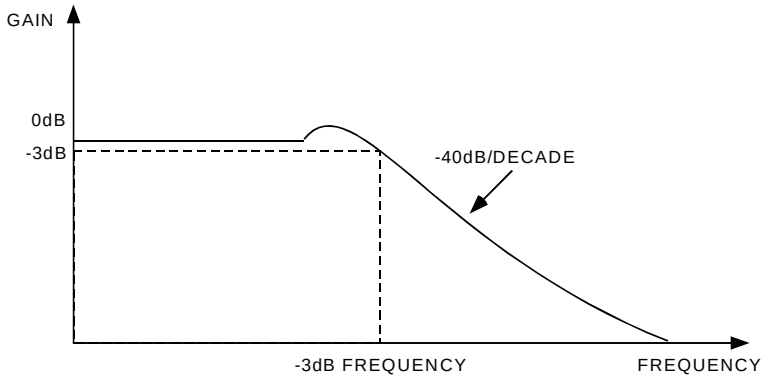

Figure 2. Jitter Transfer Characteristic

The frequency band at which the peaking occurs depends on the configuration of the PLL (i.e., feedback dividers, FS settings, etc.), since this changes the damping ratio and therefore moves the spacing between the zero (f2) and the lowest frequency pole (at a frequency lower than f3). As before, the effect of this peaking on cascaded PLLs is that any input jitter in this spectrum will grow exponentially from one stage to the next.

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