USING THE QS5919T/QS5931T PLL CLOCK DRIVERS

APPLICATION NOTE AN-227

INTRODUCTION

Designing high performance systems requires that attention be paid to details that were not important in older, slower designs. One of these details is the clock skew associated with such applications as clock distribution, clock synchronization, and clock generation. Skew can account for as much as 25% of the overall system timing budget if special care is not taken to minimize it. Using phase-locked loop (PLL) based clock drivers allow system designers to achieve maximum system performance by reducing clock skew to 350ps and lower.

The use of PLL clock drivers is relatively simple once the basics of the device are understood. This application note will describe the theory of operation behind PLL based clock drivers and provide information on the value added features of IDT's PLL based clock drivers. In addition, a detailed description of timing parameters and application examples for the QS5919T and the QS5931T will be included.

THEORY OF OPERATION

The function of a PLL based clock driver is to match the frequency and phase of the SYNC and feedback inputs. The feedback input can be supplied by one of the device outputs, thereby giving the PLL clock driver zero propagation delay. The QS5919T has 2 reference clock inputs, SYNC0 and SYNC1 which are selectable with the REF_SEL input. The QS5931T has a single clock input. The PLL matches the phase and frequency of the SYNC and feedback inputs by using the phase difference to speed up or slow down the VCO. A lowpass loop filter is used to stabilize the response of the VCO to phase differences. Loop filter design is critical to good jitter characteristics. Once the feedback and SYNC inputs have been matched, the lock output is asserted, signaling to the system that the PLL is locked to the incoming signal. The output of the VCO, which now matches the SYNC input, clocks output registers simultaneously to insure ultra low skew. The QS5919T and QS5931T both have an on-chip loop filter that improves jitter performance over a discrete resistor/capacitor network. The QS5919T , which is pin and functionally compatible with the Motorola 88915, can operate in sockets that already contain a discrete loop filter and maintain superior jitter characteristics. (Note: 47Ω decoupling resistors are not necessary and should be shorted.)

FIGURE 1: QS5919T BLOCK DIAGRAM

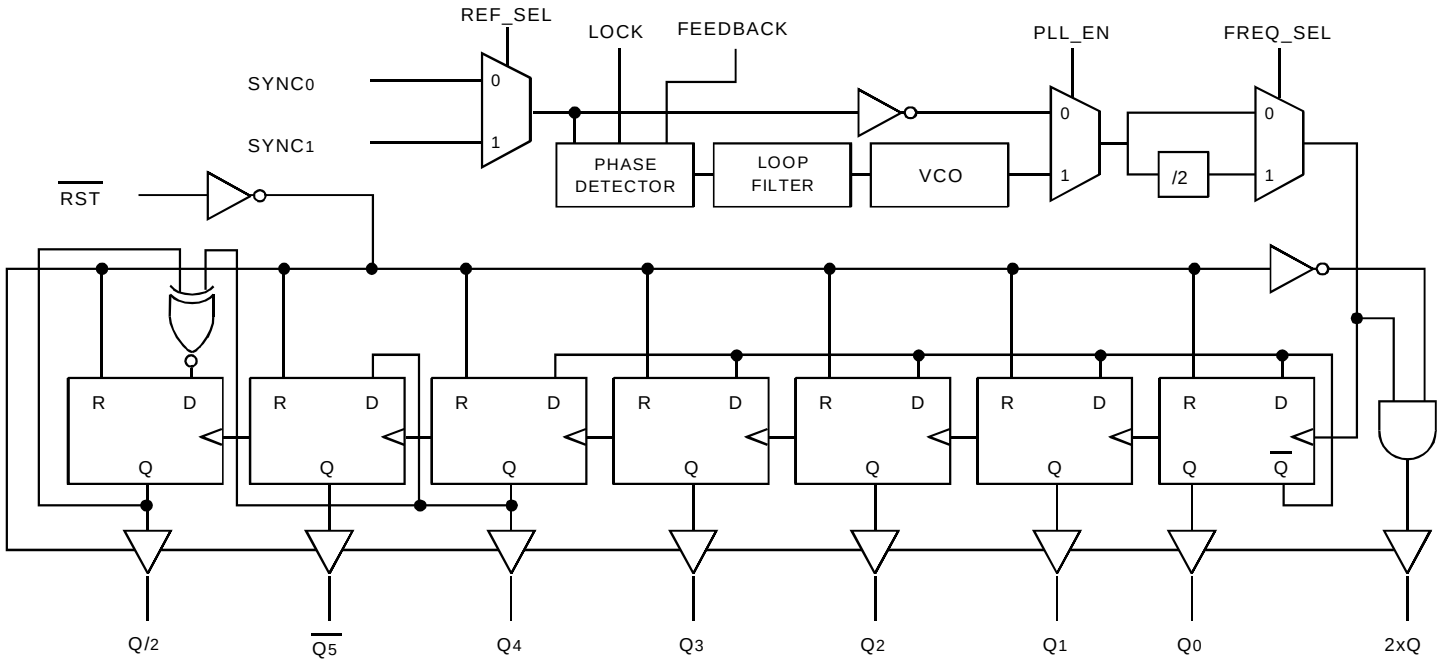

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Table 1 defines the relationship between the outputs and the inputs of the QS5919T PLL clock driver. Depending on the feedback path selected, the output frequency can range from one forth to four times the input frequency. It is important to note that with the frequency select input low, the VCO will run at twice the frequency of the 2xQ output. This allows the QS5919T device to operate over a wider range of input frequencies while still maintaining excellent jitter characteristics.

TABLE 1. INPUT TO OUTPUT FREQUENCY DEPENDENCE

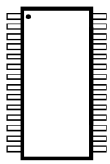
Input Frequency	Frequency Select	Feedback	Q/2 Output	Q Output	2xQ Output	Internal VCO Freq
f	0	Q/2	f	2xf	4xf	8xf
f	0	Q	f/2	f	2xf	4xf
f	0	2xQ	f/4	f/2	f	2xf
f	1	Q/2	f	2xf	4xf	4xf
f	1	Q	f/2	f	2xf	2xf
f	1	2xQ	f/4	f/2	f	f

VALUE ADDED FEATURES OF IDT'S PLL CLOCK DRIVERS

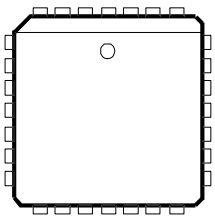
The QS5919T from IDT is a pin compatible replacement for the Motorola 88915 PLL clock driver. There are, however, some significant product enhancements that the IDT device has over competitive devices such as tri-stated outputs on reset, low noise TTL outputs, internal loop filter, and available QSOP packaging for the smallest possible footprint and lowest possible noise.

The outputs of the QS5919T tri-state during a reset cycle to reduce system noise and uncertainty. By tri-stating during reset, the outputs do not toggle uncontrollably, which reduces system noise due to switching and reduces the possibility for errors in other parts of the system caused by the unknown state of a resetting device.

To further reduce system noise and improve performance, the QS5919T and QS5931T offer low noise TTL compatible outputs. Since ground bounce noise induced by simultaneous output switching, is directly proportional to the output high level, TTL compatible outputs generate approximately 30% less noise than rail to rail outputs. In addition, the QS5919T and QS5931T are available in the IDT developed, industry standard QSOP. The QSOP package is 3.5 times smaller and approximately 20% quieter than the PLCC package. The combination of the TTL compatible outputs packaged in QSOP results in a reduction in ground bounce of approximately 45% over the equivalent rail to rail device in the PLCC package.



28-Pin
QSOP



28-Pin
PLCC

FIGURE 2. QS5919 T PACKAGING OPTIONS

TIMING PARAMETER DEFINITIONS

t_{PD} is the phase difference between the rising edges of the reference and feedback signals. The PLL aligns these signals to near zero. Because the PLL does not attempt to align the falling edges, t_{PD} only applies to the rising edges.

t_{SKr}, t_{SKf} define the window within which all outputs will switch.
t_{SKr} defines the skew of the rising edges of the outputs.
t_{SKf} defines the skew of the falling edges of the outputs.

t_J is the cycle to cycle variation of an individual output as shown below. While t_J defines jitter of an individual output, all outputs will jitter together (i.e. the skew window of all of the outputs will jitter). Output to output variation is defined by t_{SKr} and t_{SKf} as described above. t_J is only defined for the rising edges of the outputs.

The outputs of the QS5919T and QS5931T will maintain a nominal duty cycle of 50% independent of the duty cycle of the sync or feedback pin. If external circuitry is added in the feedback path to accomplish frequency dividing or multiplying, duty cycle asymmetry can be introduced. The duty cycle specification for the outputs is t_{PW}, or pulse width, which is defined as one half the cycle time ± 400ps. At 33MHz, this gives a worst case duty cycle of 51.3%/48.7%. At a 66MHz output cycle time, worst case duty cycle is 52.6%/47.4%.

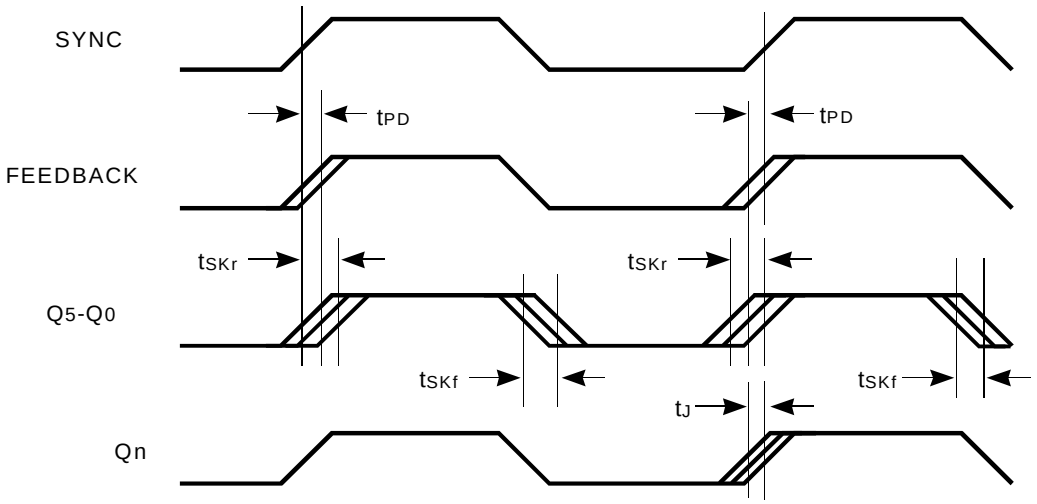


FIGURE 3. PLL CLOCK DRIVER TIMING WAVEFORMS

JITTER CHARACTERISTICS

The cycle to cycle variation of a single output is defined by jitter, t_J, which is the maximum window in which an output will vary. It is important to note that for low frequency operation, jitter performance can be improved on the QS5919T by holding the FREQ_SEL pin low. Some typical data of IDT's devices is shown in Table 2. The 250ps jitter has specification taken extreme temperature voltage supply, etc. into account. Some other factors affecting jitter are low input frequencies, and loop filter noise. The internal loop filters of the QS5919T and QS5931T allow significantly better jitter characteristics than conventional external filter circuits.

TABLE 2. TYPICAL JITTER OF QS59XX DEVICES

Output Frequency	Feedback Path	Output Measured	Measured Jitter	Spec (t_J)
132MHz	Q/2	2xQ	36ps	250ps
33MHz	Q5	Q5	46ps	250ps
16.6MHz	2xQ	Q5	92ps	250ps

* Input sync frequency = 33MHz

APPLICATION EXAMPLES

There are many applications in which a PLL clock driver is essential. Clock duplicating, clock generating, and clock phase shifting are the most common. By changing the length of the feedback path (through added trace delays, RC circuit, inverter chain, etc.), the output of the clock driver can be delayed or advanced with respect to the reference clock. In addition to phase shifting a clock, this also allows the user to compensate for transmission delays across a board or a backplane. When the delay in the feedback path matches the trace delay in the output path, the propagation delay from reference clock to destination is zero.

A PLL based clock driver can also be used as a clock generator with selectable frequencies. By placing an external divider or multiplier circuit in the feedback path, other multiples of the reference clock can be generated. In Figure 4, a preloadable 4-bit counter has been inserted into the feedback path of the clock driver. Using a single crystal oscillator for the reference clock and jumpers to select the preload value of the counter, sixteen different frequency values can be achieved using a single crystal oscillator.

Multiple copies of a clock can be generated with zero propagation delay by using several QS5805 fanout buffers in conjunction with the QS5919T or QS5931T PLL clock driver. This can be accomplished by connecting the Q outputs of the PLL clock driver to the inputs of the QS5805 devices as shown in Figure 5. By connecting one of the QS5805 outputs to the feedback input of the PLL clock driver, the propagation delay from the clock source to outputs of the QS5805 devices is reduced to zero.

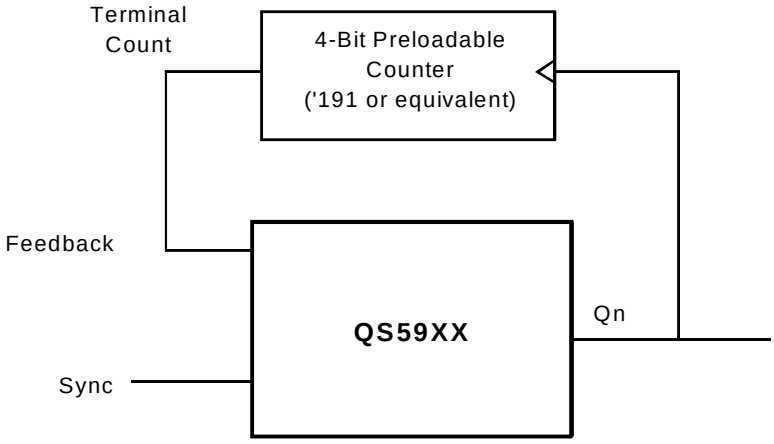


FIGURE 4. CLOCK GENERATION USING A PLL CLOCK DRIVER

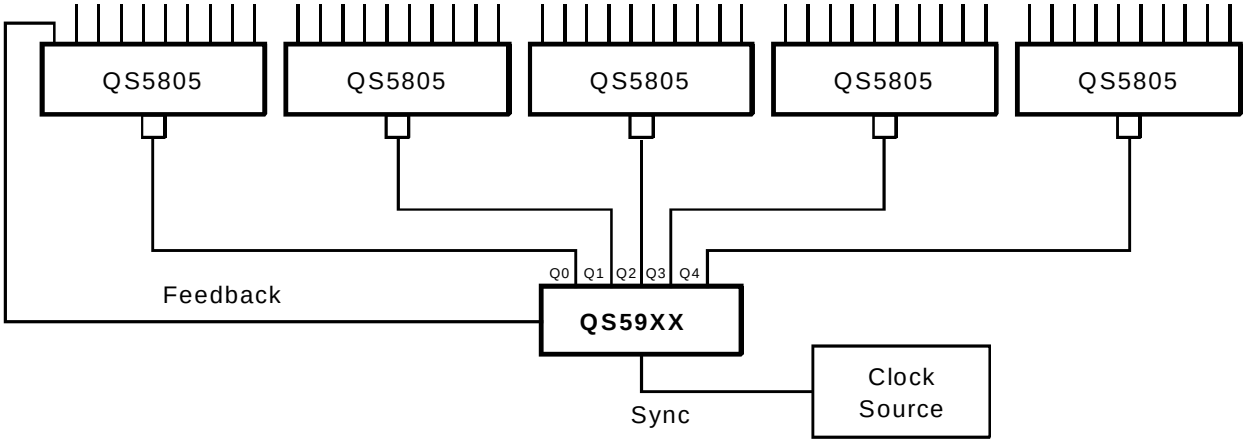


FIGURE 5. MULTIPLE ZERO PROPAGATION DELAY CLOCKS

PLL-based clock drivers such as the QS5919T and QS5931T can be used to distribute clocks across backplanes in larger systems. As shown in Figure 6, the devices can be implemented such that there is no propagation delay difference between the system clock and the point of distribution across a board or a backplane. Additionally, as shown in Figure 7, the clock can be distributed across the backplane at one half the system clock frequency to reduce system noise and EMI. At the destination board, the clock can be increased back up to the system clock frequency by feeding back the Q/2 output.

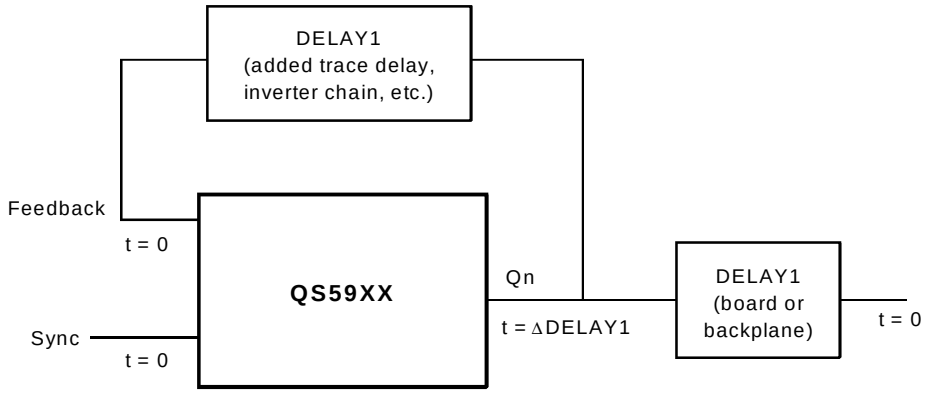


FIGURE 6. CLOCK DUPLICATING ACROSS BOARD OR BACKPLANE

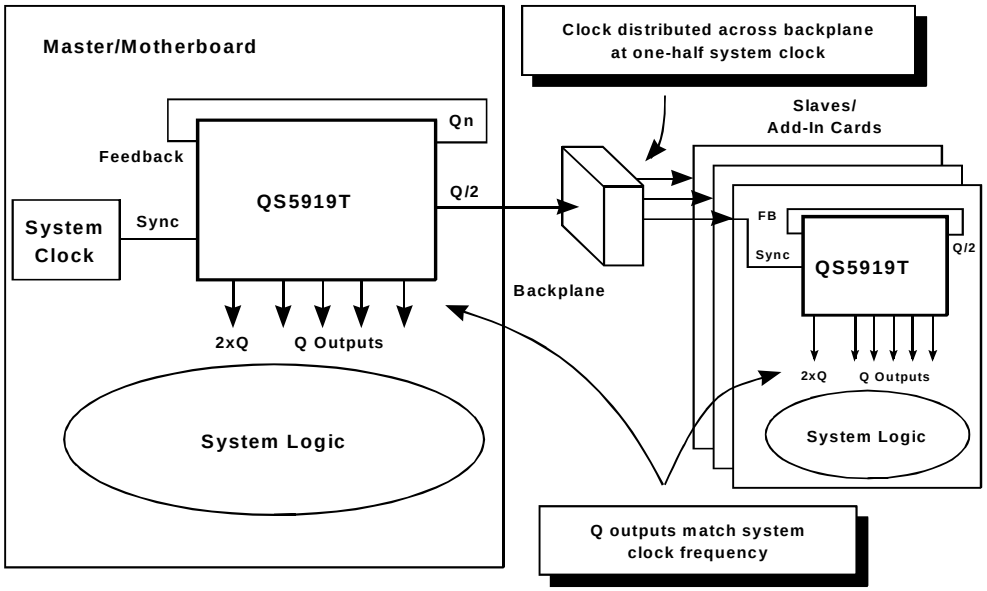


FIGURE 7. CLOCK DISTRIBUTION IN MULTI-BOARD SYSTEMS

CONCLUSION

Value-added features of IDT PLL clock drivers such as TTL output levels and QSOP packaging reduce system noise and improve system density. The QS5919T and QS5931T incorporate an on chip loop filter to improve jitter performance and eliminate the need for external components. Furthermore, the QS5919T PLL clock driver from IDT is a pin compatible replacement for the Motorola 88915 in a variety of applications. PLL based clock drivers from IDT enable system designers to achieve maximum performance from high-end designs.

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