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National Semiconductor® NEWS RELEASE

NATIONAL ANNOUNCES FIRST IMPLEMENTATION OF NEW IEEE AND TIA LVDS (LOW VOLTAGE DIFFERENTIAL SIGNAL) STANDARD

SANTA CLARA, Calif., February 13, 1995-- National Semiconductor today announced the immediate availability of the DS90C031TM LVDS Quad CMOS Differential Line Driver and the DS90C032TM LVDS Quad CMOS Differential Line Receiver. These new differential line drivers/receivers are the first discrete implementations of the new IEEE (Institute for Electrical and Electronics Engineering) 1596.3 SCI (Scalable Coherent Interface) LVDS and TIA (Telecommunication Industry Association) LVDS proposed standards. These standards define the electrical specification for this new high speed/low power physical layer interface. The IEEE 1596.3 SCI LVDS standard goes further and defines the data encoding used in packet switching for SCI data transfers.

"This standard was developed over the last three years with extensive feedback and discussion from some of the largest manufacturers of data communications, telecom, computing and networking systems," points out Stephen Kempainen, chair of the IEEE 1596.3 working committee. "It was driven by the needs of a wide range of applications for far greater data bandwidth than current approaches permit within the increasingly constrained power consumption limitations of most equipment. It has been clear for years that what was needed was a new industry-wide standard of physical data transmission that would exceed current ECL-type data rates but would consume a fraction of the power."

This need has been addressed by the IEEE 1596.3 SCI LVDS standard that passed ballot in March 1994. In the interest of promoting a wider standard, no specific process technology, media or power supply voltages are defined. This means that LVDS can be implemented in CMOS, GaAs or other applicable technologies. Formalization of the standard is expected in the first half of 1995.

"National chose to implement its first LVDS products in high performance 5 Volt CMOS," says Mitch Abbey, product launch manager for the LVDS interface products within the Data Management Division at National Semiconductor, "because it provides excellent performance in a low cost, low power implementation, and it will lead to an easy migration path for 3.3-V or even 2.5-V implementations in the future. While LVDS will first be compared to RS-422 and PECL type devices, it will open up entirely new applications and be widely used, as compared to the limited, niche-market utilization of PECL. This is because the combination of very high speeds with low power consumption solves some very real needs of today’s power-limited system manufacturers."

In design applications, the DS90C031TM/DS90C032TM can be used as replacements for standard RS-422 26C31/32 drivers/receivers and PECL 41LL-1LF devices. The one difference for PECL replacement is that the LVDS drivers/receivers need only a single 100 ohm termination resistor as opposed to the three termination resistors commonly required by the PECL drivers.

"Using LVDS, power is saved in several important ways," says Mitch Abbey. "The power dissipated by the load (the 100 ohm termination resistor) is a mere 1.2 mW. In comparison, a RS-422 driver typically delivers 3 V across a 100 ohm termination or 90 mW. Likewise, the LVDS devices require roughly one-tenth the power of PECL/ECL devices. We believe that the many advantages of LVDS technology make it likely that it will become the next data transmission standard for 100 Mbps and greater data rates, superseding the 20 kbs to 10 Mbps rates of the RS-232, RS-422 and RS-485 standards."

Mr. Kempainen agrees, "System designers are hungry for high speed without the power demands of PECL. LVDS offers the ideal solution for today and an established framework for future high speed products. At National, we are now supporting the IEEE and TIA standards with the DS90C031TM/DS90C032TMdriver/receiver pair, but in the near future we will apply LVDS technology in a number of different standard application-specific products and ASIC library. While the DS90C031TM/DS90C032TM are point-to-point drivers/receivers with 155.5 Mbps data rates, the LVDS standard can be applied in a number of peer-to-peer networking applications as well, with much higher theoretical data rates.

We will be pursuing applications areas such as telecommunications equipment, networking systems, high speed computers, multimedia applications, and many others during the next 12-18 months."

THE LVDS TECHNOLOGY

The key to LVDS technology is the use of a differential data-transmission scheme. Instead of measuring a precise voltage level for a one or a zero, this method measures the voltage differential or swing between the driver/outputs. The scheme provides for outstanding common mode noise immunity. Any noise introduced into the medium is seen as common mode modulations by the receivers and is rejected. The receivers respond only to differential voltages. In order to achieve very high data rates, LVDS uses reduced signal levels and signal swings as compared to older technologies. The following diagram shows the LVDS signal swings compared to PECL swings. LVDS signaling levels are 50 percent smaller than PECL levels, enabling faster switching and lowering EMI emissions.

LVDS addresses all areas of concern for most high data-rate applications, most notably: raw speed, ultra low power dissipation, reliable data transmission, and low noise emissions. LVDS uses a low voltage differential swing of only 345 mV(typ) that corresponds to a mere 1.2 mW load power dissipation. Further, its CMOS current mode driver design greatly reduces quiescent power supply requirements. The CMOS process used in the DS90C031TM/DS90C032TM LVDS Drivers/Receivers provides an ultra low power static current. The current mode design provides for a very flat increase in active current as the input frequency increases.

The following chart highlights the differences between LVDS, RS-422 and PECL signal levels. The important specification is that differential driver output voltage is only 1 250 - 450 mV (versus 12V for RS-422 and 1600-800 mV for PECL) and the receiver input threshold is only 1100 mV (versus 1200 mV for RS-422 and 1200-300 mV for PECL). The advantages of this approach are a significant gain in signal switching speed, and reduced EMI (electromagnetic interference).

PARAMETER	RS-422	PECL	LVDS
Differential Driver Output Voltage	+ 2.0 V	+ 600-800 mV	+ 250-450 mV
Receiver Input Threshold	+ 200 mV	+ 200-300 mV	+ 100 mV
Data Rate	5 MHz (10 Mbps)	65 Mhz	> 65 MHz
Supply Current Driver	500 A (26C31)	32-65 mA (Max.)	3.0 mA
(no load)	60 mA (26LS31)	.	.
Prop. Delay of Driver	11 ns (Max.)	4.5 ns (Max.)	3.0 ns (Max.)
Prop. Delay of Receiver	30 ns (Max.)	7.0 ns (Max.)	5.0 ns (Max.)
Supply Current/Receiver	23 mA (Max.)	40 mA (Max.)	10 mA (Max.)
Skew (Driver or Receiver)	.	500 ps	400 ps
Max Cable Length	20 m @ 10 Mbps	7-10 m	> 10 m

While the DS90C031TM/DS90C032TM Driver/Receivers are the first discrete implementations of the LVDS technology, National has also implemented LVDS into its QuickRing QR0001 Data Stream Controller. This 160-pin device acts as a virtual backplane for high-speed network hubs or routers, providing very high speed point-to- point data stream connections. It is used in a wide variety of applications including ATM switches, video delivery and editing systems, multiprocessing systems, DSP subsystems and image processing subsystems.

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National Semiconductor is ISO 9000 certified.

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