CERN - MICROELECTRONICS GROUP

PHOS4 – 4 Channel delay generation ASIC with 1ns resolution

Datasheet

Purpose

The purpose of the ASIC is to provide 4 calibrated delay lines for digital signals, which can be programmed independently via an I2C interface. One of 25 delay taps, spaced 1ns apart, can be chosen for each of the 4 signal channels and the clock channel. The chip requires a 40 MHz clock as timing reference.

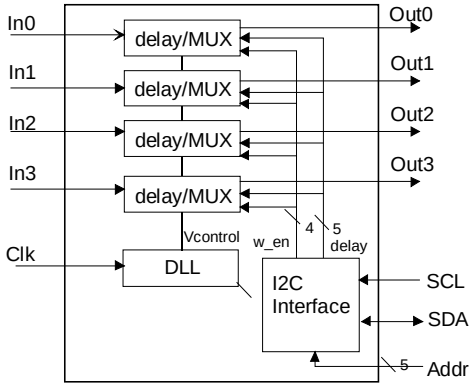
Architecture

The device contains a delay locked loop (DLL) to provide the reference control voltage for the four independent delay units. The delay units have the same layout as the DLL in order to achieve identical electrical properties in both the reference delay unit (=DLL) and in the signal delay units.

Technology

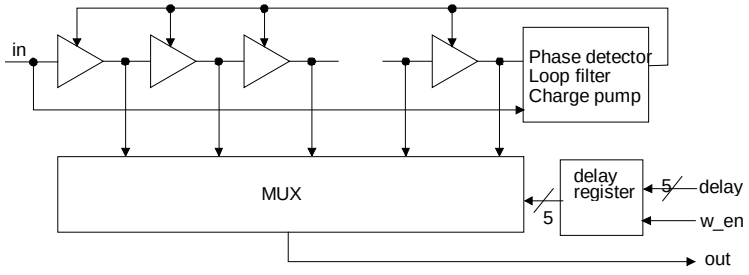
0.8 μm CMOS, AMS CYB

Functional Block diagram



Delay-locked loop and delay-lines

The DLL consists of a multi-stage variable delay line, a phase detector and a loop filter. The DLL uses a starved inverter design to incorporate a variable delay element, a phase comparator, a charge pump and a loop filter. The delay lines consist of 25 delay stages. A 25:1 multiplexing stage follows the delay-line elements. The delay value is stored in a five bit register connected to the multiplexer. In order to mirror the electrical properties of the DLL in the delay elements and vice versa, the DLL is connected to a dummy multiplexer.



I2C-Bus interface

The values of the delay-registers can be read written over the I2C-bus interface. The I2C interface uses the external signals SCL and SDA for data transfer. Of the seven device address bits (A6-A0) four bits (A5-A2) correspond to the hard-wired device address, while A6 is supposed to be zero and A1 and A0 are ignored. The data word is divided into two sections, the upper three bits (S2-S0) select one of the delay channels, the lower five bits specify the delay or are used to set the output to zero or one. (See following tables.)

A write-cycle has the following format:

S	A6	A5	A4	A3	A2	A1	A0	0	A	S2	S1	S0	D4	D3	D2	D1	D0	NA	P

S: Start condition (see [1])

A6 : MSB of device address, must be 0

A5-A2: 4 bit device address, defined by pins A5-A2.

A1-A0: lower bits of device address, ignored

A: Acknowledge cycle

D4-D0: 5 bit delay data:

D4-D0 value	Significance
0-24	Delay in ns
25	Constant 0 at output
26	Phase detector output (for test purposes)
27	Constant 1 at output

S2-S0: 3 bit device select:

S2-S0 value	Significance
0	Delay channel 0
1	Delay channel 1
2	Delay channel 2
3	Delay channel 3
4	CLK channel

NA: “Not Acknowledge” cycle

P: Stop condition

Example

To program a delay value of 15 nanoseconds on delay channel 3, the data byte which has to be transmitted calculates to 2*32+15=79. For setting the output of the clock channel to zero the data byte to be transmitted is 4*32+25=153.

Reset procedure

Since the chip does not have a reset signal, it has to be generated from the I2C interface. The first negative transition on the I2C clock line is used to trigger the reset procedure. Therefore, the first data transmission will not have any effect on the delay registers. It is to note that the clock has to be active during reset. Before a reset, or if there is no clock at the corresponding input, the chip can go into a state where current consumption is relatively high, i.e. >30mA. Therefore it is recommended to reset the chip immediately after power-up with an arbitrary transmission on the I2C bus, i.e. not necessarily addressing any of the chips on the bus.

External signals

- GND Ground
- VDD: 3.3 V supply (nominal)
- CLK (input): 40 MHz external clock signal
- DI<3:0>(input): Digital input signals
- DO<3:0>(output): Delayed digital output signals
- SDA (bidirectional): I2C-Data
- SCL (input): I2C-Clock
- A<6:3> (input): Upper four bits of I2C-Address

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	3.0	3.3*	3.6	V
V_{IH}	High-level Input voltage	2.0			V
V_{IL}	Low-level Input voltage			0.8	V
T_A	Operation free-air temperature	-20	25	75	°C
t_{rf}	Input transition rise or fall time		2	5	ns
C_L	Capacitive load at output		15	50	pF
I_L	Continuous output current			4	mA

absolute maximum ratings over operating free-air temperature range

	MIN	MAX	UNIT
Supply voltage, V_{DD}	0	5.5	V
Input voltage range	0	V_{DD}+0.5	V
Continuous output current, I_L		10	mA

Current consumption

		MIN	NOM	MAX	UNIT
P_0	DC bias current @ 40 Mhz	2	5	10	mA
P_{ch0}	Current/channel, output sw. off, 40Mhz	1	2	4	mA
P_{ch}	Current/channel, 15pF total load, 40 MHz	3	4	6	mA
P_{ch}/f	Current/channel/Mhz , 15 pF total load		0.1		mA

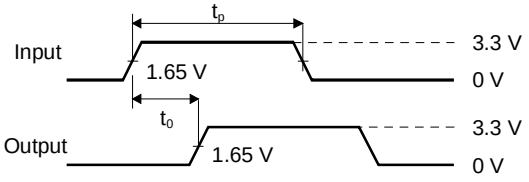
The overall current consumption is calculated by adding up the DC bias current to the currents in the active channels. If, for example, the clock output is switched off, and one channel has a mean transition frequency of 2 Mhz, then the total current calculates to $P_0 + P_{ch0} + 2\ P_{ch}/f = 7.2$ mA (with a total load of 15pF, no DC current, 40 Mhz input clock, nominal case).

* Although a higher supply voltage, e.g. 4V can be used, correct operation is not guaranteed with a reference clock of 40 Mhz and has to be tested individually. The same applies for supply voltages less than 3.0 V, and for reference clock frequencies different from the nominal case of 40 Mhz. The general trend is that higher clock frequencies require higher supply voltages.

Timing requirements

		MIN	NOM	MAX	UNIT
t_ϕ	Clock cycle time		25		ns
t_p	Pulse width in signal channels 0-3	3			ns

For timing on I2C signals SDA, SCL see [1].

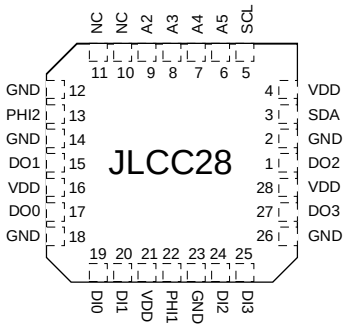


timing characteristics

		MIN	NOM	MAX	UNIT
t_0	minimum signal delay (tap 0)	8	10.5	14	ns
Δt	delay step, t_ϕ=25ns	0.92	1	1.08	ns
$\sigma_{\Delta t}$	differential non-linearity rms		26		ps
t_{e0}	integral non-linearity, Channel 0 and 3		500		ps
t_{e1}	integral non-linearity, Channel 1 and 2		250		ps
σ_t	output clock jitter (max. @ tap 24)	25		50	ps

Pin assignment

Order	Name	Description
1	DO2	data_out 2
2	GND	ground
3	SDA	I2C data
4	VDD	supply 3.3V
5	SCL	I2C clock
6	A5	I2C address
7	A4	I2C address
8	A3	I2C address
9	A2	I2C address
10	NC	not connected
11	NC	not connected
12	GND	ground
13	PHI2	clock output
14	GND	ground
15	DO1	data_out 1
16	VDD	supply 3.3 V
17	DO0	data_out 0
18	GND	ground
19	DI0	data_in 0
20	DI1	data_in 1
21	VDD	supply 3.3 V
22	PHI1	clock input
23	GND	ground
24	DI2	data_in 2
25	DI3	data_in 3
26	GND	ground
27	DO3	data_out 3
28	VDD	supply 3.3V



References

[1] Signetics I2C-bus specifications, January 1992