IMPORTANT NOTICE

This is what the new PHOS4s really look like!!

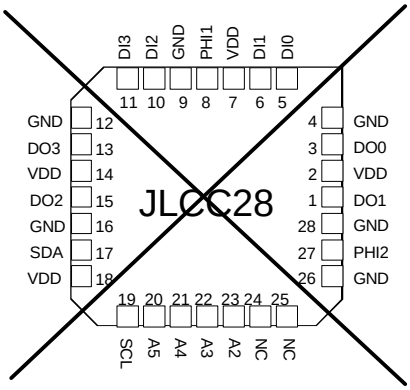
The packaging of the latest batch of PHOS4s received in Spring 2000 is not as expected from the drawings in Delaychip SpecsV1_2b.doc

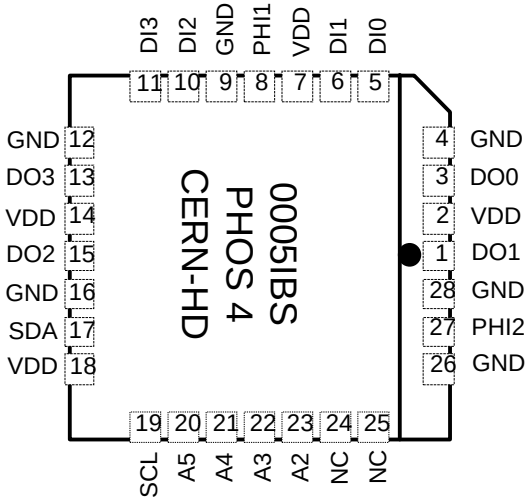
The problem is that the package has one bevelled corner, rather than the three expected, which makes the correct orientation hard to determine.

The Cambridge Group checked the pinout by probing Ground and Power pins. Martin Morrissey @RAL has confirmed our conclusions by testing 4 of the devices.

The following shows the correct package diagram, together with the (unchanged) table of pin assignations:

Pin #	Name	Description
15	DO2	data_out 2
16	GND	ground
17	SDA	I2C data
18	VDD	supply 3.3V
19	SCL	I2C clock
20	A5	I2C address
21	A4	I2C address
22	A3	I2C address
23	A2	I2C address
24	NC	not connected
25	NC	not connected
26	GND	ground
27	PHI2	clock output
28	GND	ground
1	DO1	data_out 1
2	VDD	supply 3.3 V
3	DO0	data_out 0
4	GND	ground
5	DI0	data_in 0
6	DI1	data_in 1
7	VDD	supply 3.3 V
8	PHI1	clock input
9	GND	ground
10	DI2	data_in 2
11	DI3	data_in 3
12	GND	ground
13	DO3	data_out 3
14	VDD	supply 3.3V





This is how it is