

APPLICATION NOTE

AN243

**LVT (Low Voltage Technology) and
ALVT (Advanced LVT)**

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1 INTRODUCTION

Philips Semiconductors has introduced two low voltage families optimized for backplane driving applications: LVT (Low Voltage Technology) and ALVT (Advanced LVT). The purpose of this note is to provide better insight into both families for optimal use by designers in their applications.

New circuit techniques have been pioneered that give LVT and ALVT their unique properties, some of which will be discussed in detail.

Both families are fabricated using QUBiC, an advanced BiCMOS process, where the best properties of bipolar transistors ($f_T=17\text{GHz}$) are combined with optimized CMOS ($0.65 - 0.8 \mu$). In addition, special components can be built in such as Schottky diodes and zener diodes for specific requirements. QUBiC processing enables extremely short propagation delay times combined with low power dissipation, low noise and high output drive. The process also allows very low temperature dependency of AC and DC characteristics.

The excellent properties available in the world's first Advanced BiCMOS family, Philips Semiconductors' 5V ABT family, are now taken to even greater heights in LVT and ALVT.

2 APPLICATION REQUIREMENTS FOR LVT AND ALVT

Both LVT and ALVT families are intended primarily for fast low voltage bus driver applications, especially driving low bus impedances such as backplanes. For this range of applications a number of parameters are important such as operating voltage range, propagation delay, drive capability and power dissipation (see Table 1). Other important factors, discussed below, are power-up/down characteristics, 5Volt input and output capability, bus hold and ground bounce.

ALVT is different from LVT in two ways. First ALVT is fully specified at $V_{CC} = 2.5\text{V}$, and second, it is about 40% faster than LVT. It is the fastest TTL family available: shorter propagation delays do not exist in other 5V or 3V TTL families.

Due to the trade-off between speed and ground bounce, ALVT has only Multibyte™ products with multiple GND and V_{CC} pins (flow-through architecture). Having the same speed in a standard pinning 8 bit device would require the speed to be tuned down to a level comparable to LVT. As a result, LVT has a much wider product portfolio with a variety of 8 to 10-bit bus functions and also some very fast, lower drive gates and flip-flops. Both families have versions with built-in damping resistors (for example, '2244 or '162244) to minimize undershoot, especially for driving memories.

Table 1. Basic Properties of LVT and ALVT

PARAMETER	LVT	ALVT		UNIT
		3.3V range	2.5V range	
Supply voltage	2.7–3.6	2.7–3.6	2.3–2.7	V
Input voltage	5.5			V
Output current	–32/64		–8/24	mA
Drive capability	35		75	Ω
Quiescent current	70		40	μA
Propagation delay	2.5 4.2	1.5 2.4	1.8 3.5	ns
Product portfolio Gates/Flip-flop 8-bit bus driver 16-bit bus driver	✓ ✓ ✓	✓		

3 DETAILS OF THE INTERNAL CIRCUIT

Figure 1 gives a simplified version of the internal buffer circuit, with the output enable function (\overline{OE}) and other details (some of which will be discussed later) omitted. Its purpose is to show the basic aspects of the internal circuit so that applying LVT circuits is made easier and certain aspects of the datasheet are clarified.

The input uses a small CMOS inverter stage with a low input capacitance, so no drive energy is needed. The output LOW is bipolar (Q4) with a small (M7) in parallel, and the output HIGH is a combination of a bipolar transistor (Q2) and PMOS (M4) to pull the output to the full V_{CC} .

Bipolar transistors introduce less bounce than pure CMOS. The NMOS M7 is very small and therefore does not affect ground bounce. The PMOS transistor M4 is delayed via the inverters INV1/INV2 so that it becomes active somewhat later than Q2 with only a minimal effect on V_{CC} bounce. This smart construction enables the best possible trade-off between speed and bounce.

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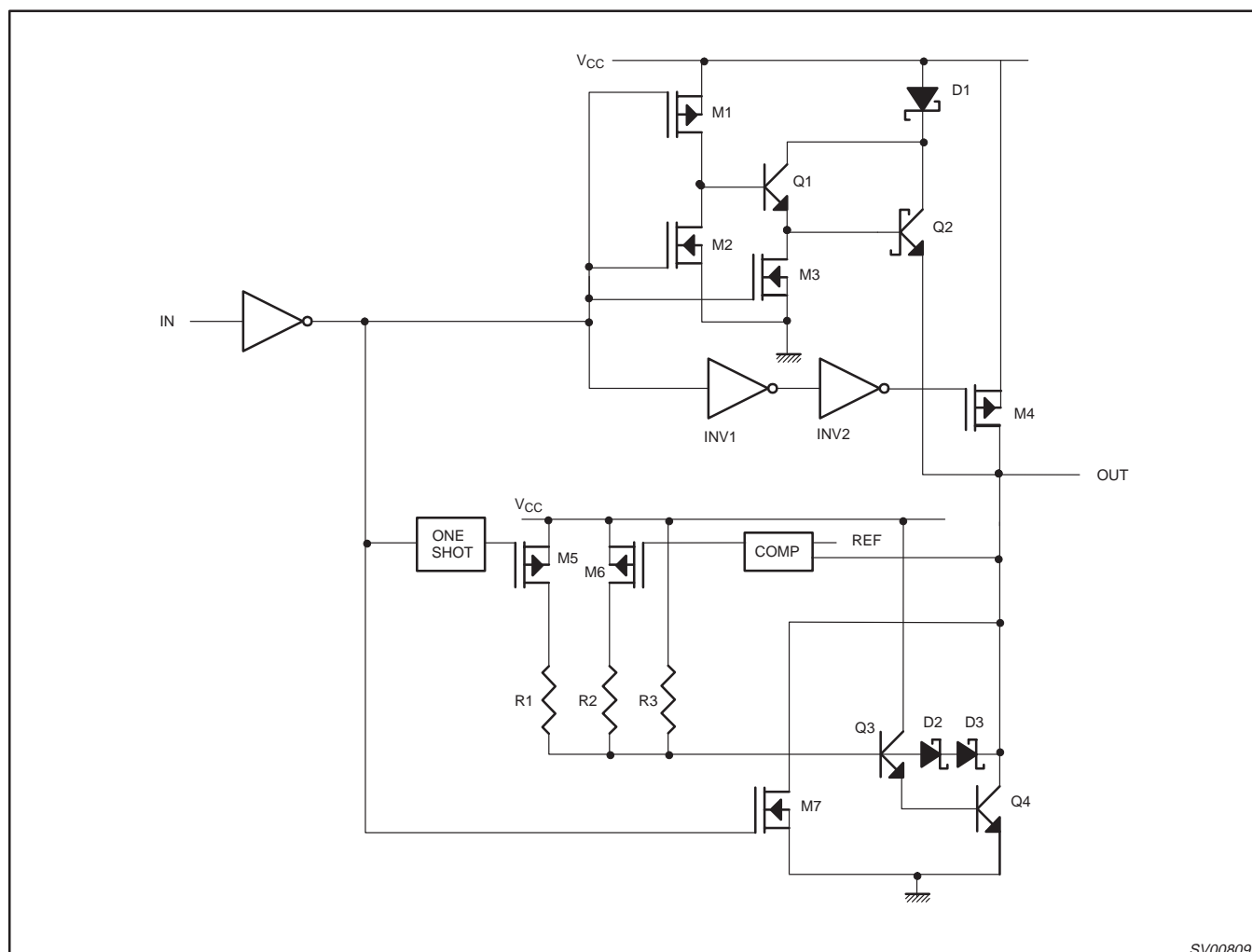


Figure 1. Simplified LVT/ALVT circuit

The drive of Q2 in the active HIGH state, taken care of by M1, M2 and Q1, is standard for advanced BiCMOS and makes optimum use of MOS and bipolar transistors to get the fastest, lowest internal capacitance inverter.

M3 ensures a fast turn-off of Q2 when the output goes LOW or into 3-state. When the output is forced LOW, a 'power-on-demand' circuit is activated. A one shot delivers Q4 with a high base current (via M5, R1 and Q3), which will quickly pull the output low. Additional base current is provided via M6/R2 and R3. The path M6/R2 is connected to the output voltage via a very fast comparator. When the output drops lower than approximately 1V, the current path via M6/R2 is blocked. The diodes D2/D3 prevent deep saturation of Q4 to enable quick turn-off.

This, at first sight, rather complex circuit ensures a very fast transition to around 1V, and below that value the output voltage smooths out somewhat so that the amount of ringing generated is kept to a minimum. Also, when the output is active LOW, a very low current is drained from the supply voltage. When a glitch appears on the output trying to pull the output HIGH, the diodes D2/D3 stop conducting, providing base current into Q3/Q4 so that the bus is pulled LOW again. This structure provides an excellent dynamic behavior, little ringing and good glitch suppression combined with low power dissipation.

When the output is in 3-state or active HIGH, only a small bias current flows (for the power-up/down circuit discussed in Section 3.1) while in the active LOW state some current flows via R3, which may vary somewhat among part types. Therefore I_{CCH} and I_{CCZ} are low, while I_{CCL} is somewhat higher.

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3.1 Powering-up/Powering-down

LVT and ALVT have a feature that is useful for live insertion and removal. A circuit is built into these families that monitors the supply voltage and ensures that the output is forced to a 3-state mode when V_{CC} is lower than 1.2V. Then, the transistor does not conduct and the external \overline{OE} signal is overruled and the output goes into 3-state mode. Normally, when removing a board in a live system, the power supply is removed first and high currents into the output circuit are prevented.

Above 1.2V the transistor will start to conduct and the part may again become active (i.e., the external \overline{OE} enables the output). It's the task of the system designer to ensure that an external circuit forces the correct \overline{OE} signal when V_{CC} is higher than 1.2V.

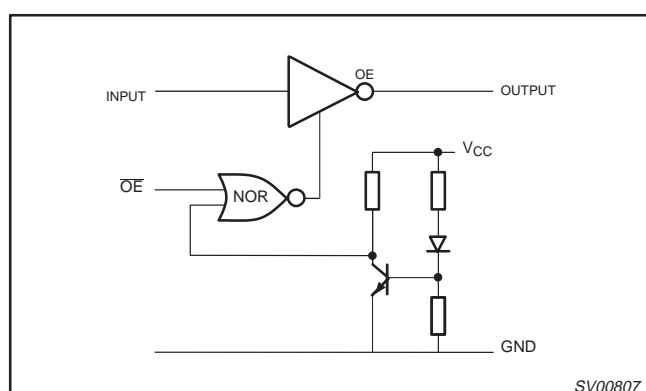


Figure 2. Power-up state

3.2 Bus Hold

All LVT and ALVT products have integrated bus hold inputs. A bus hold circuit allows CMOS input pins to be left open: the input is always defined to be LOW or HIGH via the small MOS transistors that serve as dynamic pull-up or pull-down resistors.

To allow 5V on the inputs, a Schottky diode is inserted between input and the PMOS transistor, blocking any current V_{CC} , even when the part is powered down.

For more information about bus hold circuits, see Reference #1.

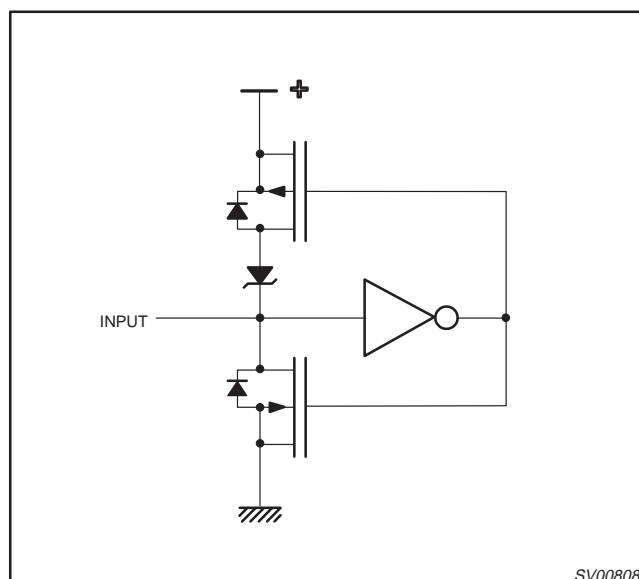


Figure 3. Bus Hold circuit

3.3 Interfacing with 5V systems

Special measures have been taken to allow easy interfacing with existing 5V systems. First, the input circuits are designed without a diode to V_{CC} so that all inputs are 5V tolerant.

For outputs on shared busses there may be a problem with the diode normally existing between drain and backgate/source of the pull-up PMOS (M4 in Figure 1). This diode current path has been blocked by replacing the normal short circuit between source and backgate with a Schottky diode (see Figure 4).

Also, special output overvoltage protection has been implemented. The output voltage is compared to V_{CC} , and when the output is approximately 0.4 to 0.5V higher than V_{CC} the output is automatically put into 3-state. In this way an overvoltage on the output will not lead to high currents from output to V_{CC} , and the device is fully protected.

The current flowing into the output for our parts and competitors' products is given in Figure 5. Above $V_{CC} + 0.5V$, LVT and ALVT interrupt the current from the output to V_{CC} . It should be noted that typically 20 to 30 mA must be delivered into the output before the overvoltage protection is activated.

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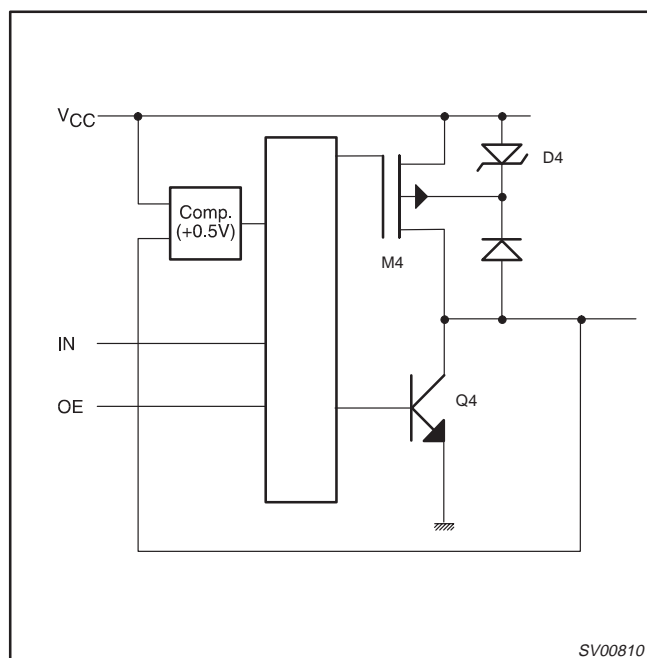


Figure 4. 5V tolerant output

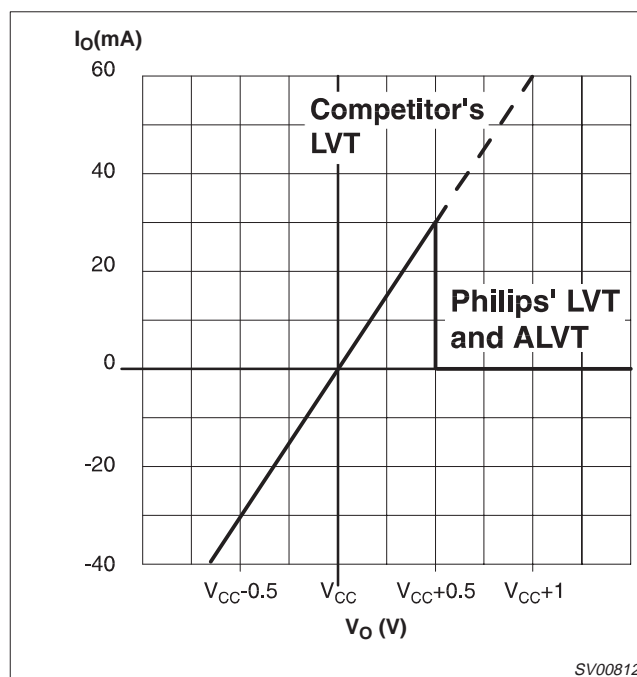


Figure 5. Output current with $V_O > V_{CC}$

More information about interfacing between 3V and 5V systems is available in an Application Note AN240 (Reference #2).

It should be noted that the 5V tolerant features built into LVT and ALVT also play a role during powering-up or-down, since they prevent any current to flow into the output pins when powered-down.

4 SPECIAL INFORMATION

The LVT and ALVT datasheets give characteristics of certain special properties that are unique for both families.

Table 2. Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS	T _{amb} (°C) −40 to +85			UNIT
			MIN	TYP	MAX	
V _{RST}	Power-up output LOW voltage	V _{CC} = 3.6V; I _O = 1 mA; V _I = GND or V _{CC}	−	−	0.55	V
I _{OFF}	Output OFF current	V _{CC} = 0V; V _I or V _O = 0 to 4.5V	−	−	± 100	μA
I _{HOLD}	Bus hold current A or B outputs	V _{CC} = 3.0V; V _I = 0.8V	75	−	−	μA
		V _{CC} = 3.0V; V _I = 2.0V	−75	−	−	
I _{EX}	Current into an output in the HIGH state when V _O > V _{CC}	V _{CC} = 3.0V; V _O = 5.5V	−	−	125	μA
I _{CCH}	Quiescent supply current	V _{CC} = 3.6V, outputs HIGH. V _I = V _{CC} or GND; I _O = 0	−	−	0.12	mA
I _{CCL}		V _{CC} = 3.6V, outputs LOW. V _I = V _{CC} or GND; I _O = 0	−	−	6	
I _{CCZ}		V _{CC} = 3.6V, outputs disabled. V _I = V _{CC} or GND; I _O = 0	−	−	0.12	
I _{PU/PD}	Power-up/down 3-State output current	V _{CC} ≤ 1.2V; V _O = 0.5V to V _{CC} ; V _I = GND or V _{CC} ; OE/OE̅ = don't care	−	−	± 100	μA

V_{RST} Applies to parts with storage cells. When all outputs are LOW and V_{CC} is made zero, after power-up the outputs are still LOW.

I_{OFF} Specifies the current flowing into the output when the supply voltage is zero (power-down mode). The output may even be pulled to higher voltages than the nominal V_{CC}.

I_{HOLD} Bus hold current at the TTL input levels.

I_{EX} Gives the current into the output when the output is pulled to a voltage higher than V_{CC}. Useful for mixed mode 2.5/3.3/5V applications.

I_{CCH} When the output is high, a current is still drawn from the supply for the automatic 3-state circuit (see Section 3).

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I_{CCL} I_{CCL} is higher than I_{CCH} , since a base current flows when the output is forced active LOW (see Section 3); its value is rather low owing to the Power-On-Demand circuitry.

I_{CCZ} See comment above for I_{CCH} .

$I_{PU/PD}$ Maximum current into the output when powering up or down. This parameter is valued for any V_{CC} between 0V and 1.2V with a transition time of up to 10ms. From $V_{CC} = 1.2V$ to $V_{CC} = 3.3V \pm 0.3V$ a transition time of 100 μs is permitted.

The ALVT datasheet contains additional data specifying AC and DC characteristics for a supply voltage of 2.5V (2.3–2.7V). Other relatively new characteristics are skew and data referring to the effects of dynamic thresholds (see section 5.1).

5 TREND CURVES FOR ALVT16245

The ALVT16245 datasheet is of great help in gaining more insight into the part's behavior due to a number of extra curves. These curves include the following:

5.1 Dynamic Thresholds

Due to some internal effects, depending on drive and loading conditions, the normally static values of V_{IL} and V_{IH} change under dynamic conditions. For parts with low output drive, such effects were usually ignored, but for high output drive parts, such as ALVT, it is useful to know how these values may change. For instance, better noise margin targets may be set due to high capacitive loading that negatively affects the input thresholds. Figures 6 and 7 give the dependency of the dynamic threshold voltages on V_{CC} and switching frequency.

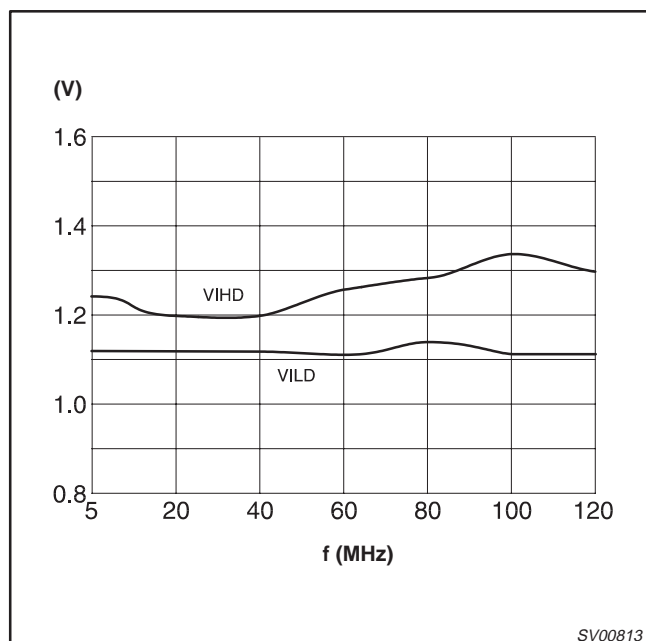


Figure 6. VILD/VIHD f (MHz)

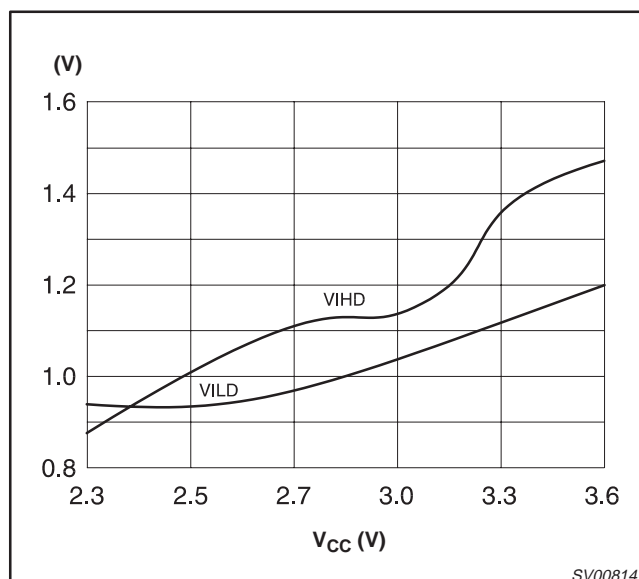


Figure 7. VILD/VIHD V_{CC} (V)

5.2 Ground Bounce

LVT and ALVT are designed so that an optimum is reached between both propagation delay and ground bounce. As we know, this represents a trade-off: higher speed parts will exhibit more ground noise. Figures 8 and 9 show that at higher capacitive loads a lower ground bounce is observed due to the optimized bipolar output stage and the delayed PMOS (see Section 3). Also, the dependency of ground bounce on the number of outputs switching has been minimized.

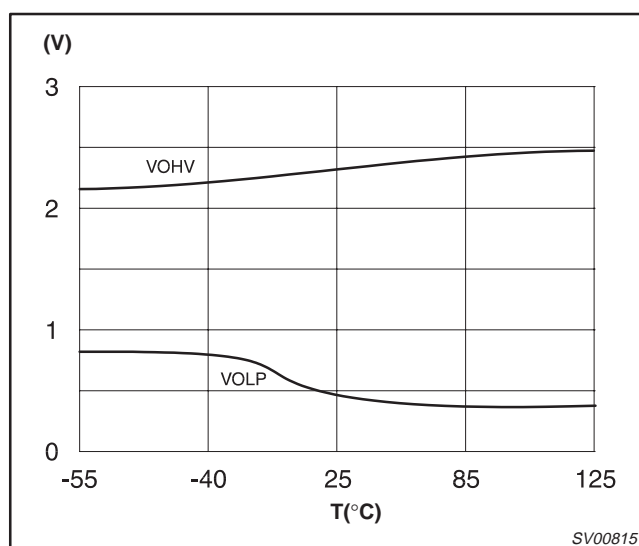
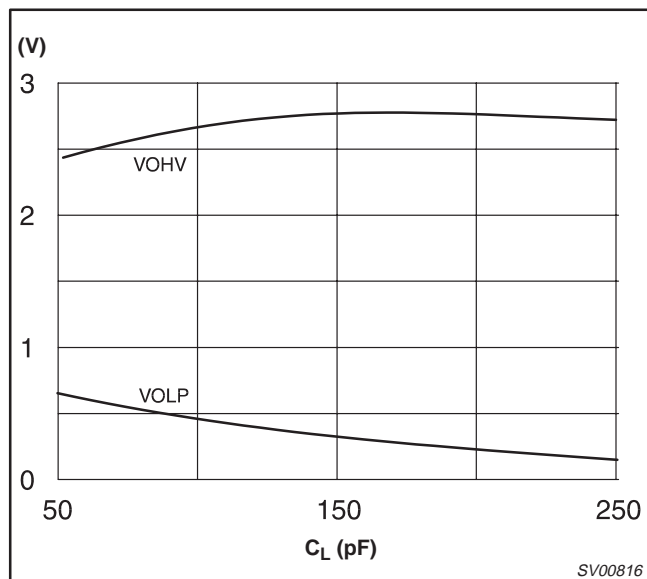
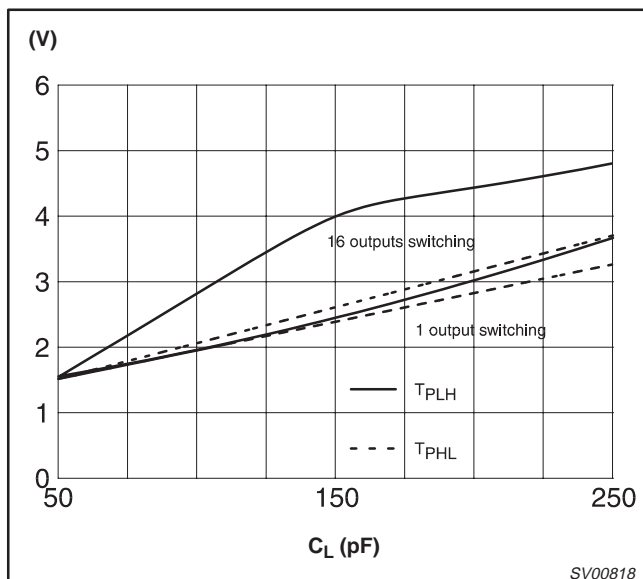


Figure 8. Bounce Temperature ($^{\circ}C$)

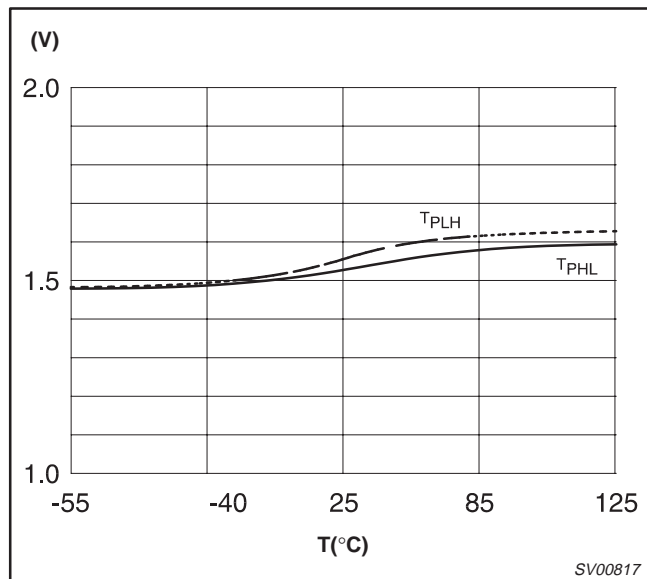
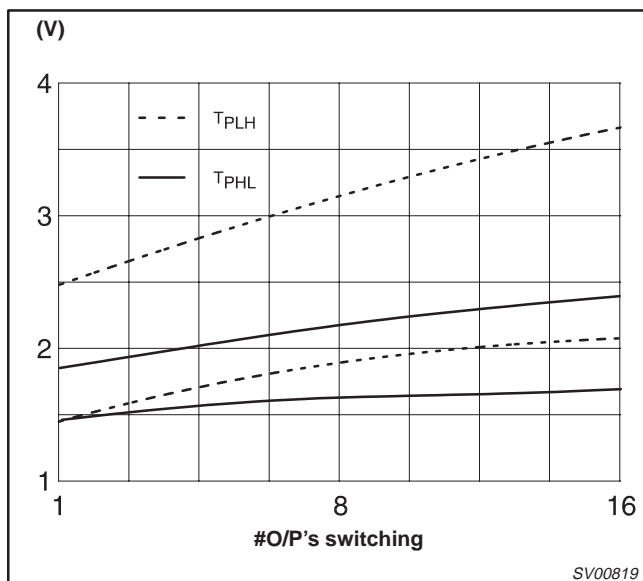
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Figure 9. Bounce C_{LOAD} (pF)Figure 11. T_{PLH}/T_{PHL} (C_L and O/P's switching) C_{LOAD} (pF)

5.3 Propagation Delays

The temperature dependency of the propagation delay times (Figure 10) is excellent due to optimum use of components available in QUBiC. Due to ground bounce, the delay time depends on the number of outputs switching simultaneously. For LVT and ALVT this is kept to a minimum by using a good balance between ground bounce and delay times as shown in Figures 11 and 12.

Figure 10. T_{PLH}/T_{PHL} Temperature ($^{\circ}C$)Figure 12. T_{PLH}/T_{PHL} (# O/P's switching)

5.4 Skew Characteristics

The propagation delay times are very short, so we decided to add skew characteristics for a variety of conditions, for example, the spread of propagation delays within one part and over various parts of the same type number. A further explanation can be found in Databook IC23 (Reference #3).

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6 DESIGNING WITH LVT/ALVT

The drive capability has been assessed in a backplane application. Figure 13 shows how a 74LVT244 behaves when driving a backplane with an impedance of around 30Ω . Notice the relatively sharp edges due to the fact that the transmission line has a low capacitance and behaves much like a real load.

SPICE models for optimizing your design with LVT and ALVT are available for some platforms such as Berkeley SPICE, PSPICE and HSPICE. The latest models can always be found on the WWW (see cover). SPICE is an essential tool for studying signal integrity and for analysis of the behavior of a system with extreme devices.

To minimize board space, all parts are available in a variety of packages including TSSOP (Thin Shrink Small Outline Package) while for the future also TVSOP (Thin Very Small Outline Package) with a 0.4mm pitch is in the planning stages for 1998.

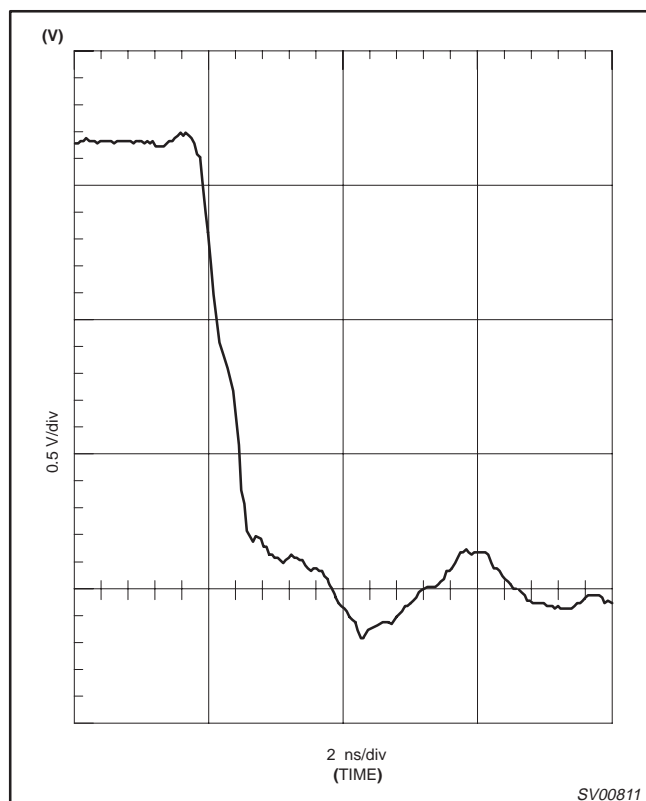


Figure 13. LVT driving 30Ω transmission line, H to L transition

7 SUMMARY

Both LVT and ALVT logic families are state-of-the-art logic families, optimized for use as backplane drivers. These parts combine very fast switching with low power dissipation. The clever design makes them an ideal choice for use in backplanes in high-end EDP and telecom applications. In other areas also where very short propagation delays are a must, both families excel. Added features such as automatic 3-state when the part's output is tied to a higher voltage make them an ideal choice in many mixed mode 3V – 5V systems.

8 ACKNOWLEDGEMENTS

We would like to acknowledge Tom Parkinson, Alan Glaus and Mike Magdaluyo for their help on this Application Note.

9 REFERENCES

1. Application Note AN2022, The behaviour of integrated bus hold circuits, Tinus van de Wouw, Philips Semiconductors, 1996, Order Number: 9397 750 00798
2. Application Note AN240, Interfacing 3V and 5V Applications, Todd Anderson and Tinus van de Wouw, Philips Semiconductors, 1995, Order Number: 9397 750 00282
3. Data handbook IC23, BiCMOS Interface Logic, 1998, Philips Semiconductors

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