VMEbus Connector Pin Assignment and Signal Descriptions Under VME64x

Pin Assignment for the VMEbus P1/J1 Connector					
Pin	Row z	Row a	Row b	Row c	Row d
1	MPR	D00	BBSY*	D08	VPC
2	GND	D01	BCLR*	D09	GND
3	MCLK	D02	ACFAIL*	D10	+V1
4	GND	D03	BG0IN*	D11	+V2
5	MSD	D04	BG0OUT*	D12	RsvU
6	GND	D05	BG1IN*	D13	-V1
7	MMD	D06	BG1OUT*	D14	-V2
8	GND	D07	BG2IN*	D15	RsvU
9	MCTL	GND	BG2OUT*	GND	GAP*
10	GND	SYSCLK	BG3IN*	SYSFAIL*	GA0*
11	RESP*	GND	BG3OUT*	BERR*	GA1*
12	GND	DS1*	BR0*	SYSRESET*	+3.3V
13	RsvBus	DS0*	BR1*	LWORD*	GA2*
14	GND	WRITE*	BR2*	AM5	+3.3V
15	RsvBus	GND	BR3*	A23	GA3*
16	GND	DTACK*	AM0	A22	+3.3V
17	RsvBus	GND	AM1	A21	GA4*
18	GND	AS*	AM2	A20	+3.3V
19	RsvBus	GND	AM3	A19	RsvBus
20	GND	IACK*	GND	A18	+3.3V
21	RsvBus	IACKIN*	SERA	A17	RsvBus
22	GND	IACKOUT*	SERB	A16	+3.3V
23	RsvBus	AM4	GND	A15	RsvBus
24	GND	A07	IRQ7*	A14	+3.3V
25	RsvBus	A06	IRQ5*	A13	RsvBus
26	GND	A05	IRQ5*	A12	+3.3V
27	RsvBus	A04	IRQ4*	A11	LI/I*
28	GND	A03	IRQ3*	A10	+3.3V
29	RsvBus	A02	IRQ2*	A09	LI/O*
30	GND	A01	IRQ1*	A08	+3.3V
31	RsvBus	-12 VDC	+5VSTBY	+12 VDC	GND
32	GND	+5 VDC	+5 VDC	+5 VDC	VPC

Note: (*): indicates active low signal.
Shaded regions indicate new signals defined or redefined under VME64 or VME64x.

Pin Assignment for the VMEbus P2/J2 Connector					
Pin	Row z	Row a	Row b	Row c	Row d
1	UsrDef	UsrDef	+5 VDC	UsrDef	UsrDef
2	GND	UsrDef	GND	UsrDef	UsrDef
3	UsrDef	UsrDef	RETRY*	UsrDef	UsrDef
4	GND	UsrDef	A24	UsrDef	UsrDef
5	UsrDef	UsrDef	A25	UsrDef	UsrDef
6	GND	UsrDef	A26	UsrDef	UsrDef
7	UsrDef	UsrDef	A27	UsrDef	UsrDef
8	GND	UsrDef	A28	UsrDef	UsrDef
9	UsrDef	UsrDef	A29	UsrDef	UsrDef
10	GND	UsrDef	A30	UsrDef	UsrDef
11	UsrDef	UsrDef	A31	UsrDef	UsrDef
12	GND	UsrDef	GND	UsrDef	UsrDef
13	UsrDef	UsrDef	+5 VDC	UsrDef	UsrDef
14	GND	UsrDef	D16	UsrDef	UsrDef
15	UsrDef	UsrDef	D17	UsrDef	UsrDef
16	GND	UsrDef	D18	UsrDef	UsrDef
17	UsrDef	UsrDef	D19	UsrDef	UsrDef
18	GND	UsrDef	D20	UsrDef	UsrDef
19	UsrDef	UsrDef	D21	UsrDef	UsrDef
20	GND	UsrDef	D22	UsrDef	UsrDef
21	UsrDef	UsrDef	D23	UsrDef	UsrDef
22	GND	UsrDef	GND	UsrDef	UsrDef
23	UsrDef	UsrDef	D24	UsrDef	UsrDef
24	GND	UsrDef	D25	UsrDef	UsrDef
25	UsrDef	UsrDef	D26	UsrDef	UsrDef
26	GND	UsrDef	D27	UsrDef	UsrDef
27	UsrDef	UsrDef	D28	UsrDef	UsrDef
28	GND	UsrDef	D29	UsrDef	UsrDef
29	UsrDef	UsrDef	D30	UsrDef	UsrDef
30	GND	UsrDef	D31	UsrDef	UsrDef
31	UsrDef	UsrDef	GND	UsrDef	GND
32	GND	UsrDef	+5 VDC	UsrDef	VPC

Note: (*): indicates active low signal.
Shaded regions indicate new signals defined or redefined under VME64 or VME64x.

Pin Assignment for the VMEbus P0/J0/RJ0/RP0 Connector							
Position	Row f	Row e	Row d	Row c	Row b	Row a	Row z
1	GND	UD	UD	UD	UD	UD	GND
2	GND	UD	UD	UD	UD	UD	GND
3	GND	UD	UD	UD	UD	UD	GND
4	GND	UD	UD	UD	UD	UD	GND
5	GND	UD	UD	UD	UD	UD	GND
6	GND	UD	UD	UD	UD	UD	GND
7	GND	UD	UD	UD	UD	UD	GND
8	GND	UD	UD	UD	UD	UD	GND
9	GND	UD	UD	UD	UD	UD	GND
10	GND	UD	UD	UD	UD	UD	GND
11	GND	UD	UD	UD	UD	UD	GND
12	GND	UD	UD	UD	UD	UD	GND
13	GND	UD	UD	UD	UD	UD	GND
14	GND	UD	UD	UD	UD	UD	GND
15	GND	UD	UD	UD	UD	UD	GND
16	GND	UD	UD	UD	UD	UD	GND
17	GND	UD	UD	UD	UD	UD	GND
18	GND	UD	UD	UD	UD	UD	GND
19	GND	UD	UD	UD	UD	UD	GND

VMEbus Signal Descriptions	
Signal Name	Description
A01 - A31	Address lines [A01 - A31] carry a binary address.
AM0 - AM5	The address modifier code [AM0 - AM5] is a 'tag' that indicates the type of VMEbus cycle in progress.
BG0IN* - BG3IN* BG0OUT* - BG3OUT*	The bus grant signals [BG0IN* - BG3IN* and BG0OUT* - BG3OUT*] are part of the bus grant daisy chain and are driven by arbiters and requesters. The slot 01 arbiter asserts a bus grant in response to a bus request on the same level [BR0* - BR3*]. The bus grant daisy-chain starts at the slot 01 system controller and propagates from module to module until it reaches the module that initially requested the bus. Each VMEbus module has a bus grant input and a bus grant output. They are standard totem-pole class signals.

BR0* - BR3*	Bus requests [BR0* - BR3*] are asserted by a requester whenever its master or interrupt han-dler needs the bus. Before accepting the bus, the master waits until the arbiter grants the bus by way of the bus grant daisy-chain [BG0IN* - BG3IN*]. They are open-collector class signals.
D00-D31	Data bus [D00-D31] is driven by masters, slaves or interrupters. These are bi-directional sig-nals and are used for data transfers. Different portions of the data bus are used de-pending upon the state of DS0*, DS1*, A01 and LWORD* pins. They are standard three-state signals. The data lines can also be used to transfer a portion of the address during MD32, MBLT and 2eVME cycles.
DS0*, DS1*	Data strobes DS0* and DS1* are driven by masters and interrupt handlers. These sig-nals serve not only to qualify data, but also to indicate the size and position of the data transfer. When combined with LWORD* and A01, the data strobes indicate the size and type of data transfer. DS0* - DS1* are high current three-state class signals.
DTACK*	Data transfer acknowledge [DTACK*] is driven by slaves or interrupters. During write cycles DTACK* is asserted by a slave after it has latched data. During read and inter-rupt acknowledge cycles, DTACK* is asserted by a slave after data is placed onto the bus. DTACK* can be an open-collector or a high current three-state class signal.
GA0* - GA4*	The geographical address [GA0*-GA4*] is a binary code that indicates the slot number of the backplane. They are open collector signals, and were added to the 160 pin P1/J1 connector in the VME64x specification.
GAP*	The geographical address parity [GAP*] is tied high or floating, depending upon the parity of the geographical address lines [GA0*-GA4*]. It is an open collector signal, and was added to the 160 pin P1/J1 connector in the VME64x specification.
GND	Ground [GND] is used both as a signal reference and a power return path.
IACK*	Interrupt acknowledge [IACK*] is driven by interrupt handlers in response to interrupt re-quests. It is connected to IACKIN* at slot 01 (on the backplane), and used by the IACK* daisy-chain driver to start propagation of the [IACKIN* - IACKOUT*] daisy-chain. IACK* can be either an open-collector or a standard three-state class signal.

IACKIN*, IACKOUT*	The interrupt acknowledge daisy chain [IACKIN* - IACKOUT*] is driven by the IACK* daisy-chain driver. These signals are used both to indicate that an interrupt acknowledge cycle is in progress, and to determine which interrupters should return a STATUS/ID. They are standard totem-pole class signals.
IRQ1*-IRQ7*	Priority interrupt requests [IRQ1*-IRQ7*] are asserted by interrupters. Level seven is the high-est priority, and level one the lowest. They are open-collector class signals.
LI/I*	The live insertion input [LI/I*] signal is used to carry hot swap (live insertion) control information. It is a three state driven signal and was added to the 160 pin P1/J1 connector in the VME64x specification.
LI/O*	The live insertion output [LI/O*] signal is used to carry hot swap (live insertion) control information. It is a three state driven signal and was added to the 160 pin P1/J1 connector in the VME64x specification.
LWORD*	Long word [LWORD*] is driven by masters. It is used in conjunction with A01, DS0* and DS1* to indicate the size of the current data transfer. LWORD* is a standard three-state class signal. During 64-bit address transfers, LWORD* doubles as address bit A00. During 64-bit data transfers, LWORD* doubles as a data bit.
MCLK, MCTL, MMD, MPR, MSD	These signals are part of the IEEE 1149.5 MTM bus. They are three-state driven signals which was added to the 160 pin P1/J1 connector in the VME64x specification.
RESERVED	The RESERVED signal pin is obsolete and is no longer used. Under the IEEE 1014-1987 version of the bus specification there was a single reserved pin. This pin was redefined under VME64 as the RETRY* pin. The VME64x specification uses the names RsvB and RsvU for reserved pins.
RESP*	The response [RESP*] signal is used to carry the information as defined by the 2eVME protocol. It was added to the 160 pin P1/J1 connector in the VME64x specification.
RsvB	The reserved/bused [RsvB] signal should not be used. VME64x backplanes must bus and terminate this signal. It was added to the 160 pin P1/J1 connector in the VME64x specification.
RsvU	The reserved/unbused [RsvU] signal should not be used. VME64x backplanes must not bus or terminate this signal. It was added to the 160 pin P1/J1 connector in the VME64x specification.

RETRY*	[RETRY*], together with [BERR*], can be asserted by a slave to postpone a data transfer. The master must then attempt the cycle again at a later time. The retry cycle prevents deadlock (deadly embrace) conditions in bus-to-bus links and sec-ondary buses. RETRY* is a standard three-state signal. The [RETRY*] signal was added in the ANSI/VITA 1-1994 (VME64) version of the bus spec-ification. This pin was RESERVED in earlier versions. However, boards that support [RETRY*] should work just fine with older backplanes, as they were required to bus and terminate this signal line.
SERA, SERB	The [SERA] and [SERB] signals are used for an (optional) serial bus such as the AUTOBAHN (IEEE 1394) or VMSbus. Under the ANSI/VITA 1-1994 (VME64) bus specification, these pins can be used for any user defined serial bus. Earlier versions of the VMEbus specification defined these pins as [SERCLK] and [SERDAT*], which were originally intended for a serial bus called VMSbus. However, they were rarely used for that purpose.
SERCLK, SERDAT*	The [SERCLK] and [SERDAT*] signals were made obsolete under the ANSI/VITA 1-1994 (VME64) bus specification. Refer to [SERA] and [SERB] for more details.
SYSCLK	16 MHz utility clock [SYSCLK] is driven by the slot 01 system controller. This clock can be used for any purpose, and has no timing relationship to other VMEbus signals. SYSCLK* is a high current totem-pole class signal.
SYSFAIL*	System fail [SYSFAIL*] can be asserted or monitored by any module. It indicates that a failure has occurred in the system. Implementation of [SYSFAIL*] is user de-fined, and its use is optional. SYSFAIL* is an open-collector class signal.
SYSRESET*	System reset [SYSRESET*] can be driven by any module and indicates that a reset (such as power-up) is in progress. SYSRESET* is an open-collector class signal.
UsrDef, UD	Pins that are user defined [specified as 'UsrDef' or 'UD'] can be specified by the user. Generally, they are routed directly through the backplane so that they can be connected to cables or to rear I/O transition modules.
VPC	Voltage pre-charge [VPC] pins forma a 'make first / break last' contact. They are intended to be used as pre-charge power sources for live insertion logic. These pins were added to the 160 pin P1/J1 and P2/J2 connectors in the VME64x specification. The VPC pins are connected to the +5 VDC power supply on VME64x backplanes. These pins may also be used as additional +5 VDC power pins in boards that do not support live insertion.

+V1, -V1, +V2, -V2	The [+/- V1/V2] power pins supply 38 - 75 VDC to the bus module. They are also known as the auxiliary power pins, and were originally intended to be used as 48 VDC battery supplies in Telecom systems. However, they can be used for any purpose. These pins were added to the 160 pin P1/J1 connector in the VME64x specification.
WRITE*	The read / write signal [WRITE*] is driven by masters. It indicates the direction of data transfer over the bus. It is asserted during a write cycle and negated during a read cycle. WRITE* is a stan-dard three-state class signal.
+5V STDBY	[+5V STDBY] is an optional +5 VDC standby power supply. This power pin is often connected to a rechargable battery. This eliminates the need for individual batteries on VMEbus modules. Individual batteries are often used for real time clock and static RAM chips.
+3.3 V	Main +3.3 VDC power source. These pins were added to the 160 pin P1/J1 connector in the VME64x specification.
+5 VDC +12 VDC, -12 VDC	The main system power supplies are [+5 VDC], [+12 VDC] and [-12 VDC].

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