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## Using SelectI/O Interfaces in Spartan-II and Spartan-IIE FPGAs

### Summary

The Spartan™-II/IIE FPGA families simplify high-performance design by offering SelectI/O™ inputs and outputs. The Spartan-II devices can support 16 different I/O standards and the Spartan-IIE devices support 19 I/O standards with different specifications for current, voltage, I/O buffering, and termination techniques. As a result, the Spartan-II/IIE FPGA can be used to integrate discrete translators and directly drive the most advanced backplanes, busses, and memories. This application note describes how to take full advantage of the flexibility of the SelectI/O features and the design considerations to improve and simplify system level design.

### Introduction

As FPGAs are used in more advanced applications, they must support an increased variety of I/O standards. Directly providing the necessary interface standard not only eliminates the cost of external translators, but also significantly improves the critical chip-to-chip speed and reduces power consumption. The revolutionary SelectI/O input/output standards of Spartan-II/IIE devices have met this need by providing a highly configurable, high-performance alternative to the I/O resources of conventional programmable devices. SelectI/O resources are most useful in applications with high-speed memory or programmable backplane interfaces running at over 100 MHz.

This application note covers the following topics:

- Overview of I/O Standards
- Choosing SelectI/O Options
- Board Design Considerations

### SelectI/O Overview

Each Spartan-II SelectI/O block can support up to 16 I/O standards (19 in the Spartan-IIE family). Supporting such a variety of I/O standards allows the support of a wide variety of applications, from general purpose standard applications to high-speed low-voltage memory busses.

SelectI/O blocks also provide selectable output drive strengths and programmable slew rates for the LVTTTL output buffers, as well as an optional, programmable weak pull-up, weak pull-down, or weak "keeper" circuit ideal for use in external bussing applications.

Each Input/Output Block (IOB) includes three registers, one each for the input, output, and 3-state signals within the IOB. These registers are optionally configurable as either a D-type flip-flop or as a level sensitive latch.

The input buffer has an optional delay element used to guarantee a zero hold time requirement for input signals registered within the IOB.

The Spartan-II/IIE SelectI/O features also provide dedicated resources for input reference voltage ( $V_{REF}$ ) and output source voltage ( $V_{CCO}$ ), along with a convenient banking system that simplifies board design.

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By taking advantage of the built-in features and wide variety of I/O standards supported by the SelectI/O features, system-level design and board design can be greatly simplified and improved.

## I/O Standards Fundamentals

Modern bus applications, pioneered by the largest and most influential companies in the digital electronics industry, are commonly introduced with a new I/O standard tailored specifically to the needs of that application. The bus I/O standards provide specifications to other vendors who create products designed to interface with these applications. Each standard often has its own specifications for current, voltage, I/O buffering, and termination techniques.

The ability to provide the flexibility and time-to-market advantages of programmable logic is increasingly dependent on the capability of the programmable logic device to support an ever increasing variety of I/O standards. The SelectI/O resources feature highly configurable input and output buffers which provide support for a wide variety of I/O standards.

## Overview of Supported I/O Standards

**Table 1** provides a brief overview of the I/O standards supported by the Spartan-II/IIe FPGAs, including the sponsors and common uses for the standard. Detailed information on each specification may be found on the Electronic Industry Association (EIA) JEDEC website at [www.jedec.org](http://www.jedec.org). The standard numbers are indicated where appropriate.

Table 1: SelectI/O Standards

Standard	Description	Spec	Use/Sponsor	Input Buffer	Output Buffer	5V Tolerant <sup>(1)</sup>
LVTTTL	Low Voltage TTL	JESD8B	General purpose	LVTTTL	Push-Pull	Yes
LVC MOS2	Low Voltage CMOS for 2.5V	JESD8B	General purpose 2.5V	CMOS	Push-Pull	Yes
LVC MOS18	Low Voltage CMOS for 1.8V	JESD8B	General purpose 1.8V	CMOS	Push-Pull	No
PCI	Peripheral Component Interconnect	PCI SIG	PCI bus	LVTTTL	Push-Pull	33 MHz, 5V Option
GTL	Gunning Transceiver Logic	JESD8-3	High-speed bus, backplane; Xerox	Differential Amplifier	Open Drain	No
GTL+	GTL Plus		Intel Pentium Pro			
HSTL	High-Speed Transceiver Logic	JESD8-6	Hitachi SRAM; IBM; three of four classes supported	Differential Amplifier	Push-Pull	No
SSTL3	Stub Series Terminated Logic for 3.3V	JESD8-8	SRAM/SDRAM bus; Hitachi and IBM; two classes	Differential Amplifier	Push-Pull	No
SSTL2	SSTL for 2.5V	JESD8-9				
CTT	Center Tap Terminated	JESD8-4	Memory bus; Fujitsu	Differential Amplifier	Push-Pull	No
AGP 2X	Accelerated Graphics Port	AGP Forum	Intel Pentium II, SRAM	Differential Amplifier	Push-Pull	No
LVDS	Low Voltage Differential Signaling	RS-644, IEEE 1596.3	High-speed interface, backplane, video; National, TI	Differential Pair	Differential Pair	No
BLVDS	Bus LVDS	RS-644, IEEE 1596.3	Multipoint LVDS	Differential Pair	Differential Pair	No
LVPECL	Low Voltage Positive ECL	Motorola	High-speed clocks	Differential Pair	Differential Pair	No

### Notes:

1. 5V tolerance only in Spartan-II family.

As shown in Table 2, each buffer type can support a variety of current and voltage requirements. While most I/O standards specify a range of allowed voltages, this document records typical voltage values only. See [www.jedec.org](http://www.jedec.org) for more details.

Table 2: SelectI/O Supported Standards (Typical Values)

I/O Standard	Input Reference Voltage ( $V_{REF}$ )	Input Voltage ( $V_{CC}$ ) <sup>(1)</sup>	Output Source Voltage ( $V_{CCO}$ )	Board Termination Voltage ( $V_{TT}$ )
LVTTTL	N/A	3.3	3.3	N/A
LVC MOS2	N/A	2.5	2.5	N/A
LVC MOS18 <sup>(1)</sup>	N/A	1.8	1.8	N/A
PCI (3V/5V <sup>(2)</sup> , 33 MHz/66 MHz)	N/A	3.3	3.3	N/A
GTL	0.8	N/A	N/A	1.2
GTL+	1.0	N/A	N/A	1.5
HSTL Class I	0.75	N/A	1.5	0.75
HSTL Class III	0.9	N/A	1.5	0.75
HSTL Class IV	0.9	N/A	1.5	0.75
SSTL3 Class I and II	1.5	N/A	3.3	1.5
SSTL2 Class I and II	1.25	N/A	2.5	1.25
CTT	1.5	N/A	3.3	1.5
AGP 2X	1.32	N/A	3.3	N/A
LVDS and BLVDS <sup>(1)</sup>	N/A	N/A	2.5	N/A
LVPECL <sup>(1)</sup>	N/A	N/A	3.3	N/A

**Notes:**

1. Spartan-IIE family only.
2. Spartan-II family only.

### LVTTTL — Low-Voltage TTL

The Low-Voltage TTL (LVTTTL) standard is a general purpose EIA/JESD standard for 3.3V applications that uses an LVTTTL input buffer and a Push-Pull output buffer. This standard requires a 3.3V output source voltage ( $V_{CCO}$ ), but does not require the use of a reference voltage ( $V_{REF}$ ) or a termination voltage ( $V_{TT}$ ).

### LVC MOS2 — Low-Voltage CMOS for 2.5V

The Low-Voltage CMOS for 2.5V or lower (LVC MOS2) standard is an extension of the LVC MOS standard used for general purpose 2.5V applications. This standard requires a 2.5V output source voltage ( $V_{CCO}$ ), but does not require the use of a reference voltage ( $V_{REF}$ ) or a board termination voltage ( $V_{TT}$ ).

### LVC MOS18 — Low Voltage CMOS for 1.8V

This standard is an extension of the LVC MOS standard. It is used in general purpose 1.8V applications. The use of a reference voltage ( $V_{REF}$ ) or a board termination voltage ( $V_{TT}$ ) is not required.

### PCI — Peripheral Component Interface

The Peripheral Component Interface (PCI) standard specifies support for both 33 MHz and 66 MHz PCI bus applications. It uses an LVTTTL input buffer and a Push-Pull output buffer. This standard does not require the use of a reference voltage ( $V_{REF}$ ) or a board termination voltage ( $V_{TT}$ ), however, it does require a 3.3V output source voltage ( $V_{CCO}$ ).

***GTL — Gunning Transceiver Logic Terminated***

The Gunning Transceiver Logic (GTL) standard is a high-speed bus standard invented by Xerox. Xilinx has implemented the terminated variation for this standard. This standard requires a differential amplifier input buffer and an Open Drain output buffer.

***GTL+ — Gunning Transceiver Logic Plus***

The Gunning Transceiver Logic Plus (GTL+) standard is a high-speed bus standard (JESD8.3) first used by the Pentium Pro processor.

***HSTL — High-Speed Transceiver Logic***

The High-Speed Transceiver Logic (HSTL) standard is a general purpose high-speed 1.5V bus standard sponsored by IBM. This standard has four variations or classes. SelectI/O devices support Class I, III, and IV. This standard requires a Differential Amplifier input buffer and a Push-Pull output buffer.

***SSTL3 — Stub Series Terminated Logic for 3.3V***

The Stub Series Terminated Logic for 3.3V (SSTL3) standard is a general purpose 3.3V memory bus standard also sponsored by Hitachi and IBM (JESD8-8). This standard has two classes, I and II. SelectI/O devices support both classes for the SSTL3 standard. This standard requires a Differential Amplifier input buffer and an Push-Pull output buffer.

***SSTL2 — Stub Series Terminated Logic for 2.5V***

The Stub Series Terminated Logic for 2.5V (SSTL2) standard is a general purpose 2.5V memory bus standard sponsored by Hitachi and IBM. This standard has two classes, I and II. SelectI/O devices support both classes for the SSTL2 standard. This standard requires a Differential Amplifier input buffer and an Push-Pull output buffer.

***CTT — Center Tap Terminated***

The Center Tap Terminated (CTT) standard is a 3.3V memory bus standard sponsored by Fujitsu. This standard requires a Differential Amplifier input buffer and a Push-Pull output buffer.

***AGP 2X — Accelerated Graphics Port***

The Intel AGP standard is a 3.3V Accelerated Graphics Port 2X bus standard used with the Pentium II processor for graphics applications. This standard requires a Push-Pull output buffer and a Differential Amplifier input buffer.

***LVDS — Low Voltage Differential Signal***

LVDS is a differential I/O standard. It requires that one data bit is carried through two signal lines. As with all differential signaling standards, LVDS has an inherent noise immunity over single-ended I/O standards. The voltage swing between two signal lines is approximately 350 mV. The use of a reference voltage ( $V_{REF}$ ) or a board termination voltage ( $V_{TT}$ ) is not required. LVDS requires the use of two pins per input or output. LVDS requires external resistor termination.

***BLVDS — Bus LVDS***

This standard allows for bidirectional LVDS communication between two or more devices. The external resistor termination is different than the one for standard LVDS.

***LVPECL — Low Voltage Positive Emitter Coupled Logic***

LVPECL is another differential I/O standard. It requires two signal lines for transmitting one data bit. This standard specifies two pins per input or output. The voltage swing between these two signal lines is approximately 850 mV. The use of a reference voltage ( $V_{REF}$ ) or a board termination voltage ( $V_{TT}$ ) is not required. The LVPECL standard requires external resistor termination.

## Specifying an I/O Standard

To select an I/O standard, you must choose the appropriate component from the library or add an IOSTANDARD attribute to the appropriate buffer component. For example, for an input buffer that uses the GTL standard, you would choose the IBUF\_GTL component or choose the IBUF component and attach the IOSTANDARD=GTL attribute to it. The component can be selected via instantiation in HDL code or by placing it into a schematic. The attribute can be attached to a generic component by attaching an attribute in the schematic or HDL code or by including it in a constraints file.

## Library Symbols

The Xilinx library includes an extensive list of symbols designed to provide support for the variety of SelectI/O features (Table 3). Most of these symbols represent variations of the five generic SelectI/O symbols.

- IBUF (input buffer)
- IBUFG (global clock input buffer)
- OBUF (output buffer)
- OBUFT (3-state output buffer)
- IOBUF (input/output buffer)

### Registered I/O

The Spartan-II/IIE IOB includes an optional flip-flop or latch on the input path, output path, and 3-state control input. Note, however, that there are no special library components for the I/O registers. To simplify design, especially synthesis, the standard register primitives are automatically absorbed into the IOB when possible. This feature is selected by the user by turning on the Map Option "Pack I/O Registers/Latches into IOBs", which can be set to "Off" (default), "Inputs Only", "Outputs Only", or "Inputs and Outputs". Alternatively, the IOB=TRUE property can be placed on a register to force the mapper to place the register in an IOB.

An optional delay element is associated with the input path in each logic input primitive (IBUF or IOBUF). When the buffer drives an input register within the IOB, the delay element activates by default to ensure a zero hold time requirement. The user can override this default with the NODELAY=TRUE property. The delay element is not used for non-registered inputs, to provide higher performance. If extra delay is desired, use the DELAY=TRUE property.

### LVTTL Slew Rate and Drive Strength

The default LVTTL interface standard provides two unique output options, slew rate and drive strength. By default, the slew rate is reduced ("Slow") to minimize power bus transients when switching non-critical signals. This option is indicated as an "S" following the buffer name. Use the "Fast" slew rate for speed-critical outputs, indicated by an "F" following the buffer name. The slew rate can be alternatively specified with the SLEW= property, which can be set to "SLOW" or "FAST".

The drive strength is selected in a similar fashion, with the default being 12 mA. Select a buffer with the appropriate suffix for the desired drive strength, choosing from 2, 4, 6, 8, 12, 16, or 24. The drive strength can be alternatively specified with the DRIVE= property, which can be set to any of the same seven values.

Table 3: SelectI/O Library Symbols

			IBUF	IBUFG	OBUF	OBUFFT	IOBUF
LVTTTL	Slew	Drive					
	Slow	2 mA	IBUF	IBUFG	OBUF_S_2	OBUFFT_S_2	IOBUF_S_2
		4 mA			OBUF_S_4	OBUFFT_S_4	IOBUF_S_4
		6 mA			OBUF_S_6	OBUFFT_S_6	IOBUF_S_6
		8 mA			OBUF_S_8	OBUFFT_S_8	IOBUF_S_8
		12 mA			OBUF_S_12	OBUFFT_S_12	IOBUF_S_12
					OBUF	OBUFFT	IOBUF
		16 mA			OBUF_S_16	OBUFFT_S_16	IOBUF_S_16
		24 mA			OBUF_S_24	OBUFFT_S_24	IOBUF_S_24
	Fast	2 mA			OBUF_F_2	OBUFFT_F_2	IOBUF_F_2
		4 mA			OBUF_F_4	OBUFFT_F_4	IOBUF_F_4
		6 mA			OBUF_F_6	OBUFFT_F_6	IOBUF_F_6
		8 mA			OBUF_F_8	OBUFFT_F_8	IOBUF_F_8
		12 mA			OBUF_F_12	OBUFFT_F_12	IOBUF_F_12
		16 mA			OBUF_F_16	OBUFFT_F_16	IOBUF_F_16
		24 mA			OBUF_SF_24	OBUFFT_F_24	IOBUF_F_24
		LVCMOS2				IBUF_LVCMOS2	IBUFG_LVCMOS2
LVCMOS18			IBUF_LVCMOS18	IBUFG_LVCMOS18	OBUF_LVCMOS18	OBUFFT_LVCMOS18	IOBUF_LVCMOS18
PCI	Speed	Voltage					
	33 MHz	3V	IBUF_PCI33_3	IBUFG_PCI33_3	OBUF_PCI33_3	OBUFFT_PCI33_3	IOBUF_PCI33_3
		5V	IBUF_PCI33_5	IBUFG_PCI33_5	OBUF_PCI33_5	OBUFFT_PCI33_5	IOBUF_PCI33_5
	66 MHz	3V	IBUF_PCI66_3	IBUFG_PCI66_3	OBUF_PCI66_3	OBUFFT_PCI66_3	IOBUF_PCI66_3
GTL			IBUF_GTL	IBUFG_GTL	OBUF_GTL	OBUFFT_GTL	IOBUF_GTL
GTL+			IBUF_GTLP	IBUFG_GTLP	OBUF_GTLP	OBUFFT_GTLP	IOBUF_GTLP
HSTL	Class						
	I		IBUF_HSTL_I	IBUFG_HSTL_I	OBUF_HSTL_I	OBUFFT_HSTL_I	IOBUF_HSTL_I
	III		IBUF_HSTL_III	IBUFG_HSTL_III	OBUF_HSTL_III	OBUFFT_HSTL_III	IOBUF_HSTL_III
	IV		IBUF_HSTL_IV	IBUFG_HSTL_IV	OBUF_HSTL_IV	OBUFFT_HSTL_IV	IOBUF_HSTL_IV
SSTL	Voltage	Class					
	3V	I	IBUF_SSTL3_I	IBUFG_SSTL3_I	OBUF_SSTL3_I	OBUFFT_SSTL3_I	IOBUF_SSTL3_I
		II	IBUF_SSTL3_II	IBUFG_SSTL3_II	OBUF_SSTL3_II	OBUFFT_SSTL3_II	IOBUF_SSTL3_II
	2.5V	I	IBUF_SSTL2_I	IBUFG_SSTL2_I	OBUF_SSTL2_I	OBUFFT_SSTL2_I	IOBUF_SSTL2_I
		II	IBUF_SSTL2_II	IBUFG_SSTL2_II	OBUF_SSTL2_II	OBUFFT_SSTL2_II	IOBUF_SSTL2_II
CTT			IBUF_CTT	IBUFG_CTT	OBUF_CTT	OBUFFT_CTT	IOBUF_CTT
AGP			IBUF_AGP	IBUFG_AGP	OBUF_AGP	OBUFFT_AGP	IOBUF_AGP
LVDS			IBUF_LVDS	IBUFG_LVDS	OBUF_LVDS	OBUFFT_LVDS	IOBUF_LVDS
LVPECL			IBUF_LVPECL	IBUFG_LVPECL	OBUF_LVPECL	OBUFFT_LVPECL	IOBUF_LVPECL

## IBUF

Signals used as inputs to the device must source an input buffer (IBUF) via an external input port. The generic IBUF symbol appears in [Figure 1](#). The extension to the base name defines which I/O standard the IBUF uses. The assumed standard is LVTTTL when the generic IBUF has no specified extension.

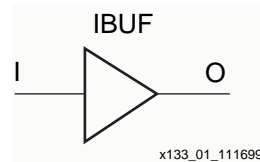


Figure 1: Input Buffer (IBUF) Symbol

## IBUFG

Signals used as high fanout clock inputs to the device should drive a global clock input buffer (IBUFG) via an external input port in order to take advantage of one of the four dedicated global clock distribution networks. The output of the IBUFG symbol can only drive a CLKDLL, CLKDLLHF, or a BUFG symbol. The generic IBUFG symbol appears in [Figure 2](#).

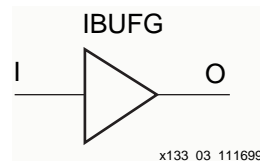


Figure 2: Global Clock Input Buffer (IBUFG) Symbol

As an added convenience, the BUFGP can be used to instantiate a high fanout clock input. The BUFGP symbol represents a combination of the LVTTTL IBUFG and BUFG symbols, such that the output of the BUFGP can connect directly to the clock pins throughout the design.

Unlike previous architectures, the Spartan-II/IIE BUFGP symbol can only be placed in a global clock pad location. The LOC property can specify a location for the BUFGP.

## OBUF

An OBUF must drive outputs through an external output port. The generic output buffer (OBUF) symbol appears in [Figure 3](#).

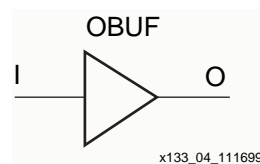


Figure 3: Output Buffer (OBUF) Symbol

## OBUFT

The generic 3-state output buffer OBUFT, shown in Figure 4, typically implements 3-state outputs or bidirectional I/O. Unused I/O are configured with OBUFT\_S\_12, which is disabled with a weak pull-down.

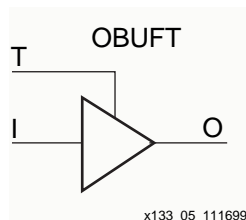


Figure 4: 3-State Output Buffer (OBUFT) Symbol

3-state output buffers and bi-directional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak “keeper” circuit. Control this feature by adding the appropriate symbol to the output net of the OBUFT (PULLUP, PULLDOWN, or KEEPER).

$V_{REF}$  is typically needed only for inputs that use an I/O standard requiring  $V_{REF}$ . However, an IOB configured using an OBUFT with a weak keeper circuit requires the input buffer to sample the I/O signal. Therefore, using an OBUFT will require the use of the  $V_{REF}$  pins in the bank if the OBUFT is configured with KEEPER and a standard that requires  $V_{REF}$ . In most applications the  $V_{REF}$  pins in the bank will be needed anyway because the OBUFT is usually combined with an input IBUF component.

## IOBUF

Use the IOBUF symbol for bidirectional signals that require both an input buffer and a 3-state output buffer with an active high 3-state pin. This symbol combines the functionality of the OBUFT and IBUF symbols. The generic input/output buffer IOBUF appears in Figure 5.

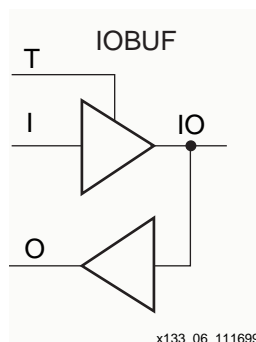


Figure 5: Input/Output Buffer (IOBUF) Symbol

3-state output buffers and bi-directional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak “keeper” circuit. Control this feature by adding the appropriate symbol to the output net of the IOBUF (PULLUP, PULLDOWN, or KEEPER).

## HDL Entry

SelectI/O components can be easily instantiated in VHDL or Verilog code. The Xilinx development system includes Language Templates for any of the standard I/O components. Following is an example of the template for the IOBUF input/output buffer component. Note that registers can automatically be merged into the Spartan-II/IIE SelectI/O block, simplifying the generation of the HDL code.

```
--Replace the XXX with the appropriate I/O standard
-- INOUT_PORT : inout STD_LOGIC;
--**Insert the following between the
-- 'architecture' and 'begin' keywords**
    signal IN_SIG, OUT_SIG, T_ENABLE:  std_logic;
component IOBUF_XXX
    port (I, T: in std_logic;
          O: out std_logic;
          IO: inout std_logic);
end component;
--**Insert the following after the 'begin' keyword**
U1: IOBUF_XXX port map (I => OUT_SIG, T => T_ENABLE,
                       O => IN_SIG, IO => INOUT_PORT);
```

### 5V Tolerance (Spartan-II only)

When the input buffer symbol (IBUF, IBUFG, or IOBUF) used supports an I/O standard that does not require a differential amplifier input (LVTTTL, LVCMOS2, or PCI33\_5), and the  $V_{CCO}$  within the given I/O bank is greater than 2V, the input automatically configures with a 5V-tolerant input buffer. If placing the single-ended input in a bank with an HSTL standard ( $V_{CCO} < 2V$ ), the input buffer is not 5V tolerant.

When the input symbol used supports an I/O standard that requires a differential amplifier input, the input automatically configures with a differential amplifier input buffer. The low-voltage I/O standards with a differential amplifier input require an external reference voltage input  $V_{REF}$ .

In summary, the following lists the Spartan-II SelectI/O standards for which the input and output buffers are 5V tolerant:

- LVTTTL
- LVCMOS2
- PCI33\_5

The 3V PCI I/O standards do not include 5V-tolerant input and output buffers.

## I/O Placement Rules

Each Spartan-II device provides eight banks of I/O, two per edge, for supporting multiple I/O standards on the same device. This allows multiple  $V_{REF}$  and  $V_{CCO}$  values on the same device. It is important to understand the restrictions on placement based on the availability of these banks.

### Reference Voltage ( $V_{REF}$ ) Pins

Low voltage I/O standards with a differential amplifier input buffer require an input reference voltage ( $V_{REF}$ ). Provide the  $V_{REF}$  as an external signal to the device. A resistor divider can be used to generate the source voltage, since the current required by  $V_{REF}$  is typically less than 10  $\mu A$ .

The voltage reference signal is "banked" within the device on a half-edge basis such that for all packages there are eight independent  $V_{REF}$  banks internally. See [Figure 6](#) for a representation of the I/O banks. Within each bank approximately one of every six I/O pins is automatically

configured as a  $V_{REF}$  input. After placing a differential amplifier input signal within a given  $V_{REF}$  bank, the same external source must drive all I/O pins configured as a  $V_{REF}$  input.

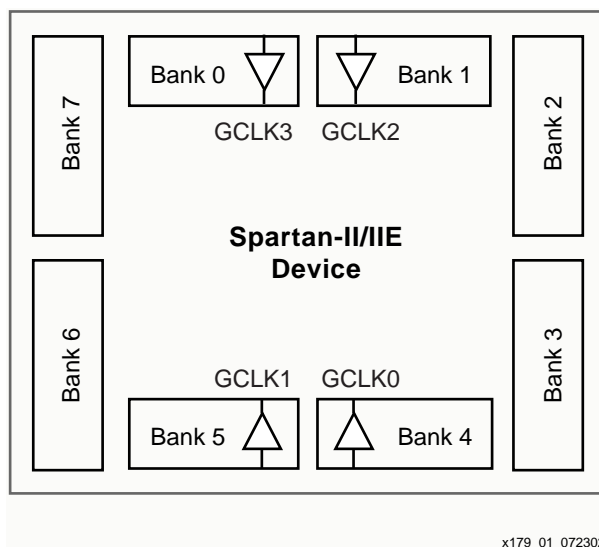


Figure 6: Spartan-II/IIE I/O Banks

Within each  $V_{REF}$  bank, any input buffers that require a  $V_{REF}$  signal must be of the same type. Output buffers of any type and input buffers can be placed without requiring a reference voltage within the same  $V_{REF}$  bank. Table 4 summarizes the input standards compatibility requirements.

Table 4: Xilinx Input Standards Compatibility Requirements

Rule 1	All differential amplifier input signals within a bank are required to be of the same standard.
Rule 2	There are no placement restrictions for inputs with standards that require a single-ended input buffer.

## Output Drive Source Voltage ( $V_{CCO}$ ) Pins

Many of the low voltage I/O standards supported by SelectI/O devices require a different output drive source voltage ( $V_{CCO}$ ). As a result each device can often have to support multiple output drive source voltages.

The  $V_{CCO}$  input is also divided into the same eight banks as  $V_{REF}$ . In some packages, the eight  $V_{CCO}$  banks are tied together in pairs by edge, allowing only four independent  $V_{CCO}$  levels, or all may be tied together, requiring one  $V_{CCO}$  level for the entire device. The number of independent  $V_{CCO}$  levels is shown in Table 5.

Table 5: Number of Independent  $V_{CCO}$  Levels

	Spartan-II	Spartan-IIE
FG456	8	8
FG256	8	N/A
FT256	N/A	8
PQ208	1	1
CS144	4	N/A
TQ144	4	1
VQ100	1	N/A

Output buffers within a given  $V_{CCO}$  bank must share the same output drive source voltage. Input buffers of any type and GTL output buffers can be placed within any  $V_{CCO}$  bank. Table 6 summarizes the output standards compatibility requirements.

**Table 6: Output Standards Compatibility Requirements**

Rule 1	Only outputs with standards which share compatible $V_{CCO}$ may be used within the same bank.
Rule 2	There are no placement restrictions for outputs with standards that do not require a $V_{CCO}$ .
$V_{CCO}$	Compatible Standards
3.3	PCI, LVTTTL, SSTL3_I, SSTL3_II, CTT, AGP, LVPECL, GTL, GTL+
2.5	SSTL2_I, SSTL2_II, LVCMOS2, LVDS, GTL, GTL+
1.8LVC MOS18, GTL, GTL+	HSTL_I, HSTL_III, HSTL_IV, GTL, GTL+
1.5	HSTL_I, HSTL_III, HSTL_IV, GTL, GTL+

## Location Constraints

Specify the location of each SelectI/O symbol with the location constraint LOC attached to the SelectI/O symbol. The external port identifier indicates the value of the location constrain. The format of the port identifier depends on the package chosen for the specific design. See the Spartan-II and Spartan-IIE data sheets for pin names and bank locations.

The LOC properties use the following form.

LOC = A12

LOC = P37

## Design Considerations

While the SelectI/O features are easy to use, attention to the following design considerations can help avoid pitfalls and improve success.

### Transmission Line Effects

The delay of an electrical signal along a wire is dominated by the rise and fall times when the signal travels a short distance. Transmission line delays vary with inductance and capacitance, but a well-designed board can experience delays of approximately 180 ps per inch.

Transmission line effects, or reflections, typically start at 1.5 inches for fast (1.5 ns) rise and fall times. Poor (or non-existent) termination or changes in the transmission line impedance cause these reflections and can cause additional delay in longer traces. As system speeds continue to increase, the effect of I/O delays can become a limiting factor and therefore transmission line termination becomes increasingly more important.

### Termination Techniques

A variety of termination techniques reduce the impact of transmission line effects.

The following lists output termination techniques.

- None
- Series
- Parallel (Shunt)
- Series and Parallel (Series-Shunt)

Input termination techniques include the following.

- None

- Parallel (Shunt)

These termination techniques can be applied in any combination. A generic example of each combination of termination methods appears in Figure 7.

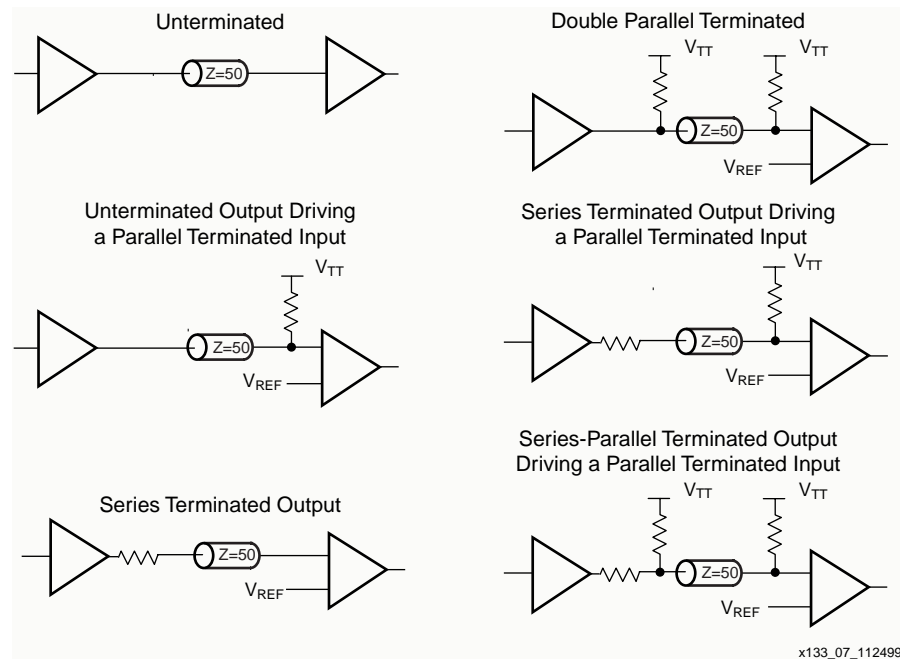


Figure 7: Overview of Standard Input and Output Termination Methods

## Simultaneous Switching Guidelines

Ground bounce can occur with high-speed digital ICs when multiple outputs change states simultaneously, causing undesired transient behavior on an output, or in the internal logic. This problem is also referred to as the Simultaneous Switching Output (SSO) problem.

Ground bounce is primarily due to current changes in the combined inductance of ground pins, bond wires, and ground metallization. The IC internal ground level deviates from the external system ground level for a short duration (a few nanoseconds) after multiple outputs change state simultaneously.

Ground bounce affects stable Low outputs and all inputs because they interpret the incoming signal by comparing it to the internal ground. If the ground bounce amplitude exceeds the actual instantaneous noise margin, then a non-changing input can be interpreted as a short pulse with a polarity opposite to the ground bounce.

Table 7 provides the guidelines for the maximum number of simultaneously switching outputs allowed per output power/ground pair to avoid the effects of ground bounce. Refer to Table 8 for the number of effective output power/ground pairs for each Spartan-II/IIE device and package combination.

**Table 7: Guidelines for Maximum Number of Simultaneously Switching Outputs per Power/Ground Pair**

Standard	Package	
	CS, FG, FT	PQ, TQ, VQ
LVTTL Slow Slew Rate, 2 mA drive	68	36
LVTTL Slow Slew Rate, 4 mA drive	41	20
LVTTL Slow Slew Rate, 6 mA drive	29	15
LVTTL Slow Slew Rate, 8 mA drive	22	12
LVTTL Slow Slew Rate, 12 mA drive	17	9
LVTTL Slow Slew Rate, 16 mA drive	14	7
LVTTL Slow Slew Rate, 24 mA drive	9	5
LVTTL Fast Slew Rate, 2 mA drive	40	21
LVTTL Fast Slew Rate, 4 mA drive	24	12
LVTTL Fast Slew Rate, 6 mA drive	17	9
LVTTL Fast Slew Rate, 8 mA drive	13	7
LVTTL Fast Slew Rate, 12 mA drive	10	5
LVTTL Fast Slew Rate, 16 mA drive	8	4
LVTTL Fast Slew Rate, 24 mA drive	5	3
LVC MOS2	10	5
PCI	8	4
GTL	4	4
GTL+	4	4
HSTL Class I	18	9
HSTL Class III	9	5
HSTL Class IV	5	3
SSTL2 Class I	15	8
SSTL2 Class II	10	5
SSTL3 Class I	11	6
SSTL3 Class II	7	4
CTT	14	7
AGP	9	5

**Notes:**

1. This analysis assumes a 35 pF load for each output.

Table 8: Effective Output Power/Ground Pairs for Spartan-II Devices

Package	Spartan-II Devices				
	XC2S15	XC2S30	XC2S50	XC2S100	XC2S150
VQ100	8	8	-	-	-
CS144	12	12	-	-	-
TQ144	12	12	12	12	-
PQ208	-	16	16	16	16
FG256	-	-	16	16	16
FG456	-	-	-	48	48

Table 9: Effective Output Power/Ground Pairs for Spartan-IIE Devices

Package	Spartan-IIE Devices				
	XC2S50E	XC2S100E	XC2S150E	XC2S200E	XC2S300E
TQ144	8	8	-	-	-
PQ208	16	16	16	16	-
FT256	24	24	24	24	24
FG456	-	32	32	32	32

## Useful Application Examples

Creating a design with the SelectI/O features requires the instantiation of the desired library symbol within the design code. At the board level, designers need to know the termination techniques required for each I/O standard.

This section describes some common application examples illustrating the termination techniques recommended by each of the standards supported by the SelectI/O features.

### Termination Examples

Circuit examples involving typical termination techniques for each of the SelectI/O standards follow. For a full range of accepted values for the DC voltage specifications for each standard, refer to the table associated with each figure.

The resistors used in each termination technique example and the transmission lines depicted represent board level components and are not meant to represent components on the device.

### GTL

A sample circuit illustrating a valid termination technique for GTL is shown in Figure 8.

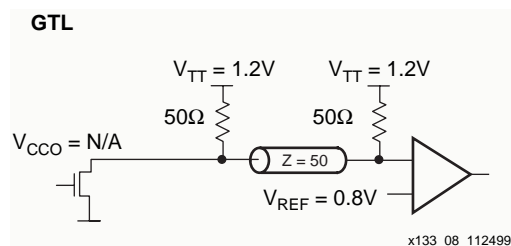


Figure 8: Terminated GTL

Table 10 lists DC voltage specifications.

Table 10: GTL Standard

Parameter	Min	Typ	Max
$V_{CCO}$	-	N/A	-
$V_{REF} = N \times V_{TT}^{(1)}$	0.74	0.8	0.86
$V_{TT}$	1.14	1.2	1.26
$V_{IH} = V_{REF} + 0.05$	0.79	0.85	-
$V_{IL} = V_{REF} - 0.05$	-	0.75	0.81
$V_{OH}$	-	-	-
$V_{OL}$	-	0.2	0.4
$I_{OH}$ at $V_{OH}$ (mA)	-	-	-
$I_{OL}$ at $V_{OL}$ (mA) at 0.4V	32	-	-
$I_{OL}$ at $V_{OL}$ (mA) at 0.2V	-	-	40

**Notes:**

1. N must be greater than or equal to 0.653 and less than or equal to 0.68.

## GTL+

A sample circuit illustrating a valid termination technique for GTL+ appears in Figure 9. DC voltage specifications appear in Table 11.

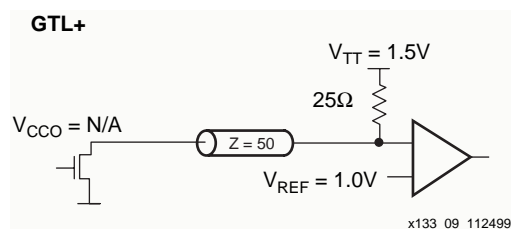


Figure 9: Terminated GTL+

Table 11: GTL+ Standard

Parameter	Min	Typ	Max
$V_{CCO}$	-	-	-
$V_{REF} = N \times V_{TT}^1$	0.88	1.0	1.12
$V_{TT}$	1.35	1.5	1.65
$V_{IH} = V_{REF} + 0.2$	1.08	1.2	-
$V_{IL} = V_{REF} - 0.2$	-	0.8	0.92
$V_{OH}$	-	-	-
$V_{OL}$	0.3	0.45	0.6
$I_{OH}$ at $V_{OH}$ (mA)	-	-	-
$I_{OL}$ at $V_{OL}$ (mA) at 0.6V	36	-	-
$I_{OL}$ at $V_{OL}$ (mA) at 0.3V	-	-	48

**Notes:**

1. N must be greater than or equal to 0.653 and less than or equal to 0.68.

## HSTL

A sample circuit illustrating a valid termination technique for HSTL\_I appears in Figure 10. HSTL Class I DC voltage specifications appear in Table 12.

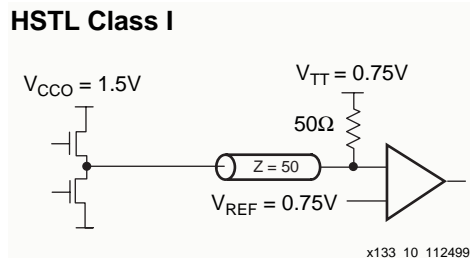


Figure 10: Terminated HSTL Class I

Table 12: HSTL Class I Standard

Parameter	Min	Typ	Max
$V_{CCO}$	1.40	1.50	1.60
$V_{REF}$	0.68	0.75	0.90
$V_{TT}$	-	$V_{CCO} \times 0.5$	-
$V_{IH}$	$V_{REF} + 0.1$	-	-
$V_{IL}$	-	-	$V_{REF} - 0.1$
$V_{OH}$	$V_{CCO} - 0.4$	-	-
$V_{OL}$	-	-	0.4
$I_{OH}$ at $V_{OH}$ (mA)	-8	-	-
$I_{OL}$ at $V_{OL}$ (mA)	8	-	-

A sample circuit illustrating a valid termination technique for HSTL\_III appears in Figure 11. DC voltage specifications appear in Table 13.

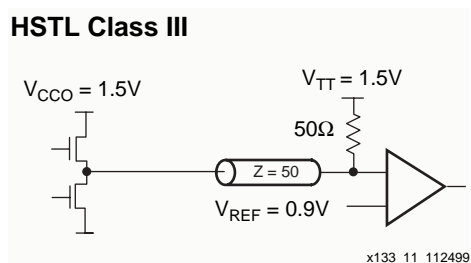


Figure 11: Terminated HSTL Class III

Table 13: HSTL Class III Standard

Parameter	Min	Typ	Max
$V_{CCO}$	1.40	1.50	1.60
$V_{REF}^{(1)}$	-	0.90	-
$V_{TT}$	-	$V_{CCO}$	-
$V_{IH}$	$V_{REF} + 0.1$	-	-
$V_{IL}$	-	-	$V_{REF} - 0.1$
$V_{OH}$	$V_{CCO} - 0.4$	-	-
$V_{OL}$	-	-	0.4
$I_{OH}$ at $V_{OH}$ (mA)	-8	-	-
$I_{OL}$ at $V_{OL}$ (mA)	24	-	-

**Notes:**

1. Per EIA/JESD8-6, "The value of  $V_{REF}$  is to be selected by the user to provide optimum noise margin in the use conditions specified by the user."

A sample circuit illustrating a valid termination technique for HSTL\_IV appears in Figure 12. DC voltage specifications appear in Table 14.

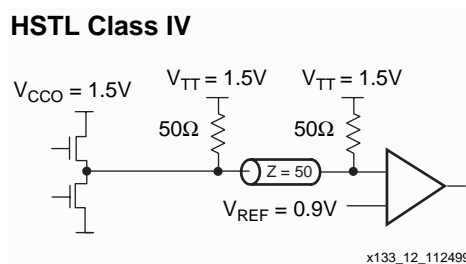


Figure 12: Terminated HSTL Class IV

Table 14: HSTL Class IV Standard

Parameter	Min	Typ	Max
$V_{CCO}$	1.40	1.50	1.60
$V_{REF}$	-	0.90	-
$V_{TT}$	-	$V_{CCO}$	-
$V_{IH}$	$V_{REF} + 0.1$	-	-
$V_{IL}$	-	-	$V_{REF} - 0.1$
$V_{OH}$	$V_{CCO} - 0.4$	-	-
$V_{OL}$	-	-	0.4
$I_{OH}$ at $V_{OH}$ (mA)	-8	-	-
$I_{OL}$ at $V_{OL}$ (mA)	48	-	-

**Notes:**

1. Per EIA/JESD8-6, "The value of  $V_{REF}$  is to be selected by the user to provide optimum noise margin in the use conditions specified by the user."

## SSTL3\_I

A sample circuit illustrating a valid termination technique for SSTL3\_I appears in Figure 13. DC voltage specifications appear in Table 15.

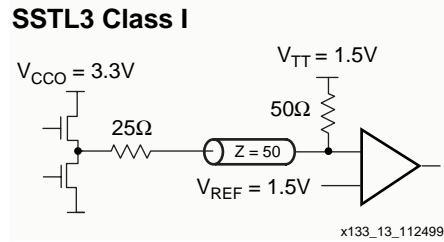


Figure 13: Terminated SSTL3 Class I

Table 15: SSTL3\_I Standard

Parameter	Min	Typ	Max
$V_{CCO}$	3.0	3.3	3.6
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} = V_{REF} + 0.2$	1.5	1.7	3.9 <sup>(1)</sup>
$V_{IL} = V_{REF} - 0.2$	-0.3 <sup>(2)</sup>	1.3	1.5
$V_{OH} = V_{REF} + 0.6$	1.9	2.1	-
$V_{OL} = V_{REF} - 0.6$	-	0.9	1.1
$I_{OH}$ at $V_{OH}$ (mA)	-8	-	-
$I_{OL}$ at $V_{OL}$ (mA)	8	-	-

**Notes:**

1.  $V_{IH}$  maximum is  $V_{CCO} + 0.3$ .
2.  $V_{IL}$  minimum does not conform to the formula.

## SSTL3\_II

A sample circuit illustrating a valid termination technique for SSTL3\_II appears in Figure 14. DC voltage specifications appear in Table 16.

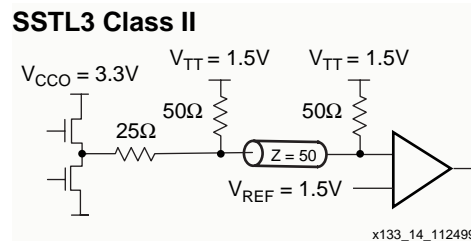


Figure 14: Terminated SSTL3 Class II

Table 16: SSTL3\_II Standard

Parameter	Min	Typ	Max
$V_{CCO}$	3.0	3.3	3.6
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} = V_{REF} + 0.2$	1.5	1.7	3.9 <sup>(1)</sup>
$V_{IL} = V_{REF} - 0.2$	-0.3 <sup>(2)</sup>	1.3	1.5
$V_{OH} = V_{REF} + 0.8$	2.1	2.3	-
$V_{OL} = V_{REF} - 0.8$	-	0.7	0.9
$I_{OH}$ at $V_{OH}$ (mA)	-16	-	-
$I_{OL}$ at $V_{OL}$ (mA)	16	-	-

**Notes:**

1.  $V_{IH}$  maximum is  $V_{CCO} + 0.3$ .
2.  $V_{IL}$  minimum does not conform to the formula.

**SSTL2\_I**

A sample circuit illustrating a valid termination technique for SSTL2\_I appears in Figure 15. DC voltage specifications appear in Table 17.

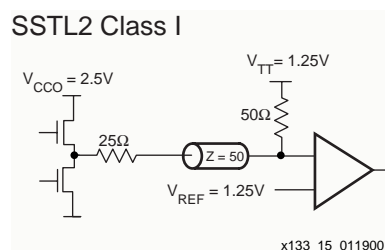


Figure 15: Terminated SSTL2 Class I

Table 17: SSTL2\_I Standard

Parameter	Min	Typ	Max
$V_{CCO}$	2.3	2.5	2.7
$V_{REF} = 0.5 \times V_{CCO}$	1.15	1.25	1.35
$V_{TT} = V_{REF} + N^{(1)}$	1.11	1.25	1.39
$V_{IH} = V_{REF} + 0.18$	1.33	1.43	3.0 <sup>(2)</sup>
$V_{IL} = V_{REF} - 0.18$	-0.3 <sup>(3)</sup>	1.03	1.17
$V_{OH} = V_{REF} + 0.05$	1.76	1.82	1.96
$V_{OL} = V_{REF} - 0.05$	0.54	0.68	0.74
$I_{OH}$ at $V_{OH}$ (mA)	-7.6	-	-
$I_{OL}$ at $V_{OL}$ (mA)	7.6	-	-

**Notes:**

1. N must be greater than or equal to -0.04 and less than or equal to 0.04.
2.  $V_{IH}$  maximum is  $V_{CCO} + 0.3$ .
3.  $V_{IL}$  minimum does not conform to the formula.

## SSTL2\_II

A sample circuit illustrating a valid termination technique for SSTL2\_II appears in Figure 16. DC voltage specifications appear in Table 18.

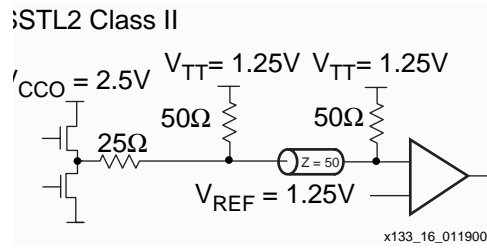


Figure 16: Terminated SSTL2 Class II

Table 18: SSTL2\_II Standard

Parameter	Min	Typ	Max
$V_{CCO}$	2.3	2.5	2.7
$V_{REF} = 0.5 \times V_{CCO}$	1.15	1.25	1.35
$V_{TT} = V_{REF} + N^{(1)}$	1.11	1.25	1.39
$V_{IH} = V_{REF} + 0.8$	1.33	1.43	3.0 <sup>(2)</sup>
$V_{IL} = V_{REF} - 0.8$	-0.3 <sup>(3)</sup>	1.07	1.21
$V_{OH}$	1.95	2.01	-
$V_{OL}$	-	0.49	0.55
$I_{OH}$ at $V_{OH}$ (mA)	-15.2	-	-
$I_{OL}$ at $V_{OL}$ (mA)	15.2	-	-

**Notes:**

1.  $N$  must be greater than or equal to  $-0.04$  and less than or equal to  $0.04$ .
2.  $V_{IH}$  maximum is  $V_{CCO} + 0.3$ .
3.  $V_{IL}$  minimum does not conform to the formula.

## CTT

A sample circuit illustrating a valid termination technique for CTT appears in Figure 17. DC voltage specifications appear in Table 19 .

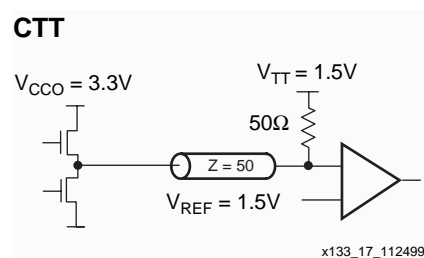


Figure 17: Terminated CTT

Table 19: CTT Standard

Parameter	Min	Typ	Max
$V_{CCO}$	2.05 <sup>1</sup>	3.3	3.6
$V_{REF}$	1.35	1.5	1.65
$V_{TT}$	1.35	1.5	1.65
$V_{IH} = V_{REF} + 0.2$	1.55	1.7	-
$V_{IL} = V_{REF} - 0.2$	-	1.3	1.45
$V_{OH} = V_{REF} + 0.4$	1.75	1.9	-
$V_{OL} = V_{REF} - 0.4$	-	1.1	1.25
$I_{OH}$ at $V_{OH}$ (mA)	-8	-	-
$I_{OL}$ at $V_{OL}$ (mA)	8	-	-

**Notes:**

1. Timing delays are calculated based on  $V_{CCO}$  min of 3.0V.

**PCI33\_3 and PCI66\_3**

PCI33\_3 or PCI66\_3 require no termination. DC voltage specifications appear in Table 20.

Table 20: PCI33\_3 and PCI66\_3 Standard

Parameter	Min	Typ	Max
$V_{CCO}$	3.0	3.3	3.6
$V_{REF}$	-	-	-
$V_{TT}$	-	-	-
$V_{IH} = 0.6 \times V_{CCINT}$	1.425	1.5	3.6
$V_{IL} = 0.4 \times V_{CCINT}$	-0.5	1.0	1.05
$V_{OH} = 0.9 \times V_{CCO}$	2.7	-	-
$V_{OL} = 0.1 \times V_{CCO}$	-	-	0.36
$I_{OH}$ at $V_{OH}$ (mA)	Note 1	-	-
$I_{OL}$ at $V_{OL}$ (mA) Timing delays are calculated based on $V_{CCO}$ min of 3.0V.	Note 1	-	-

**Notes:**

1. Tested according to the relevant specification.

## PCI33\_5

PCI33\_5 requires no termination. DC voltage specifications appear in [Table 21](#).

Table 21: PCI33\_5 Standard

Parameter	Min	Typ	Max
$V_{CCO}$	3.0	3.3	3.6
$V_{REF}$	-	-	-
$V_{TT}$	-	-	-
$V_{IH}$	1.425	1.5	5.5
$V_{IL}$	-0.5	1.0	1.05
$V_{OH}$	2.4	-	-
$V_{OL}$	-	-	0.55
$I_{OH}$ at $V_{OH}$ (mA)	Note 1	-	-
$I_{OL}$ at $V_{OL}$ (mA)	Note 1	-	-

**Notes:**

1. Tested according to the relevant specification.

## LVTTL

LVTTL requires no termination. DC voltage specifications appear in [Table 22](#).

Table 22: LVTTL Standard

Parameter	Min	Typ	Max
$V_{CCO}$	3.0	3.3	3.6
$V_{REF}$	-	-	-
$V_{TT}$	-	-	-
$V_{IH}$	2.0	-	5.5
$V_{IL}$	-0.5	-	0.8
$V_{OH}$	2.4	-	-
$V_{OL}$	-	-	0.4
$I_{OH}$ at $V_{OH}$ (mA)	-24	-	-
$I_{OL}$ at $V_{OL}$ (mA)	24	-	-

**Notes:**

1.  $V_{OL}$  and  $V_{OH}$  for lower drive currents are sample tested.

## LVCMOS2

LVCMOS2 requires no termination. DC voltage specifications appear in [Table 23](#).

**Table 23: LVCMOS2 Standard**

Parameter	Min	Typ	Max
$V_{CCO}$	2.3	2.5	2.7
$V_{REF}$	-	-	-
$V_{TT}$	-	-	-
$V_{IH}$	1.7	-	5.5
$V_{IL}$	-0.5	-	0.7
$V_{OH}$	2.4	-	-
$V_{OL}$	-	-	0.4
$I_{OH}$ at $V_{OH}$ (mA)	-12	-	-
$I_{OL}$ at $V_{OL}$ (mA)	12	-	-

## AGP-2X

The specification for the AGP-2X standard does not document a recommended termination technique. DC voltage specifications appear in [Table 24](#).

**Table 24: AGP-2X Standard**

Parameter	Min	Typ	Max
$V_{CCO}$	3.0	3.3	3.6
$V_{REF} = N \times V_{CCO}^{(1)}$	1.17	1.32	1.48
$V_{TT} = V_{REF}$	1.35	1.5	1.65
$V_{IH} = V_{REF} + 0.2$	1.37	1.52	-
$V_{IL} = V_{REF} - 0.2$	-	1.12	1.28
$V_{OH} = 0.9 \times V_{CCO}$	2.7	3.0	-
$V_{OL} = 0.1 \times V_{CCO}$	-	0.33	0.36
$I_{OH}$ at $V_{OH}$ (mA)	Note 2	-	-
$I_{OL}$ at $V_{OL}$ (mA)	Note 2	-	-

**Notes:**

1. N must be greater than or equal to 0.39 and less than or equal to 0.41.
2. Tested according to the relevant specification.

## Revision History

The following table shows the revision history for this document.

Date	Version	Revision
11/24/99	1.0	Initial release.
07/23/02	2.0	Added Spartan-IIE specifications.