TIMING, TRIGGER AND CONTROL INTERFACE MODULE FOR ATLAS SCT READ OUT ELECTRONICS

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ABSTRACT

The SCT detector interfaces with the ATLAS Level 1 using the LHC-wide TTC (Timing, Trigger, and Control) system. The design of the TIM (TTC Interface Module), part of the SCT off-detector electronics [1], and the interface with the RODs (Read Out Drivers), is described.

Also described is the forerunner of the TIM, the CLOAC (Clock And Control) MASTER module, developed to provide a stand-alone timing and trigger capability in the absence of the TTC system. CLOACs are currently used in the SCT tests at CERN. They are also available to the SCT community for use in front-end modules testing.

1. INTRODUCTION

The SCT interface with ATLAS Level 1 receives the signals through the Timing, Trigger, and Control (TTC) system [2] and returns the SCT Busy signal to the Central Trigger Processor (CTP). It interfaces with the SCT off-detector electronics, in particular with the Read-Out Driver (ROD), and is known as the SCT TTC system .

The SCT TTC system consists of the standard TTC system distributing the signals to a custom TTC Interface Module (TIM) in each crate of RODs. In addition, a Busy module returns the SCT Busy signal.

This paper and the accompanying diagrams describe the essential features of the TIM. For further details refer to the interface specification documents [3] [4] [5]. The TIM module also has to satisfy the requirements set out in the SCT TTC Interface Requirements document [6].

(By the way – these documents have been shown to be useful in getting engineers in different countries, and continents, to come to an agreement on how to make their modules understand each other. Provided they are not too long, of course, otherwise there is no time and no inclination to read them !)

2. TIM

2.1 Functionality

The diagram (Fig.1) illustrates the main function of the TIM, which is to interface the off-detector electronics, in particular the ROD, with the outside world of Level-1 electronics. Diagrams showing an overview of the SCT system [7] and the TTC context [8] are also available.

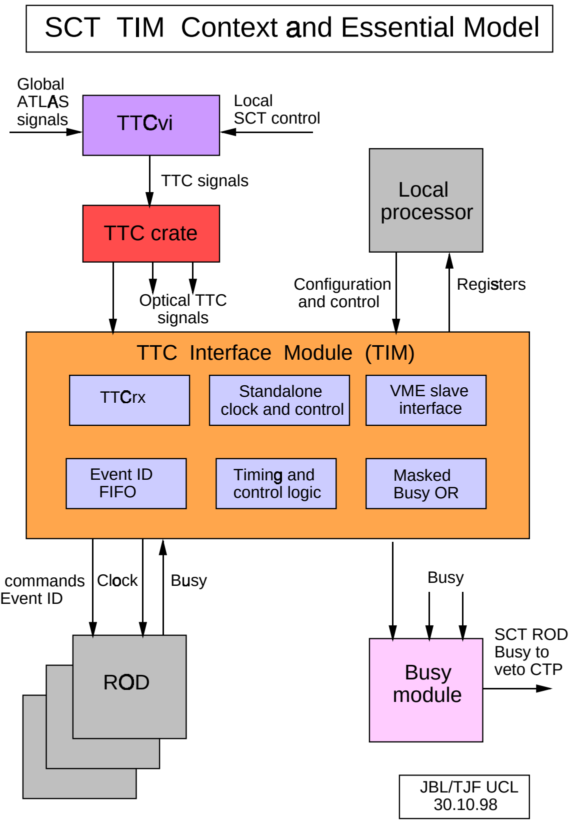
SCT TIM Context and Essential Model
Global ATLAS signals
TTCvi
Local SCT control
TTC signals
TTC crate
Local processor
Optical TTC signals
Configuration and control
Registers
TTC Interface Module (TIM)
TTCrx
Standalone clock and control
VME slave interface
Event ID FIFO
Timing and control logic
Masked Busy OR
Fast commands and Event ID
Clock
Busy
Busy
ROD
Busy module
SCT ROD Busy to veto CTP
JBL/TJF UCL 30.10.98

Fig. 1 : SCT TIM Context and Essential Model

- The TIM transmits the clock, fast commands and event ID from the TTC system to the RODs with minimum latency. The clock is also transmitted to the Back-Of-Crate optocards (BOC)
- The TIM passes the Busy from the RODs via a Busy module to the CTP in order to stop it sending triggers
- The TIM can send stand-alone clock, fast commands and event ID to the RODs under control of the local processor
- The TIM has programmable timing adjustments and control functions
- The TIM has a VME slave interface to give the local processor read and write access to its registers
- The TIM is configured by the local processor setting up TIM's registers. They can be inspected by the local processor

2.2 TTC Interface

The TIM receives the TTC signals and passes the required subset to the RODs (Fig. 2).

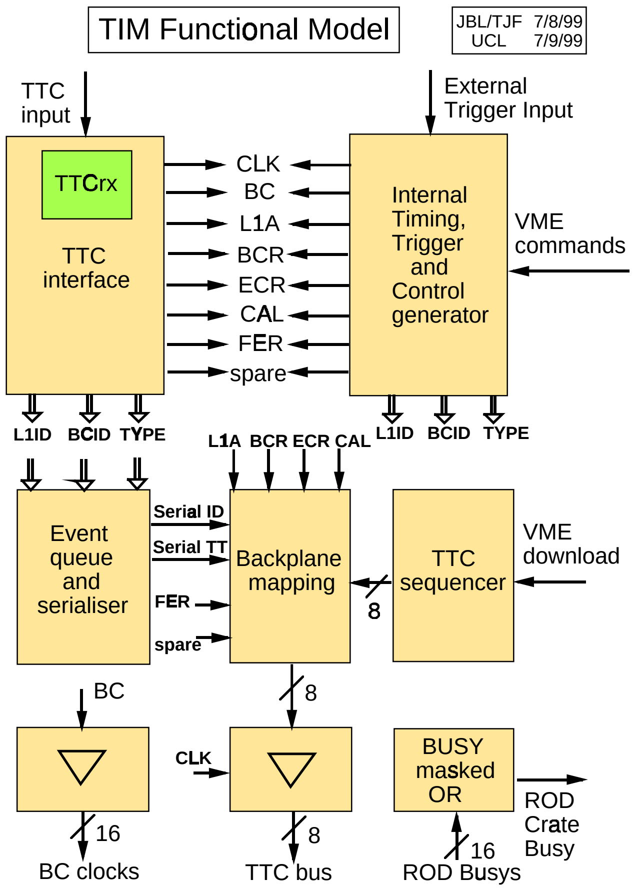
TIM Functional Model
JBL/TJF 7/8/99
UCL 7/9/99
TTC input
External Trigger Input
TTCrx
TTC interface
CLK
BC
L1A
BCR
ECR
CAL
FER
spare
Internal Timing, Trigger and Control generator
VME commands
L1ID
BCID
TYPE
L1A
BCR
ECR
CAL
L1ID
BCID
TYPE
Event queue and serialiser
Serial ID
Serial TT
FER
spare
Backplane mapping
8
TTC sequencer
VME download
BC
8
CLK
BUSY masked OR
ROD Crate Busy
16
BC clocks
8
TTC bus
16
ROD Busys

Fig. 2 : TIM Functional Model

The optical TTC signals are received by a receiver section containing a standard TTCrx receiver chip, which decodes the TTC information into electrical form.

The TTC information, required by the RODs and by the SCT FE electronics, is the following :

Clock :	BC	Bunch Crossing clock
Fast command :	L1A	Level-1 Accept
	ECR	Event Counter Reset
	BCR	Bunch Counter Reset
	CAL	Calibrate signal
Event ID :	L1ID	24-bit Level-1 trigger number
	BCID	12-bit Bunch Crossing number
	TTID	8-bit Trigger Type

The TIM outputs the above information onto the backplane of a ROD crate with the appropriate timing. The event ID is transmitted with a serial protocol and so a FIFO (First In First Out) buffer is required in case of rapid triggers (Fig. 3).

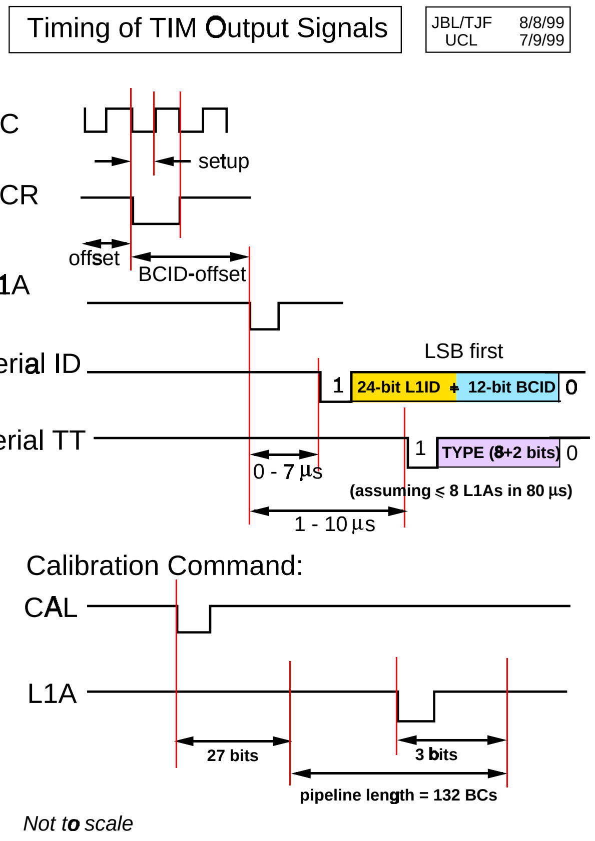
Timing of TIM Output Signals
JBL/TJF 8/8/99
UCL 7/9/99
BC
setup
BCR
offset
BCID-offset
L1A
LSB first
Serial ID
1
24-bit L1ID
12-bit BCID
0
Serial TT
1
TYPE (8+2 bits)
0
0 - 7 µs
(assuming ≤ 8 L1As in 80 µs)
1 - 10 µs
Calibration Command:
CAL
L1A
27 bits
3 bits
pipeline length = 132 BCs
Not to scale

Fig. 3 : Timing of TIM Output Signals

An additional FER (Front End Reset) signal, which may be required by the SCT FE electronics, can also be generated, either by the SCT-TTC or by the TIM.

The TIM can also generate all the above information stand-alone at the request of the local processor. It can also be connected to another TIM for stand-alone multi-crate operation for system tests in the absence of TTC signals.

The TIM does a masked OR of the ROD Busy signals in each crate and outputs the overall crate Busy to a BUSY module [9]. It is intended to implement the monitoring functionality of the BUSY module on TIM .

2.3 Hardware Implementation

The TTC interface is based on the standard TTCrx receiver chip, together with the associated PIN diode and preamplifier developed by the RD12 group at CERN, as described elsewhere [10]. This provides the BC clock and all the signals as listed in section 2.2 above.

The BC clock destined for the BOCs and RODs, with the timing adjusted on the TTCrx, is passed via differential PECL drivers directly onto the point-to-point backplane tracks. These are designed to be of identical length for all the slots in each crate to provide a synchronised timing marker. All the fast commands are also clocked directly, without any local delay, onto the backplane to minimise the TIM latency budget [11].

Apart from the BC clock normally provided by the TTCrx, the TIM generates its own 40.08 MHz internal clock. This, as well as the externally input ECL or NIM clocks, can be selected by the local processor to drive the TIM and generate the backplane clocks. To ensure the identical timing relationship as when using the BC clock, an additional programmable delay is provided in the internal clock circuit.

Timing adjustments and setting of various delays is an important part of the TIM operation. There are fine and coarse delays for the BC clock and the TTC fast commands incorporated on the TTCrx. In addition, TIM provides further fine delay to the clock used for the timing of the backplane signals (Fig. 4).

The L1ID, the BCID and the TTID information for at least eight subsequent events (assuming the current ATLAS restriction of a maximum of 8x L1As in 80 usec) are required to be buffered and serialised onto two event ID backplane lines. Remaining circuitry consists mainly of the mapping required to provide 8 individually selectable signal lines to be output and bussed across the VME backplane, and of the necessary synchronising and buffering required to obtain sufficiently stable setup and hold times for all the RODs in each VME crate [12]. Most of this is implemented using MACH-5 programmable logic devices.

All the 8 backplane signals, which normally come from the TTC, are also capable of being either generated on the command of the local processor, or automatically by the TIM under local processor control. Further details of the stand-alone capabilities of the TIM are described below in the CLOAC MASTER Functionality section 3.1.

In addition, a sequencer, using 8x32k RAM, is provided to allow long sequences of commands and ID data to be written in by the local processor and used for testing the FE and off-detector electronics [13].

There is also a complete set of external inputs for clock and all the above signals on the front panel in both NIM and differential ECL. All the backplane signals are also mirrored as differential ECL outputs on the front panel to allow TIM interconnection.

Most of the logic circuitry required for the stand-alone operation is also contained on a number of PLDs, with only the buffering of the various inputs and outputs being done by separate integrated circuits [14].

The TIM has been designed as a 9U, single width, VME module, with a standard VME slave interface. A24/D16 or A32/D16 access is selectable, with the base address A16 – A23 (or A16 - A31) preset as required. A combination of FastTTL, ECL, PECL and LV BiCMOS devices is used, requiring +5V, +3V3 and -5V2 voltage supplies.

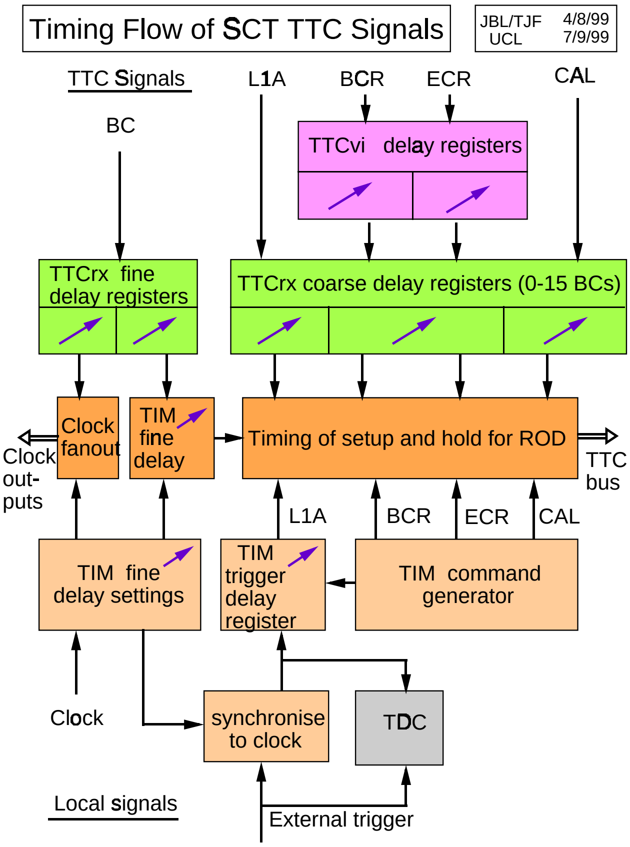

Fig. 4 : Timing Flow of SCT - TTC Signals

3. CLOAC

To prototype some of the stand-alone functionality of the TIM, and to generate the clock and fast commands to enable front-end modules to be tested in the absence of the TTC system, the CLOAC (Clock And Control) MASTER module has been designed [15].

3.1 Functionality

The CLOAC MASTER module generates the clock and all the fast commands as discussed in section 2.2 above, either on command from a local processor or fully stand-alone.

The triggers can either be issued singly or repetitively, with the number of triggers programmable (from 0 to 65535, or continuous) and their frequency fully programmable and selectable as either a single frequency (in the range 50 Hz – 600 kHz), or with an average random rate (between 12.5 Hz – 150 kHz). There is also a fully programmable "latency" delay (of 0 - 143 clock periods) between the receipt of an external trigger and the issue of the trigger to the FE module.

The calibration pulse is followed by an automatically generated calibration trigger after a delay, programmable in the same range of 0 – 143 clock periods, so it is received when data is at the end of the pipeline (of 132 BCs). Either single or multiple (0 to 65535) calibration pulses can be selected, with a minimum repetition period of about 84 usec (depending on the programmed calibration trigger delay).

The capability of being able to issue a precise number of triggers or calibration pulses very fast is useful for obtaining histograms from the FE readout data.

Internally generated Soft Reset signals are issued at a programmable frequency (between 0.05 Hz - 60 Hz) and BC Reset at a preset frequency of about 11.2456 kHz (the LHC beam orbit rate) .

The CLOAC MASTER can also synchronise to an external clock and can accept external fast commands provided as NIM or differential ECL inputs. It can receive BUSY inputs to provide a masked BUSY output.

A basic trigger "window", capable of being programmed in width and delay (0 to 24 nsec in steps of 1 nsec) with respect to the received clock, is also available to assist with random trigger tests (eg. using cosmics or test beams).

A combination of these fast commands, selected by the local processor, is synchronised to the selected clock. The commands are then converted to command strings (fully programmable, but normally set to the values specified by the SCT front-end ASIC chip protocol [16]) and mixed together, using a priority selector to avoid the issue of simultaneous commands.

Additionally, a programmable slow command of up to 64 bits long can be issued to provide a very basic setting-up capability for the FE modules.

The CLOAC MASTER provides four separate electrical outputs of the clock and command strings in differential ECL to allow direct connection to four FE modules in the absence of RODs.

(Note : The TIM will not be capable of issuing command strings since normally this functionality will be provided by the RODs).

3.2 Hardware Implementation

The CLOAC MASTER module has been implemented as a 6U PCB with a standard A24 / D16 VME slave interface (Fig. 5). All the logic circuitry, including the VME interface, reside on three MACH-5 PLDs. A combination of FastTTL and ECL devices has been used, requiring +5V and –5V2 supplies.

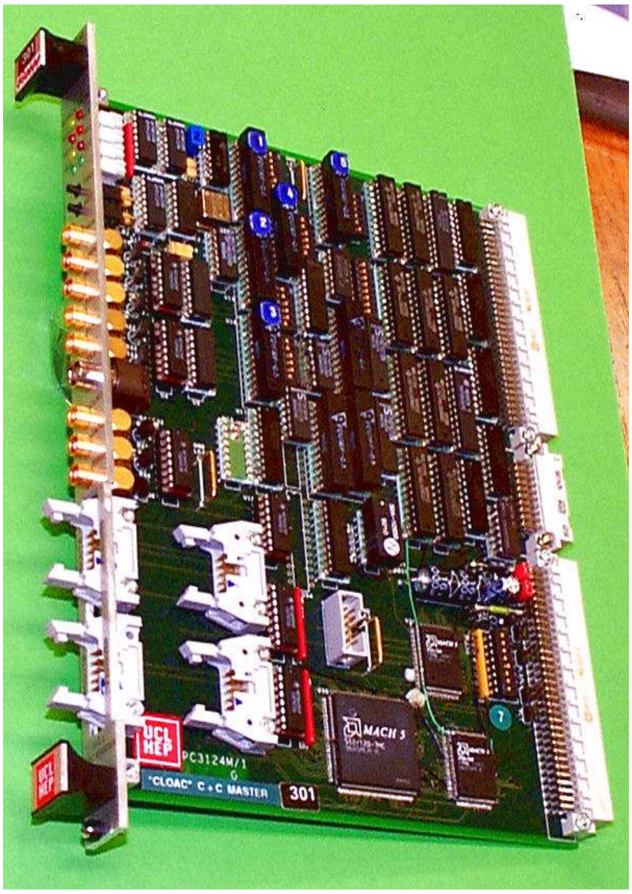

Fig. 5 : Picture of CLOAC MASTER module

Some CLOAC MASTER modules have been used in the SCT system and beam tests at CERN since 1998.

An additional number of CLOAC MASTER modules has been manufactured and made available to the SCT community for testing FE modules in combination with MuSTARD and SLOG modules [17].

Additionally, a number of CLOAC FANOUT modules has also been produced which provide 7 separate clock and data differential ECL outputs each (Fig. 6).

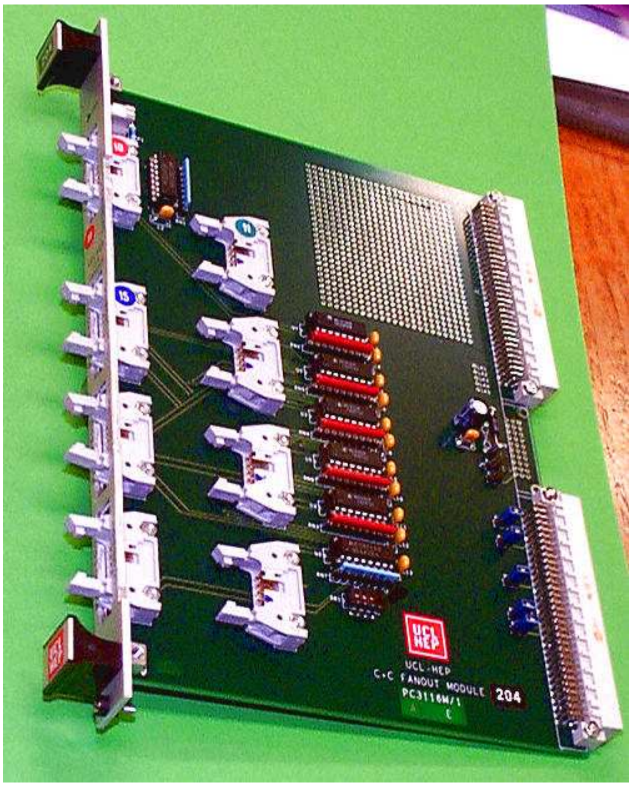

Fig. 6 : Picture of CLOAC FANOUT module

4. ACKNOWLEDGEMENTS

We would like to thank Professor Tegid W. Jones for his continuous support of our work in the ATLAS collaboration. We also wish to thank Janet Fraser who, at short notice and despite her own ATLAS - SCT work, helped to produce the diagrams and the overhead transparencies used in this paper.

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[16] SCT Electronics :
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[17] System and Beam Tests Setup :
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6. FIGURES :

Fig. 1 SCT TIM Context and Essential Model :
http://www.hep.ucl.ac.uk/~mp/TIM_figure.pdf
Fig. 2 TIM Functional Model :
http://www.hep.ucl.ac.uk/~mp/TIM_Functional_model.eps
Fig. 3 Timing of TIM Output Signals :
http://www.hep.ucl.ac.uk/~mp/TIM_Outputs_timing.eps
Fig. 4 Timing Flow of SCT-TTC signals :
http://www.hep.ucl.ac.uk/~mp/TIM_Timing_flow.eps
Fig. 5 Picture of CLOAC MASTER module :
http://www.hep.ucl.ac.uk/~tjf/bd2nov.jpg
Fig. 6 Picture of CLOAC FANOUT module :
http://www.hep.ucl.ac.uk/~tjf/bd1nov.jpg