

# **TIM ( TTC Interface Module ) for ATLAS SCT & PIXEL Read Out Electronics**

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## ***Abstract***

The design, functionality, description of hardware and firmware of the TIM ( TTC Interface Module ) are described.

The TIM is the standard SCT and PIXEL detector interface module to the ATLAS Level-1 Trigger, using the LHC-standard TTC ( Timing, Trigger and Control ) system.

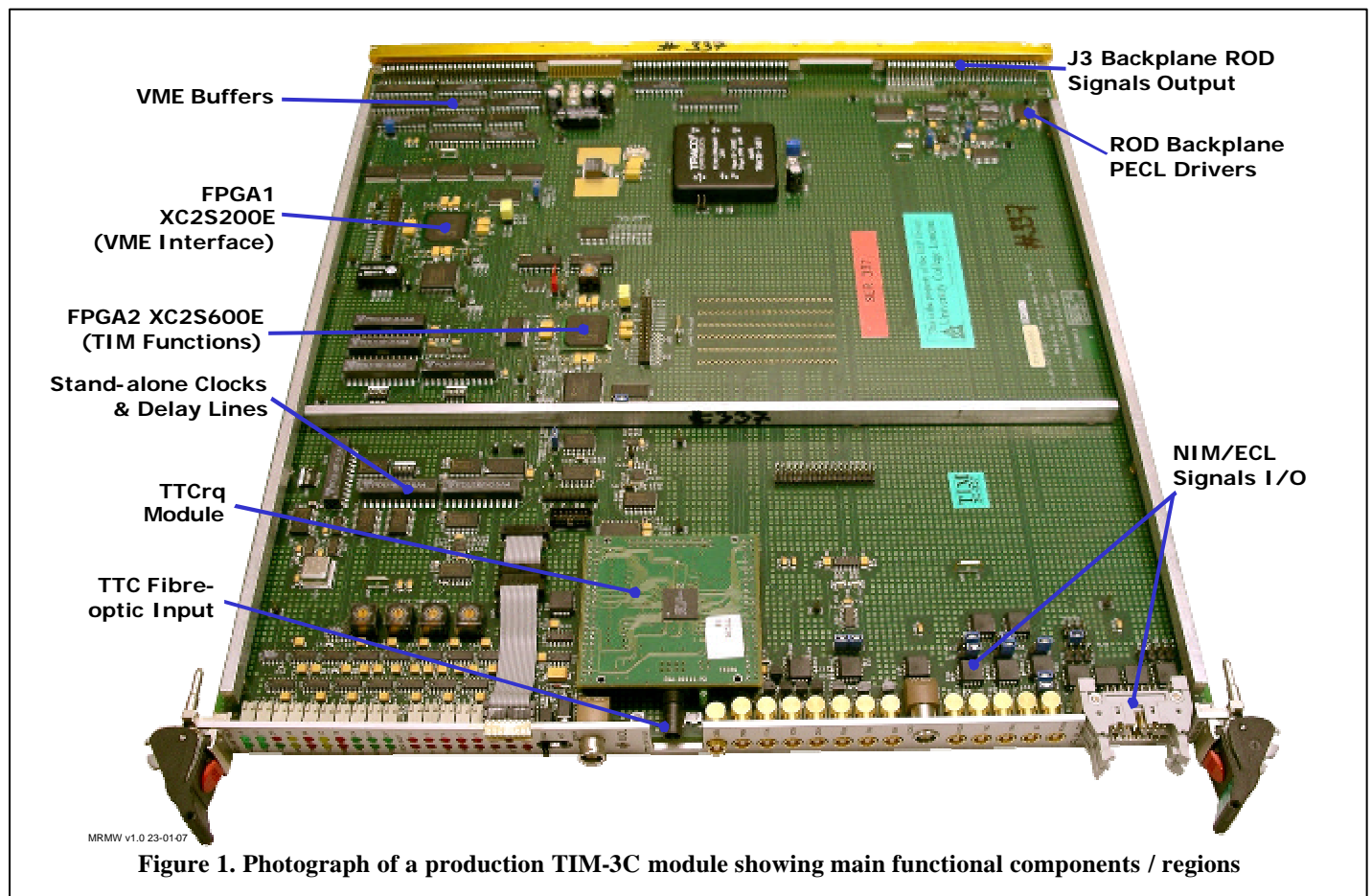
The first two prototypes TIM-0 was designed and built during 1999 and 2000.

Twelve prototype TIM-1s and TIM-2s, based on ten AMD/Lattice CPLD devices, have been produced in 2001-2004. They were used at various SCT assembly sites, at the SCT and Pixel test-beams and the ROD-DAQ development sites.

Twenty-four final production TIM-3C modules, manufactured in 2004 - 2005, are based on two Xilinx FPGAs. The details of the transition in hardware and firmware from CPLD to FPGA are described below.

Additionally, further twenty-four TIM-3 modules were also manufactured in 2005 for use by the CSC and MDT muon detectors.

It has been our aim from the start of the design work to make all versions TIM compatible as far as the end users are concerned. Details of the TIM requirements and operation are detailed in [ 1 ] as well as in three papers [ 2,3,4 ].



## I. INTRODUCTION

This paper and the accompanying diagrams describe some hardware details of the TIM and their functionality. It should be read in conjunction with the other specification documents [ 5 ], [ 6 ], [ 7 ], [ 8 ] and [ 9 ].

The TTC Interface Module ( TIM ) interfaces the ATLAS Level-1 Trigger system signals to the Read-Out Drivers ( RODs ) of the SCT and PIXEL inner sub-detector ( as well as the MDT and CSC muon sub-detector ). Clock and trigger signals are received from the Timing, Trigger and Control ( TTC ) system [ 10 ] and a busy signal is returned to the Central Trigger Processor ( CTP ). These interfaces can be seen in Figure 2.

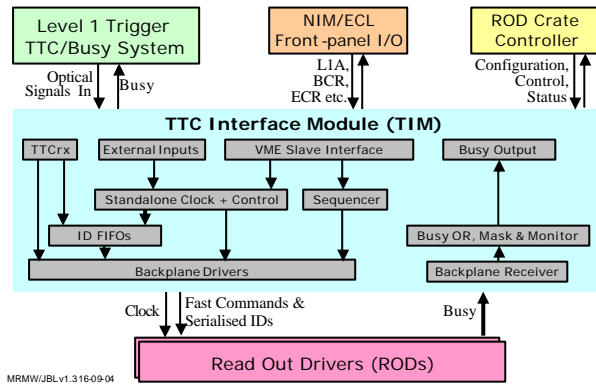


Figure 2 : TIM interfaces and main functional blocks

## II. FUNCTIONALITY

The diagram ( Fig. 3 below ) shows the functional model of the TIM, and illustrates the principal functions of the TIM modules :

- To transmit the fast commands and event ID from the TTC system to the RODs with minimum latency. The clock is first transmitted to the Back-Of-Crate optocards ( BOC ) , from where it is passed to the RODs
- To pass the masked Busy from the RODs to the CTP in order to stop it sending triggers
- To generate and send stand-alone clock, fast commands and event ID to the RODs under control of the local processor

In addition to these main functions, the TIM has also the following capabilities :

- The TIM has programmable timing adjustments and control functions
- The TIM has a VME slave interface to give the local processor read and write access to its registers [ 11 ]
- The TIM is configured by the local processor setting up TIM's registers. They can be inspected by the local processor.

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Figure 3 : TIM Functional Model

The TTC information, required by the RODs and by the SCT or PIXEL FE ( Front End ) electronics, is the following :

Clock :	BC	Bunch Crossing clock
Fast command :	L1A	Level-1 Accept
	ECR	Event Counter Reset
	BCR	Bunch Counter Reset
	CAL	Calibrate signal
Event ID :	L1ID	24-bit Level-1 trigger number
	BCID	12-bit Bunch Crossing number
	TTID	8-bit Trigger Type ( + 2 spare bits )

The TIM outputs the above information onto the backplane of a ROD crate with the appropriate timing. The event ID is transmitted with a serial protocol and so a FIFO ( First In First Out ) buffer is required in case of rapid triggers.

An additional FER ( Front End Reset ) signal, which may be required by the SCT FE electronics, can also be generated, either by the SCT-TTC or by the TIM. At present, it is proposed that FER is carried out by the ECR.

The optical TTC signals are received by a receiver section containing a standard TTCrx receiver chip, which decodes the TTC information into electrical form [ 12 ].

The TIM can also generate all the above information stand-alone at the request of the local processor. It can also be connected to another TIM for stand-alone multi-crate operation for system tests in the absence of TTC signals.

Detailed flowcharts [ 13 ] show the differences of the sources and of the flow of the fast commands [ 14 ] and event ID information on TIM, finally producing the same output to the RODs via the backplane.

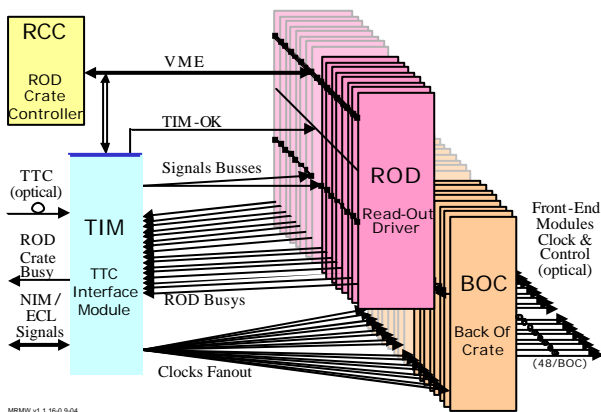
Another diagram [ 15 ] shows the flow, the distribution and the programmable delays of the clocks in both the “Run” and the “SA” modes.

It is important to note that in the “Run” mode [ 16 ] the priority is given to passing the BC clock and commands to the RODs, in their correct timing relationship, with the absolute minimum of delay to reduce the latency.

In the “SA” mode, both the clock and the commands can arrive from a variety of sources [ 17 ]. The clock can be either generated on-board using an 80.16 MHz crystal oscillator, or arrive from external sources in either NIM or differential ECL standards. Similarly, the fast commands can be generated on the command of the local processor, or automatically by the TIM under local processor control. The fast commands can also be input from external sources in either NIM or differential ECL [ 18 ]. Thus, any of these internally or externally generated commands must be synchronised to whichever clock is being used at the time, to provide the correctly timed outputs.

In addition, a ‘sequencer’, using 8x32k RAM, is provided to allow long sequences of commands and serial ID data to be written in by the local processor and used for testing the FE and off-detector electronics. A ‘sink’ ( receiver RAM ) of the same size is also provided to facilitate off-line checking of commands and ID data sent to the RODs [ 19 ].

All the backplane signals are also mirrored as differential ECL outputs on the front panel to allow TIM interconnection.



**Figure 4 : TIM connections in a ROD-crate**

The TIM produces a masked OR of the ROD Busy signals in each crate and outputs the overall crate Busy to a separate

BUSY module. A basic ROD BUSYs monitoring is also available on TIM.

A single TIM distributes the clock and trigger signals to a maximum of 16 RODs with their associated Back-Of-Crate cards ( BOCs ). Communication is via a custom J3 backplane in a 9U VME64x crate.

Each ROD returns an individual busy signal to the TIM, where a crate-busy signal is generated. Figure 4 shows these connections graphically.

### III. HARDWARE IMPLEMENTATION

The TIM has been designed [ 20 ] as a 9U, single width, VME64x module, with a standard VME slave interface. A24/D16 or A32/D16 - D32 access is selectable, with the base address A16 – A23 ( or A16 - A31 ) being either preset as required, or set by the geographical address of the TIM slot in each ROD crate. Full geographical addressing ( GA ) and interrupts ( e.g. for clock failure ) are available if required.

On the TIM module, a combination of FastTTL, LVTTTL, ECL, PECL and LV BiCMOS devices is used, requiring +5V, +3V3 and +/- 12V ( to produce -5V2 ) voltage supplies.

The TTC interface is based on the standard TTCrx receiver chip, together with the associated PIN diode and preamplifier developed by the RD12 group at CERN, as described elsewhere [ 12 ]. This provides the BC clock and all the signals as listed in section A above. On the TIM modules, the TTCrq ( or TTCrm ) mezzanine board [ 21 ] is used to allow an easy replacement if required.

The BC clock destined for the BOCs and RODs, with the timing adjusted on the TTCrx, is passed via differential PECL drivers [ 22 ] directly onto the point-to-point parallel impedance-matched backplane tracks. These are designed to be of identical length for all the slots in each crate to provide a synchronised timing marker. All the fast commands are also clocked directly, without any local delay, onto the backplane to minimise the TIM latency budget [ 23 ].

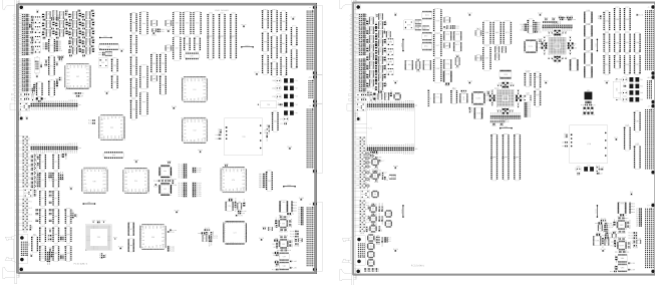
#### A. PROGRAMMABLE LOGIC

The TIM prototypes were produced using 10 AMD/Lattice MACH5 CPLDs on each board. As this device family, its firmware language ( DSL ) and its associated compiler / fitter ( MachXL ) are now obsolete and unsupported, a more flexible configuration was sought.

We selected the Xilinx Spartan IIE FPGA series, as our ROD collaborators already had experience with Xilinx, and new Spartan IIE devices were being released at the time ( ensuring maximal protection against obsolescence ) that matched our requirement. These devices contain enough RAM

resources to allow the prototype TIM's discrete RAMs and FIFO devices to be incorporated into the FPGA [ 25 ].

The production TIM design uses two FPGAs per board - lowering costs - with much increased logic resources and flexibility for expansion. Figure 5 shows differences in programmable-logic PCB area utilised ( including the RAMs and FIFOs ) between the prototype and production version.



**Figure 5 : Filled blocks show programmable-logic, RAM and FIFO on CPLD (left) and FPGA (right) based TIMs**

## B. OTHER HARDWARE CHANGES

The TIM will always attempt to provide a clock to all of the RODs in its crate. It is able to switch between different sources without a glitch, and in the case of a clock failure, does so automatically. To achieve this, dedicated clock-multiplexer devices have been utilised.

These devices [ 24 ] switch automatically to a back-up clock if the selected clock is absent. Using clock detection circuits, errors can be flagged and transmitted to all the RODs in the crate via a dedicated backplane line ( TIM-OK ), allowing RODs to tag events accordingly. This system is shown in [ 26 ].

Additional control and clock connections have been added to allow configuration of the QPLL on the TTCrx [ 21 ] version of the TTCrx mezzanine.

An open-collector busy output option ( jumper configurable ) has been added to allow a wired-OR of busy from multiple TIMs to be sent to a single busy input [ 27 ].

## IV. FIRMWARE

The firmware for the production TIM is a re-write of the original DSL in VHDL. As VHDL is supported by most hardware and software vendors, with a large developer base, we are optimistic that the code will be maintainable over the lifetime of the board.

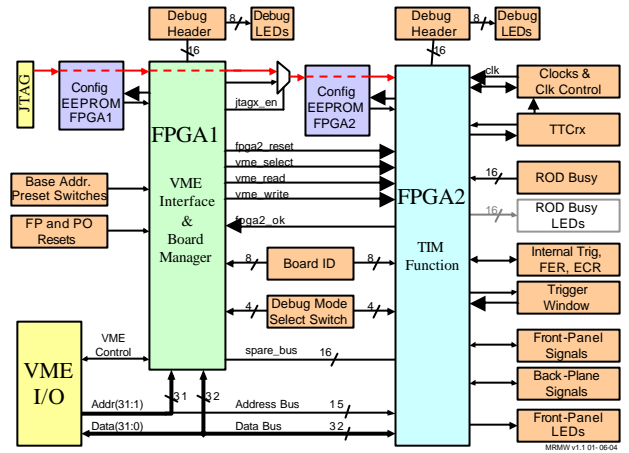
## A. OVERALL STRUCTURE

The production TIM design uses two FPGA's specifically to perform two different roles.

FPGA1 is the board manager – supporting the more generic board functions: VME Interface, local bus control, board reset and provides status information on FPGA2.

FPGA2 hosts all the TIM specific functions and provides interfaces to front-panel and ROD backplane signals.

With this partitioning it is envisaged that firmware for FPGA1 will stabilise earlier than FPGA2 allowing remote updates. Figure 6 shows the functional connections.



**Figure 6 : TIM Functional layout**

## B. NEW FUNCTIONALITY

The prototype TIM was capable of all of the original TIM requirements [ 6 ]. The production TIM is a drop-in replacement for the prototype. By moving components like the FIFOs into the FPGA we are now also able to accommodate requests for additional functions – e.g. the new orbit counter and event-counter-reset ID.

Aside from some additional debug registers, the only new functionality specific to the production TIM at present relates to resonating wire-bonds from fixed-frequency triggers, as detailed in the next section.

## V. RESONATING WIRE-BONDS

Triggers can initiate increased activity in some parts of front-end electronics. This can lead to large variations in the current flowing through some wire-bonds between read-out and idle times. On CDF, trigger rates close to the mechanical resonant frequency of a wire-bond in a strong magnetic field have been seen to cause the bond-wires to oscillate to destruction [ 28 ].

In ATLAS, physics triggers are random, and have very little chance of damaging a wire-bond [ 29 ], but calibration and test runs can easily generate triggers at fixed frequencies.

To understand this problem in the context of the SCT, studies were undertaken with test wire-bonds. Although it was found that the SCT wire-bonds were not at risk - they are oriented parallel to the magnetic field on the barrel and are short enough on the end-caps to not resonate within the trigger frequency range – some protection may still benefit the life-time of the detector.

### ***A. FIXED FREQUENCY TRIGGER VETO***

A single TIM distributes triggers to +/-500 front-end modules within a sub-detector partition. It can also generate triggers, some from its own trigger oscillator. This, coupled with it being responsible for sending a busy to the CTP that can stop triggers, makes it a good place to locate some sub-detector specific trigger management logic.

The Fixed Frequency Trigger Veto (FFTV ) module is tasked with identifying this type of trigger, and stopping them. Although Fast Fourier Transforms seem ideally suited to the task, the large amount of logic resources required and the complexity of the system led us to try something simpler.

Using an algorithm from CDF [ 29, 30 ] as a basis, we compare successive trigger periods and increment a counter if they match ( within a programmable tolerance ). By setting maximum and minimum values for trigger period, outside of which no action is taken, we can tune the system for a specific band of triggers.

During LHC machine testing, it is likely that runs with one bunch in the machine will take place. These will generate triggers at a fixed frequency ( ~11.2kHz ), but below the band of danger to wire-bonds. By tuning the FFTV to ignore these, the SCT will not compromise these important runs.

To ensure the FFTV does not interfere with ATLAS data taking its operation needs to be compatible with the Level-1 Trigger system. In run mode vetoing triggers independently will cause mis-aligned trigger-numbers and render all events after that point unusable. TIM will therefore assert the busy when fixed frequency triggers are encountered. The time spent in this state will be counted, allowing the contribution to dead-time to be monitored.

### ***B. LOCAL EMERGENCY ACTION***

In the case where triggers are received by TIM (or ROD) after the Veto has been asserted, a Local Emergency Action must prevent these triggers reaching the modules. In this case triggers will be discarded, the ROD-Busy will be set for an indefinite period, and flags raised to signal the run should be terminated [ 30 ]. To allow for the round-trip time from sending the ROD-Busy signal to the CTP and triggers stopping, a short delay between Veto and Emergency Action is allowed for ( ~2usec ).

To ensure the FFTV is not accidentally disabled, TIM users are required to insert a jumper and set a bit in software before trigger vetoing is inhibited.

In stand-alone mode the TIM generates the trigger numbers internally, so the veto can stop triggers before this is done.

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## VII. FIGURES

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- Fig. 2 TIM interfaces and main functional blocks :  
[http://www.hep.ucl.ac.uk/atlas/sct/tim/TIM\\_essential\\_model.pdf](http://www.hep.ucl.ac.uk/atlas/sct/tim/TIM_essential_model.pdf)
- Fig. 3 TIM Functional Model :  
[http://www.hep.ucl.ac.uk/~jbl/SCT/diagrams/TIM\\_model.pdf](http://www.hep.ucl.ac.uk/~jbl/SCT/diagrams/TIM_model.pdf)
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- Fig. 6 TIM-3 Functional Layout  
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