



FDR of the SCT/Pixel TIM Module

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REPORT OF THE FINAL DESIGN REVIEW

SCT/PIXEL TIM MODULE

Abstract

The FDR of the TIM module was held at CERN on June 28th 2004. No show stoppers were detected. A list of recommendations is given.

Prepared by :

P. Farthouat, Cern

Checked by :

**S. Baron, Cern
G. Perrot, LAPP**

Approved by :

M. Nessi

*for information,
you can contact :*

Ph. Farthouat

Tel.

+41.22.767 6221

Fax.

+41.22.767 8350

E-Mail

Philippe.Farthouat@cern.ch

Distribution: EB Members, SCT Members, all participants mentioned in the report.

PURPOSE OF THIS REVIEW

The objective of the review was to check that the TIM module as designed satisfy the SCT and Pixel requirements.

MEMBERS OF THE REVIEW COMMITTEE

Review Committee

S. Baron, Cern
Ph. Farthouat, Cern
G. Perrot, LAPP

SCT ROD-BOC Team

J.M. Butterworth, UCL
J. Carter, Cambridge
J. Hill, Cambridge
J.B. Lane, UCL
M. Postranecky, UCL
M. Warren, UCL

Ex officio

A. Grillo, Santa-Cruz
M. Nessi, CERN
M. Tyndel, RAL
S. Stapnes, CERN

For Information

T. Weidberg, Oxford

AGENDA

The agenda and documentation are available at

<http://agenda.cern.ch/fullAgenda.php?ida=a042186>

OUTCOMES OF THE REVIEW

Busy Distribution Scheme

It seems wise that the busy from each ROD crate goes to the Busy module in the TTC crate to do the “or” of the 2 crates before transmission to the LTP, rather than having a chained busy which would cause problems in case one crate is off.

VME Interface

A full D32 mode should be implemented.

L1A Id in different part of system

The L1ID 24 bits and ECR counter could be combined at the same place in the TIM before being transmitted to the ROD instead of duplicating the ECR counter in each ROD. It is a matter of choice, but duplicating several counters all over the system increases the probability of de-synchronisation. This would also apply to the BCID if it becomes 32 bits. It might be necessary to implement that on the spare transmission line as it might take too much time to transmit serially all the information (L1AID,BCID,TT) on a single line.

L1A ID and BCID need to be modified at the ROD level to maintain coherency with the rest of ATLAS. The offsets to be applied must be rechecked.

QPLL Unlock

The unlocking of the QPLL when transmitting triggers need to be understood (with Sophie) as soon as possible.

Resonance problem

The proposed scheme of introducing dead-time in case of danger has been approved by the Level-1 trigger team and should be implemented. The exact algorithm has still to be optimised in order to minimise the overall ATLAS dead-time; it is for instance useless to maintain a BUSY active as long as there is a fixed frequency trigger (in the bad range) when introducing dead-time half of the time would divide this frequency by 2.

TTC clock jitter

More work is necessary to understand where the quite high jitter is coming from in the TTC clock distribution. Measures should be done with Serial Data Analyser or with scope equipped with clock detection and generation of eye diagram. Depending on the transition time of the signal, a scope with a higher bandwidth than 1 GHz might be necessary. These measures must be done all along the chain and the final jitter value compared to the maximum value allowed by the system. This should be done with activity on all the boards crossed by the measured channel and adjacent boards.

Some of the the jitter may come from the combination of the QPLL and the Mux PLL. If this contribution is too high then the clock chain should maybe done only with traditional buffers (i.e without PLL).

Production schedule

The production schedule is sound. Care should be taken to make sure that the SCT and Pixel versions are identical in order to optimise the number of spare modules to be built.

RECOMMENDATIONS

When the recommendations given above have been implemented and the jitter understood, the production of the 20 needed boards can start.