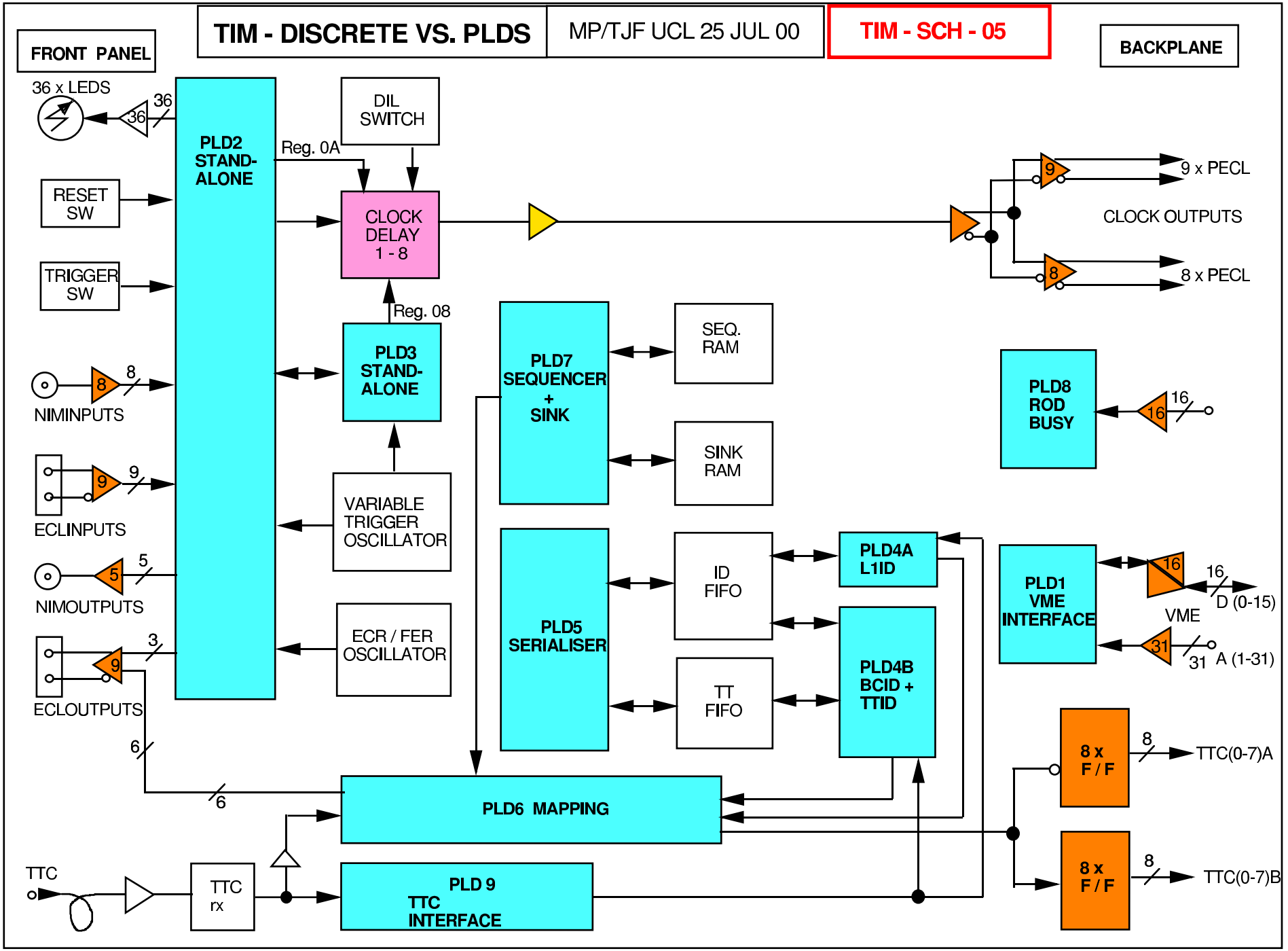
TIM - DISCRETE VS. PLDS
MP/TJF UCL 25 JUL 00
TIM - SCH - 05
FRONT PANEL
BACKPLANE
36 x LEDS
36
PLD2 STAND-ALONE
DIL SWITCH
Reg. 0A
RESET SW
TRIGGER SW
CLOCK DELAY 1 - 8
9
9 x PECL
CLOCK OUTPUTS
8
8 x PECL
Reg. 08
PLD3 STAND-ALONE
PLD7 SEQUENCER + SINK
SEQ. RAM
SINK RAM
PLD8 ROD BUSY
16
NIMINPUTS
8
ECLINPUTS
9
VARIABLE TRIGGER OSCILLATOR
NIMOUTPUTS
5
ECR / FER OSCILLATOR
PLD5 SERIALISER
ID FIFO
TT FIFO
PLD4A L1ID
PLD4B BCID + TTID
PLD1 VME INTERFACE
D (0-15)
VME
A (1-31)
31
ECLOUTPUTS
3
6
PLD6 MAPPING
8 x F / F
TTC(0-7)A
TTC(0-7)B
TTC
TTC rx
PLD 9 TTC INTERFACE