28 July 2000

TTC INTERFACE MODULE (TIM) : MODULE CONNECTIONS to the BACKPLANE

Update Log :

28 Jul. 2000, MP-UCL : Updated with additional changes to CLK40+/- slot numbering and to ROD-Busy slot numbering to take into account the move of TIM from slot 5 to slot 13
03 Jul. 2000, MP-UCL : Corrected & changed as per comments from ROD Workshop, UCL, 15-16 June 2000
09 Jun. 2000, MP-UCL : Changed as per final "SCT Off Detector Crate Backplane" document, dated 22 May 2000
07 Dec. 1999, MP-UCL : Removed unused VME signals
01 Dec. 1999, MP-UCL : Added Jaux & JBL minor changes
30 Nov. 1999, MP-UCL : Simplify & JBL minor corrections
29 Nov. 1999, MP-UCL : TIM backplane connections only

This document is a description of the actual TIM0 module connections to the ROD Crate Backplane.
It follows the Interface Specification Document, as shown in the "SCT Off Detector Crate Back Planes and Crate Card Utilization"

Version 1.0, 8 Oct. 1999
Version 2.n 22 May 2000
Version - 24 July 2000

P1 Connector on TIM module :

Pin	***Row Z***	***Row A***	***Row B***	***Row C***	***Row D***	***Pin***
1		D00		D08	**+5V**	**1**
2	**Gnd**	D01		D09	**Gnd**	**2**
3		D02		D10		**3**
4	**Gnd**	D03		D11		**4**
5		D04		D12		**5**
6	**Gnd**	D05		D13		**6**
7		D06		D14		**7**
8	**Gnd**	D07		D15		**8**
9		**Gnd**		**Gnd**	GAP*	**9**
10	**Gnd**				GA0*	**10**
11		**Gnd**		BERR*	GA1*	**11**
12	**Gnd**	DS1*			**+3.3V**	**12**
13		DS0*		LWORD*	GA2*	**13**
14	**Gnd**	WRITE*		AM5	**+3.3V**	**14**
15		**Gnd**		A23	GA3*	**15**
16	**Gnd**	DTACK*	AM0	A22	**+3.3V**	**16**
17		**Gnd**	AM1	A21	GA4*	**17**
18	**Gnd**		AM2	A20	**+3.3V**	**18**
19		**Gnd**	AM3	A19		**19**
20	**Gnd**	IACK*	**Gnd**	A18	**+3.3V**	**20**
21		IACKIN*		A17		**21**
22	**Gnd**	IACKOUT*		A16	**+3.3V**	**22**
23		AM4	**Gnd**	A15		**23**
24	**Gnd**	A07	IRQ(7)*	A14	**+3.3V**	**24**
25		A06	IRQ(6)*	A13		**25**
26	**Gnd**	A05	IRQ(5)*	A12	**+3.3V**	**26**
27		A04	IRQ(4)*	A11		**27**
28	**Gnd**	A03	IRQ(3)*	A10	**+3.3V**	**28**
29		A02	IRQ(2)*	A09		**29**
30	**Gnd**	A01	IRQ(1)*	A08	**+3.3V**	**30**
31		**−12V**	**+5V**	**+12V**	**Gnd**	**31**
32	**Gnd**	**+5V**	**+5V**	**+5V**	**+5V**	**32**

GND: 26 pins
+5V 6 pins
+3.3V 10 pins
−12V 1 pin
+12V 1 pin

P2 Connector on TIM module :

Pin	*Row Z*	*Row A*	*Row B*	*Row C*	*Row D*	*Pin*
1			**+5V**			**1**
2	**Gnd**		**Gnd**			**2**
3						**3**
4	**Gnd**		A24	**−5.2V (#)**		**4**
5			A25			**5**
6	**Gnd**		A26			**6**
7		**−5.2V (#)**	A27			**7**
8	**Gnd**		A28			**8**
9			A29			**9**
10	**Gnd**		A30			**10**
11			A31			**11**
12	**Gnd**		**Gnd**			**12**
13		**−5.2V (#)**	**+5V**			**13**
14	**Gnd**					**14**
15						**15**
16	**Gnd**					**16**
17						**17**
18	**Gnd**					**18**
19		**−5.2V (#)**		**−5.2V (#)**		**19**
20	**Gnd**					**20**
21						**21**
22	**Gnd**		**Gnd**			**22**
23						**23**
24	**Gnd**					**24**
25						**25**
26	**Gnd**					**26**
27						**27**
28	**Gnd**					**28**
29						**29**
30	**Gnd**					**30**
31			**Gnd**		**Gnd**	**31**
32	**Gnd**		**+5V**		**+5V**	**32**

GND: 21 pins
+5V: 4 pins
−5.2V 5 pins

Note : **(#)** **−5.2V** supply pins on **TIM P2** are for prototype testing purposes in VME/VXI-type crates at UCL or CERN only, and will not be provided on the final version. All the above **−5.2V** pins have links for isolation

P3 Connector on TIM module :

Pin	***Row Z***	***Row A***	***Row B***	***Row C***	***Row D***	***Pin***
1		**Gnd**		**+3.3v**	ROD-Busy5	**1**
2			**Gnd**	ROD-Busy6	**+3.3v**	**2**
3		CLK-40+ slot5	CLK-40- slot5	**+3.3v**	ROD-Busy7	**3**
4	**Gnd**	CLK-40+ slot14	CLK-40- slot14	ROD-Busy8	**+3.3v**	**4**
5		**Gnd**		**Gnd**		**5**
6		CLK-40+ slot6	CLK-40- slot6	ROD-Busy9	**+3.3v**	**6**
7		CLK-40+ slot15	CLK-40- slot15	**+3.3v**	ROD-Busy10	**7**
8		CLK-40+ slot7	CLK-40- slot7	**+3.3v**	**+3.3v**	**8**
9	**Gnd**		**Gnd**	ROD-Busy11	**+3.3v**	**9**
10		CLK-40+ slot16	CLK-40- slot16	**Gnd**	**+3.3v**	**10**
11		**Gnd**		ROD-Busy12	Laser-Interlock	**11**
12		CLK-40+ slot8	CLK-40- slot8	ROD-Busy14	**Gnd**	**12**
13		CLK-40+ slot17	CLK-40- slot17	ROD-Busy15	ROD-Sense **(1)**	**13**
14	**Gnd**		**Gnd**	ROD-Busy16	ROD-Busy17	**14**
15		CLK-40+ slot9	CLK-40- slot9	**Gnd**	ROD-Busy18	**15**
16		CLK-40+ slot18	CLK-40- slot18	ROD-Busy19	ROD-Busy20	**16**
17		**Gnd**		ROD-Busy21	**+5V**	**17**
18		CLK-40+ slot10	CLK-40- slot10		CLK-40+ **(5)**	**18**
19	**+5V**	CLK-40+ slot19	CLK-40- slot19		CLK-40- **(5)**	**19**
20		**Gnd**		**Gnd**	**+5V**	**20**
21		CLK-40+ slot11	CLK-40- slot11		TIM-Busy Out	**21**
22		CLK-40+ slot20	CLK-40- slot20		**+5V**	**22**
23			**Gnd**	TTC-7B	TTC-7A	**23**
24	**+5V**	CLK-40+ slot12	CLK-40- slot12	TTC-6B	TTC-6A	**24**
25		CLK-40+ slot21	CLK-40- slot21	**Gnd**	TTC-5A	**25**
26		**Gnd**		TTC-5B	TTC-4A	**26**
27		CLK-40+ slot13	CLK-40- slot13	TTC-4B	**+5V**	**27**
28			**Gnd**	TTC-3B	TTC-3A	**28**
29	**+5V**			TTC-2B	TTC-2A	**29**
30				**Gnd**	TTC-1A	**30**
31		**Gnd**		TTC-1B	TTC-0A	**31**
32				TTC-0B	**+5V**	**32**

GND : 22 pins
+5V : 8 pins
+3.3V : 10 pins **(ARE NOT USED BY TIM, BUT ARE DECOUPLED ON TIM USING 100nF CAPACITORS TO GND)**

Note: **The TIM module must only be used in its dedicated slot 13**

Note: The ground pins have been selected so that no damage will occur if the card is put in any slot

Note: The signal pin selection may cause damage to the TIM or BOC.

Note: **(1)** **ROD-Sense:** Grounded on all RODs and on backplane in TIM slot only, pulled high on TIM and BOC by 1k resistor

(4) **CLK-40 +/- slotNN:** from TIM to BOC only, all clock lines have the same electronic length and are 100 ohm impedance

(5) **CLK-40 +/- :** return to TIM. This is the return signal from TIM slot Row A and B above. It is the same electrical length as all the other clock lines from TIM to BOC, and the same 100 ohm impedance

- All **CLK-40 +/-** are differential PECL signal pairs.

- They all have 270R resistor to GND on TIM and have 100R resistor between differential pairs on BOC

Note: – **TTC-(0-7)A/B** are **LOW GOING** TTL signals bussed to all RODs. They are not used on BOCs.

These lines are terminated on the backplane in slot 21 and slot 5 respectively

Impedance about 50 ohms with all ROD cards plugged in

Note: – **ROD-BUSY(5-12)&(14-21)** are **LOW GOING** LV signals, point-to-point from all RODs. They are not used on BOCs.

These lines are pulled high on TIM by 10k resistor to +3V3

Paux ("Jaux") Connector on TIM :

Note : **Paux not soldered in – pads only provided**

Pin	***Row A***	***Row B***	***Row C***	***Pin***
1		**Gnd**		**1**
2		**Gnd**		**2**
3		**Gnd**	**Gnd**	**3**
4		**Gnd**		**4**
5		**Gnd**		**5**
6		**Gnd**		**6**
7				**7**
8				**8**
9	**–5.2V (#)**	**–5.2V (#)**	**–5.2V (#)**	**9**
10	**–5.2V (#)**	**–5.2V (#)**	**–5.2V (#)**	**10**

GND: 6 pins
–5.2V 6 pins

Note : **(#)** **–5.2V** supply pins on **TIM Paux** are for prototype testing purposes in VME/VXI-type crates at UCL or CERN only, and will not be provided on the final version. All the above **–5.2V** pins have links for isolation