

## Design and development of electronics for the EuXFEL clock and control system

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RECEIVED: *November 15, 2011*REVISED: *December 15, 2011*ACCEPTED: *December 16, 2011*PUBLISHED: *January 16, 2012*

TOPICAL WORKSHOP ON ELECTRONICS FOR PARTICLE PHYSICS 2011,  
26–30 SEPTEMBER 2011,  
VIENNA, AUSTRIA

## Design and development of electronics for the EuXFEL clock and control system

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**ABSTRACT:** The development of the Clock and Control (CC) hardware and firmware for the EuXFEL DAQ system is presented. The system exploits the data handling advances provided by the new telecommunication architecture standard for physics. The CC is responsible for synchronising the DAQ system to overall system timing. The hardware consists of a DESY designed MTCA.4 board and a UCL designed Rear Transition Module (RTM). Each RTM controls up to 16 Front End Modules (FEMs) for a 1 Megapixel 2D detector. The CC system is designed to provide extendibility and scalability to support future upgrades to the DAQ or larger detectors.

**KEYWORDS:** Modular electronics; Instrumentation for FEL; Digital electronic circuits; Data acquisition circuits

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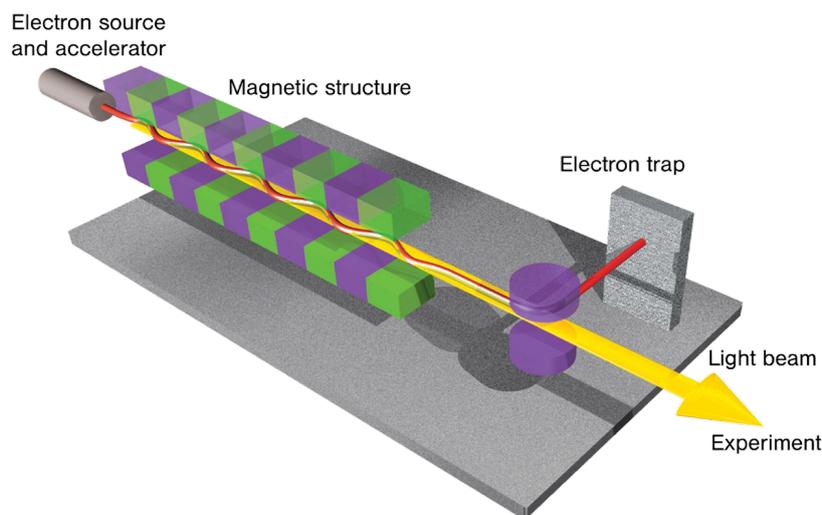
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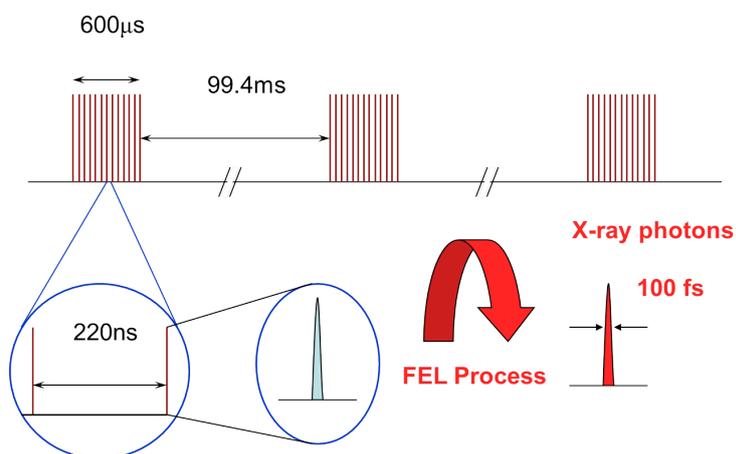
## 1 Introduction

The European Free Electron Laser (EuXFEL) facility being constructed at DESY, Hamburg will benefit many areas of science, from creating extreme states of matter in plasma physics to probing currently inaccessible molecules in structural biology and investigating the structure of large biomolecules like proteins [1]. The EuXFEL project is a large-scale facility using high intensity, high energy beams usually only associated with particle physics experiments. The accelerator will be 3.4 km long using novel superconducting RF technology to accelerate electrons to high energy. The electrons will then pass through an undulator, causing them to oscillate and emit laser-like photons (figure 1). When it turns on, the EuXFEL will provide a beam 100 million times more brilliant than current synchrotron sources [2]. To measure the effect of the impact of the particle beam on the various samples, large megapixel detectors ( $\geq 1$  Mpixel) will be used to reconstruct an accurate diffractive image.

The superconducting acceleration technique involves 1.3 GHz superconducting cavities at a temperature of 2 K generating acceleration fields of 20–25 MV/m for use at the EuXFEL. A single cavity structure contains nine accelerating cells and eight structures with their beam controlling elements mounted into one cryostat segment. The entire LINAC consists of 101 segments where most of them will be assembled into one long superconducting tube. Despite the use of superconductivity techniques some heat is generated and the accelerating field can be switched on for only 0.6 ms every 100 ms. This prohibits continuous wave (CW) operation, instead trains of consecutive electron bunches are accelerated. In normal operation 27 000 bunches, compared to 60 to 120 at the other XFELs [2], are generated per second, grouped into 10 trains of 2 700 bunches with an inter bunch time separation of 220 ns which corresponds to a frequency of 4.5 MHz. This requires that all control and data taking electronics have to cope with 4.5 MHz bunch delivery rates interspersed by 99.4 ms inactivity periods. The lasing generated from 20 mm electron bunches provides short X-ray flashes of  $< 100$  fs duration [3]. Figure 2 illustrates the bunch trains and the timings.

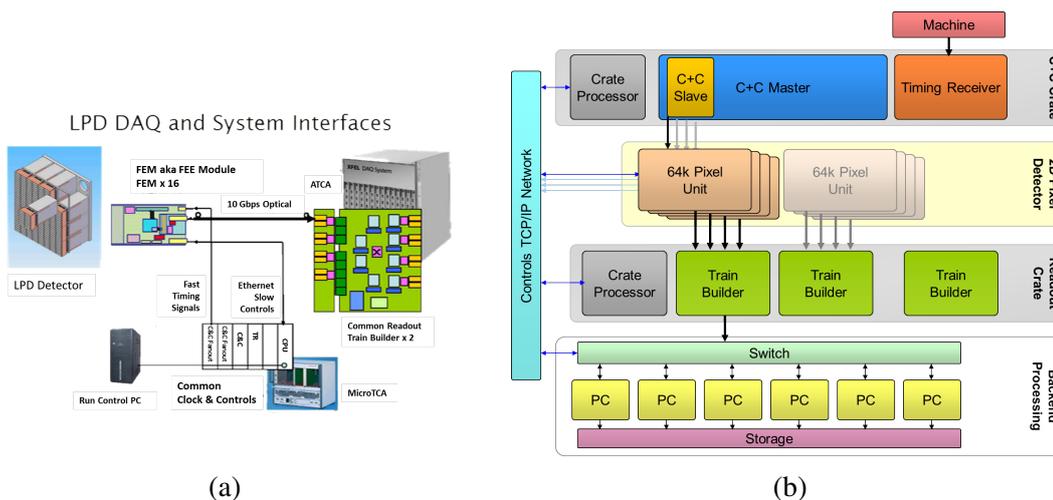


**Figure 1.** Representation of electron acceleration for EuXFEL.



**Figure 2.** EuXFEL bunch and photon timings.

Each generated X-ray flash is intense enough to produce a full diffractive picture of scattering targets. Three different detector designs are in development, namely, AGIPD [3], DSSC [4] and LPD [5]. Although each focuses on different measurement classes and use different technologies, the basic concepts regarding mechanical and functional block design are similar and are sketched in figure 3a for LPD. The detector head has a silicon sensor facing the scattered X-rays. ASICs that contain the electronics necessary for preamplification, shaping and data readout control are bump-bonded to their back side and board level electronics are located nearby [3]. This forms a detector head at the beam line which forms the front end module (FEM), in which a vacuum barrier is integrated to reduce the scattering of the X-rays but allows air cooled electronics. Each FEM supports 64 K pixels of the final image, therefore, as an example, for a 1 Mpixel camera 16 FEMs are to be used.



**Figure 3.** (a) Representation of the DAQ system with the LPD detector, (b) the block diagram of the DAQ system.

Rack mounted electronics is located a few metres away which comprises the units providing DAQ and infrastructure functionality. The clock and control (CC) system is a part of the rack mounted electronics for the DAQ system which constitutes the interface between the overall EuXFEL timing and the FEM electronics.

## 2 The clock and control system for DAQ

The DAQ system for the megapixel cameras comprises the CC system, a train builder and the power and the cooling infrastructure to operate the FEM units. The CC system provides the synchronising clock and bunch and train related information to the FEM electronics. It also receives status feedback from FEMs and distributes the veto signals to the FEMs to reject some of the detector data. The FEM electronics provide the read-out data for the Train Builder (TB) board and control the ASIC. Figure 3b presents the general structure of the DAQ system.

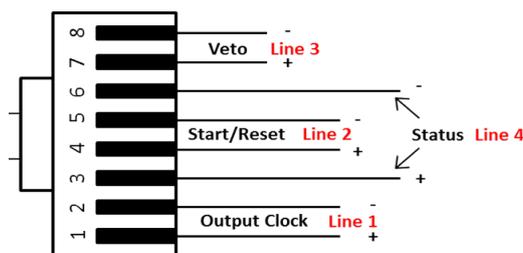
The interface to the overall EuXFEL timing system is accomplished through the connections to the timing receiver (TR) board [6] which provides clocks and timing related information to all systems within the facility in order to synchronise the operation. With the connections to the FEM electronics, the CC system synchronises the DAQ timing to the general EuXFEL facility timing.

### 2.1 CC system interfaces

In order to synchronise the FEM operations with the overall facility timing the connections to the FEM electronics are realised on AC-coupled LVDS links on CAT6 RJ45 cables. Being a widely available, tested and proven technology, LVDS on RJ45 CAT6 cables drives down the cost and design effort.

One RJ45 connector provides 4 LVDS pairs sufficient for the connections to a single FEM. The names and the description of the signals to FEMs are:

1. Output clock (FAST clock): a  $\sim 99$  MHz clock derived from the 4.5 MHz bunch clock.



**Figure 4.** Distribution of signals for the FEM interface.

2. Output data (FAST data): provides the trigger start signal and train ID data to the FEMs.
3. Veto: is the bunch reject data encoded on a either 99 or 4.5 MHz clock.
4. Status: a status feedback from the FEMs.

Figure 4 shows how these signals are assigned to a RJ45 connector.

The interface to the overall facility timing is realised through the connections to the TR system. These connections are:

1. Start/Trigger: the signal which denotes the start of the bunch train.
2. Telegram Data: the information sent by the TR system comprising the bunch train number and the index of the bunch train pattern.
3. Telegram Clock: the 130 MHz clock for sending the telegram data.
4. Bunch clock: the 4.5 MHz bunch clock that is common to all the units in the facility.
5. Extra connections for various function such as resetting the CC system and status from the CC system.

In addition to the interfaces to the FEMs and the TR system, there needs to be another interface to the overall software control system. Through this interface tasks such as initial configuration, emergency shutdown, and overall status checking are performed.

## 2.2 General hardware

The TCA standards used in telecommunications are chosen to be used at EuXFEL to provide a multi-layer highly scalable managed platform architecture designed to achieve the highest possible system availability. Additionally, the TCA platform is the first all-serial communication platform available to the physics community to support both massively complex accelerator controls and massively large, high bandwidth and throughput experimental data acquisition systems [7].

The recent extension to the  $\mu$ TCA standards, MTCA.4, namely  $\mu$ TCA for physics [8], defines mechanics for supporting large I/O bound physics applications through the use of Rear Transition Modules (RTMs). It also defines backplane connections to support high-speed serial differential links as well as dedicated channels and differential buses to distribute high quality clock and trigger

signals. The use of RTMs also allows flexible combinations to design modular and scalable systems in order to reduce the overall design effort and cost.

For the CC system we have gone for a MTCA.4 solution. The system consists of a MTCA.4 AMC (Advanced Mezzanine Card) board and a Rear Transition Module (RTM). The MTCA.4 AMC board (DAMC2) [9] is designed by DESY as a multi-purpose FPGA hardware platform for various projects in DESY and provides the processing capability needed for the CC functionality. We have developed our own custom RTM board according to the MTCA.4 standard which connects to the DAMC2 through two thirty-pair Advanced Differential Fabric (ADF) connectors. This configuration enables us to deliver the required functionality with a modular and scalable solution that also led to a significant reduction in design effort duplication.

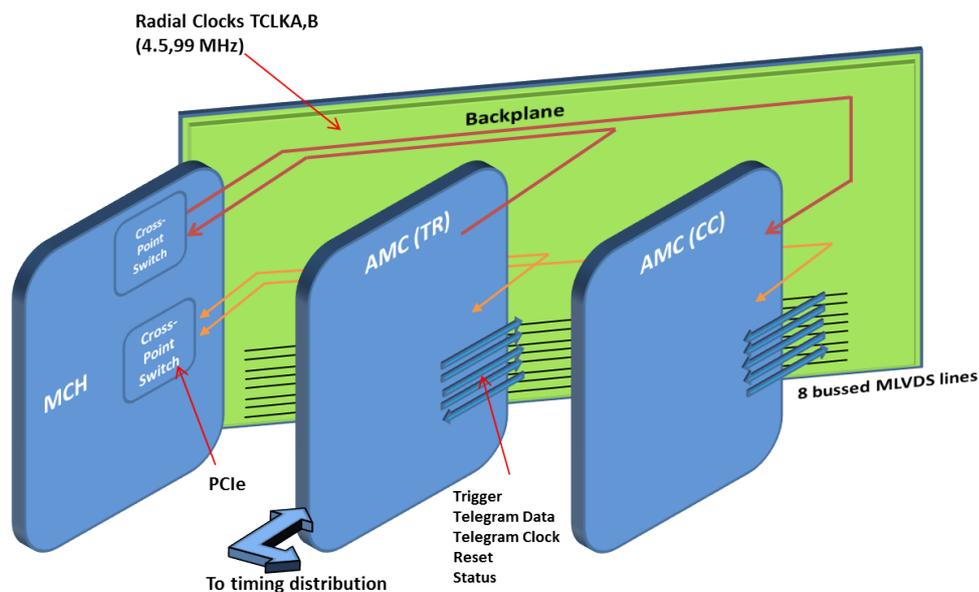
The TR board [10] is also an AMC board and will be housed in the same MTCA.4 crate. Figure 5 shows the connections on the MTCA.4 backplane. Eight bussed LVDS links provide the necessary connections mentioned in the previous section between the TR board and the CC system. The 4.5 MHz bunch clock from the TR board is transmitted on the high-quality TCLK link on the backplane. The interface to the overall software system is realised on a 4-lane PCIe link which connects the all AMC boards to the CPU board which is also housed in the crate.

Figure 6 provides the actual photo of the RTM. The first thing to observe is the stacked RJ45 connector which provides channels to support up to 16 FEM modules. This enables the capability of using one AMC/ $\mu$ RTM combo for a 1 MPixel 2D detector. Just behind the stacked RJ45 connector are the two 1:16 LVDS fan-out buffers for the FAST clock and the data.

The two ADF connectors provide in total 54 differential links to the Xilinx Virtex5 FPGA on the DAMC2 board in addition to 12V power, MTCA.4 specification related I2C link, 3.3 V management power and the  $\mu$ RTM present signal. In our implementation we use the FPGA links in both differential and single ended configuration. The differential links are used for the clocks into and from the  $\mu$ RTM, veto signals and FAST data out to the FEMs, status signals from the FEMs and links to and from a spare RJ45 connector which is also placed on the front panel for possible future capability extensions. The single ended links comprise the signals to control for the PLLs, to control the LED controllers for the stacked RJ45 connector, status signals from the PLLs, and a number of spare signals for test and debug purposes.

The block number one in figure 6 is the clock generation block whose main function is taking a differential clock (4.5 MHz or 9 MHz) from the DAMC2 board and multiplying this in order to generate the clock for the FEM units (99 MHz). For standalone operation, or in the absence of a clock from the main system, there is a clock crystal chip on board as well. In order to provide the highest flexibility, a glitch-free, zero-delay PLL based clock multiplexer is used to select between the system clock and the standalone clock. This selected clock is input to another PLL chip whose multiplication factor is controlled by the FPGA. This PLL chip generates the FAST clock signal to the FEMs which is input to a 1:16 LVDS fan-out buffer. The outputs of this buffer are connected to the respective pins on each of the 16 RJ45 channels. The output of the second PLL is also sent back to the FPGA on a differential link.

The block number two is the circuitry for the MTCA.4 management requirements. This block includes an I2C expander chip for controlling the LEDs on the front panel, checking the status of the hot-swap switch and enabling the power supplies on the  $\mu$ RTM by the MMC on the DAMC2 board. Additionally there is an EEPROM and a temperature sensor chip all on the same I2C bus as



**Figure 5.** Connections between the MCH, TR board and the CC board on the MTCA.4 backplane.

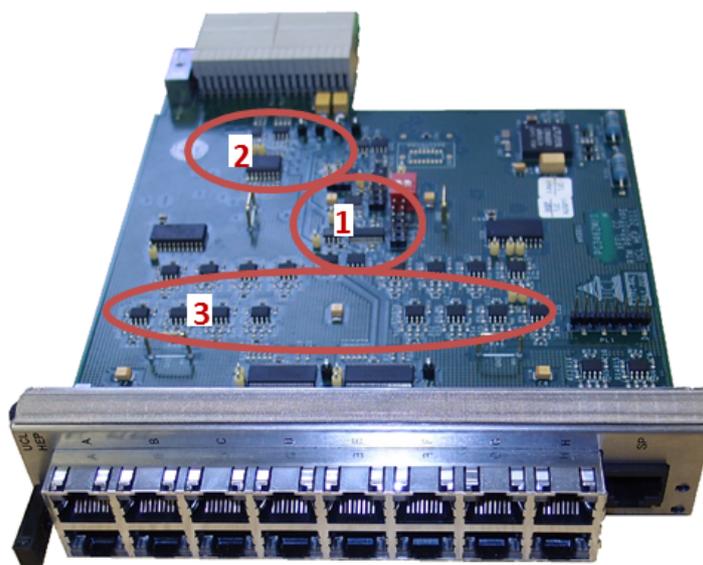
the expander. The EEPROM holds the  $\mu$ RTM information and MTCA.4 specified information for electronic keying.

The block number three comprises the LVDS receivers which gather the status data coming from the FEMs. A special circuitry involving two LVDS buffer chips for each FEM channel is used. [11] The reason for this circuitry is to provide necessary level shifting on the AC-coupled LVDS data link in the absence of a decoding algorithm providing a DC-balanced link. This circuitry has been tested on a development board before being added to the CC  $\mu$ RTM design. The results of the test are included in the results section.

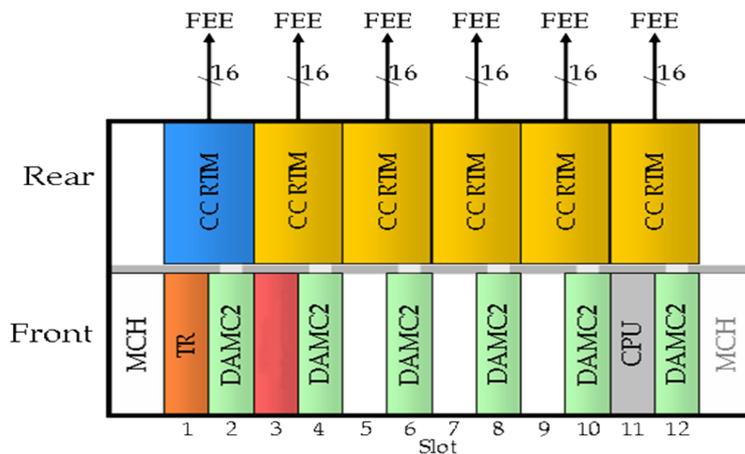
The CC system is designed to provide scalability to support higher Mpixel detectors by using extra AMC and  $\mu$ RTM board pairs in the same crate with one pair designated as master and sharing the clock and the data through the MTCA.4 backplane. Each CC board pair takes up two slots (double full-size board) on the crate which comes in either 6 or 12 slot configuration. Therefore up to 6 Mpixel cameras can be supported by a single 12 slot crate as shown in figure 7.

### 2.3 FPGA firmware

The firmware block diagram for the CC board is shown in figure 8. The FAST TX module generates the FAST data to the FEMs. The telegram RX module receives and decodes the information coming from TR board on a clock and data pair through the backplane. The control and clocking module provides the control signals for all the modules in the firmware and the components on the  $\mu$ RTM. Another function of this block is to provide synchronisation of the FAST data to the FAST clock that is generated on the  $\mu$ RTM as well as instantiating the on-chip PLL units to produce the necessary clocks for the firmware modules. The PCIe block provides the connection to the crate CPU to receive configuration data from the control software [12]. There is a separate module for generating the veto data to the FEMs. The RocketIO module makes use of the small form-factor pluggable



**Figure 6.** A photo of the CC RTM.

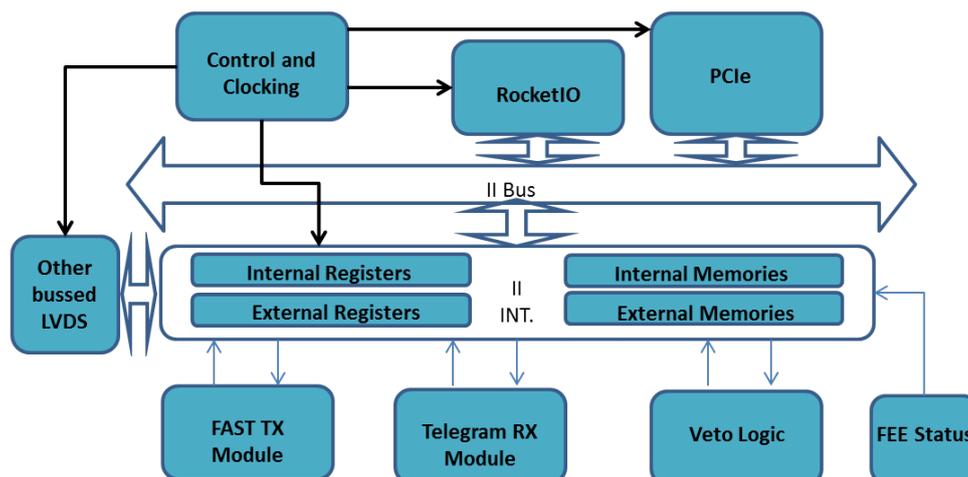


**Figure 7.** Placement of the boards in a 12-slot MTCA.4 crate.

(SFP) transceivers on the DAMC2 board and provides an optional veto source input to the firmware. All the modules in the firmware are integrated through a bus and a register block called Internal Interface (II) [13] which is developed by DESY.

### 3 Tests and results

As mentioned in the previous section the level-shifting circuitry for the AC-coupled LVDS links was tested before being used in the CC  $\mu$ RTM. The tests involved sending pseudo-random bit patterns generated by a linear feedback shift register (LFSR) realised on the FPGA of a development board (Xilinx XUPV5). A special daughterboard that provides transmit and receive LVDS links through RJ45 connectors was designed to fit the extension connectors on these boards [14]. The



**Figure 8.** Block diagram of the FPGA firmware.

receive circuitry on the daughterboard comprised the LVDS level-shifting circuitry. The bit patterns consisted of 22-bit words synchronised to the 4.5 MHz clock and sent along with the 99 MHz clock which would be the case in the actual operation of the FAST data link. Another development board received these patterns and compared them with the internally generated patterns using the same LFSR structure and the seed. The 99 MHz clock was sent on another LVDS line pair through a 5 metre CAT6 Ethernet cable. A counter named “error\_count” is incremented in the FPGA in the case the pattern received doesn’t match the internally generated pattern. The FPGA source code also contained other test cases where long series of zeros or ones were introduced between the pseudo-random bit patterns. All of the tests were run for long periods of time (>24 hours) and no errors were detected on the link.

A series of other tests are planned to be executed. The first test involved checking the compliance to the MTCA.4 standard such that the power to the  $\mu$ RTM would be enabled by the DAMC2 and the necessary 3.3 V voltage rail on the  $\mu$ RTM would be generated by the DC-DC converter onboard. This would ensure the I2C link between the MMC on the DAMC2 board and the CC  $\mu$ RTM operating correctly and the data on the  $\mu$ RTM EEPROM was correctly written to and read. The test was successfully passed by the  $\mu$ RTM and the relevant LEDs on the front panel and on the board were lit up.

Additional tests to prove the functionality of the CC RTM are still being devised. These include the successful reception of the telegram clock and data from the TR board in the MTCA.4 crate and the reception and the quality of the 4.5 MHz bunch clock in terms of jitter from the crate MCH.

## 4 Conclusion

The CC hardware/firmware system is designed to provide the flexibility, extensibility and scalability to support possible future upgrades to the EuXFEL 2D megapixel camera DAQ. It also reduces the cost and effort for the development of such system by using a general-purpose MTCA.4 FPGA board as its processing platform and an RTM to provide the custom functionality.

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