**DAMC2 meeting.**

**26.01.2012**

Results of discussion:

1. Organized interface MLVDS bus to FPGA by next type:
   * All signals from RX ports (RX17 – RX20) of Back Plane should be connected to positive side of differential “Clock Capable” pins of FPGA
   * All signals from RX ports can be used as single ended **clocks**
   * All signals from TX ports (TX17 – TX20) of Back Plane should be connected to negative side of differential “Clock Capable” pins of FPGA
   * All signals from TX ports can be used as general purpose single ended **I/O**
2. New clock distribution scheme will be implemented in consequence with Patrick and Erdem proposals.
3. The FMC interface will be implemented
4. The new ATxmega128A1 as new MMC will be implemented
5. The configuration mode of FPGA will be changed from serial to parallel
6. The JTAG of uRTM board will be included in FPGA daisy chain
7. The modification of Hot Swap controller will be done
8. GTP interface will be not used in uRTM interface
9. Heat-Sink for FPGA will be implemented – blue clip with radiator 35x35x12 mm
10. The connection **signal GND to Front Panel is optional**
11. The reducing of DAMC2 production price is open question and some additional investigations are needed