

NOTES

1. RESISTANCE VALUE IN Ohms
2. REFERENCE DESIGNATOR USED:

A. INTEGRATED CIRCUITS: U1 - U36

B. CERAMIC CAPS: C1 - C3, C6 - C9, C11, C12, C15,C16, C21, C22, C24, C27 - C44, C46 - C61, C63 - C68, C70 - C92, C94 - C96, C98 - C110, C112 - C114, C119 - C122, C125 - C132, C135 - C150, C153 - C164, C167, C168, C170 - C181, C184 - C189, C191 - C195, C197 - C230, C232 - C262, C264 - C270, C272 - C277.

C. CAPACITORS ARRAY: C13, C14, C23, C62, C69, C 93, C117, C118, C165, C166, C169, C182, C183, C190, C196, C263, C271

D. SMD ALUMINUM ELECTROLITIC CAPACITOR: C20.

E. LOW ESL&ESR TANTALUM CAPS: C4, C5, C10, C17 - C19, C25, C26, C45, C97, C111, C115, C116, C123, C124, C133, C134, C151, C152, C231.

F. SMD RESISTORS: R1 - R49, R51 - R54, R57, R58, R60 - R67, R69, R70, R72 - R89, R91 - R101, R103, R104, R106 - R110, R112 - R115, R117 - R121, R123 - R164, R169 - R180.

G. ARRAY CHIP RESISTORS: R50, R55, R56, R59, R68, R71, R90, R102, R105, R111, R116, R122, R165 - R168.

H. CONNECTORS/HEADERS: J1 - J31, JP1.

I. OSCILLATORS, RESONATOR: Q1 - Q4.

J. EMI FILTERS (BEADS&INDUCTORS): L1 - L52.

K. SWITCH (PUSHBUTTON, MICROSWITCH): SW1, SW2.

L. SMD LEDs, FRONT PANEL LEDS: V1 - V11, V14, V15, V17, V18, V19.

M. SMD DIODE AND TRANSISTOR: V12, V13, V16

N. TEST POINTS: TP1, TP2

O. SFP CAGE AND ESD STRIP: X1, X2
3. BOARD PROPERTIES:

A. FR4 BOARD MATERIAL

B. MINIMUM TRACE WIDTH/SPACING: 0.08/0.1 MM

C. MINIMUM VIA SIZE: 0.2 MM

D. STACKUP (14 LAYERS):

1. TOP - SIGNAL ROUTING, AREA FILLS

2. POWER PLANE: GND

3. SIGNAL ROUTING, AREA FILLS

4. SPLIT POWER PLANE: +1V, +2V5, +3V3

5. SIGNAL ROUTING

6. POWER PLANE: GND

7. SIGNAL ROUTING

8. POWER PLANE: GND

9. SIGNAL ROUTING

10. SPLIT POWER PLANE: +2V5, +3V3, +12V, AVCCPLL_1V2, AVTTX_1V2, VCC0V9_VREF

11. SIGNAL ROUTING

12. SIGNAL ROUTING

13. SPLIT POWER PLANE: +3V3, +12V, AVCCPLL_1V2, AVCC_1V0, AVTXX_1V2, GND_SCLK, VCC, V_OSC1, 1V8

14. SIGNAL ROUTING, AREA FILLS
- | REV. | DESCRIPTION | OWNER |
|------|-------------|---------|
| 0 | PROTOTYPE | DESY/FE |
| | | |
- SCHEMATIC CONTENTS
- SCHEMATIC1:

1, 2, 3, 4, 5, 6, 7, 8, 9 - CONSTRUCTION PROPOSALS

10. BLOCK SCHEMATIC OF DAMC2

11. DDR2 POWER

12. DAMC2 WITH TWO HOME MADE MEZZANINE BOARDS

13. LAST DAMC2 BLOCK DIAGRAM

SCHEMATIC2:

1. NOTES AND CONTENTS

2. EDGE PLASTIC CONNECTOR, AUXILIARY CONNECTOR AND ESD

3. FMC CONNECTOR (LPC)

4. ispFLASH

5. JTAG CHAIN

6. uRTM Hot Swap CONTROLLER

7. Interface to FMC (LPC) connector

8. PCIExpress Clock AND IODELAY CLOCK

9. MMC

10. SPARE VIRTEX-5 BANKS

11. DDR2 address and control signals

12. DDR2 data and control signals

13. DDR2 Bytes 0&1 - ODT(64 MByte)

14. DDR2 Bytes 2&3 - ODT (+64MByte)

15. System monitor, configuration logics, auxiliary and core powers

16. 4 LANES PCIExpress to back plane

17. 4 LANES to EDGE Connector - Ports 12-15

18. 3 Lanes to SFP connectors and one to SFP or to FMC

19. Powers for GTP and GTP_SWITCH

20. MLVDS bus to Edge Connector

21. LOW JITTER CLOCK Crosspoint Switch

22. GLOBAL CLOCKS

23. Termination Regulator for DDR2 MEMORY

24. Four SFP connectors

25. SFP CONTROLLER

26. Two connectors to RTM, 3 Amp/12V

27. 2V5 Interface to RTM

28. Power for GTP, DDR2 and ispFlash

29. Main Power for DAMC+FMC+uRTM
- | | | | | | |
|---------------------|-----------|--|--|----------------|---------|
| Developer: | Vetrov P. | ProjectFLASH Double DAMC Schematicschematic2 | | | |
| Drawn by: | Vetrov P. | Sheet: | | | |
| Layouter: | Vetrov P. | DESY-FEA Notkestrasse 85 D-22607 Hamburg | | | |
| Changed of sch: | Vetrov P. | | | | |
| Date Changed: | 20.8.2009 | PCB No: 8423 | | Rev: 00 | Size:A3 |
| Date of prod. data: | | PCB name :DAMC2 | | Sheet: 1 of 29 | |

EDGE Plastic Connector

AUX_Power_Connector

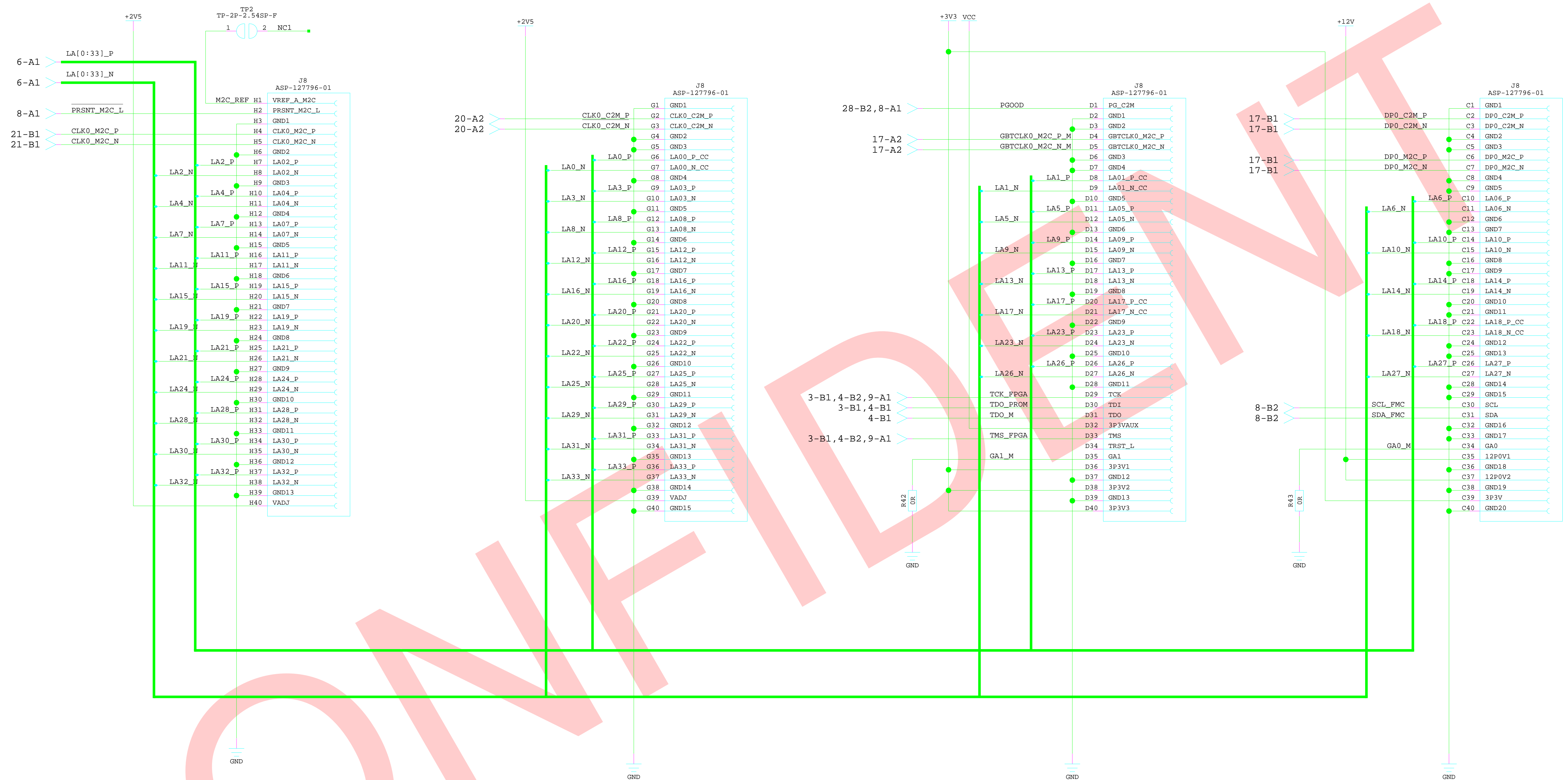
ESD strip

Max Hight of components on side 2 is 3mm!!!

Max thickness of PCB is 1.76 mm (1.6 mm +10%)!!!

Developer:	Vetrov P.	ProjectFLASH Double DAMC			
Drawn by:	Vetrov P.	Schematic2			
Layouter:	Vetrov P.	Sheet:			
Changed of sch:	Vetrov P.	DESY-FEA Notkestrasse 85 D-22607 Hamburg			
Date Changed:	20.8.2009	PCB No: 8423		Rev: 00	Size:A3
Date of prod. data:		PCB name:DAMC2		Sheet: 2 of 29	

FMC connector (LPC)



VREF_A_M2C - ref. voltage associated with the signaling standard used by the bank A data pins, LAXx.

If the signaling standard on Bank A does not require a reference voltage then this pin can be left unconnected.

3P3VAUX - VCC auxiliary power supply, which is used only for IPMI.

VADJ will be +2V5 - SP601 and ML605!

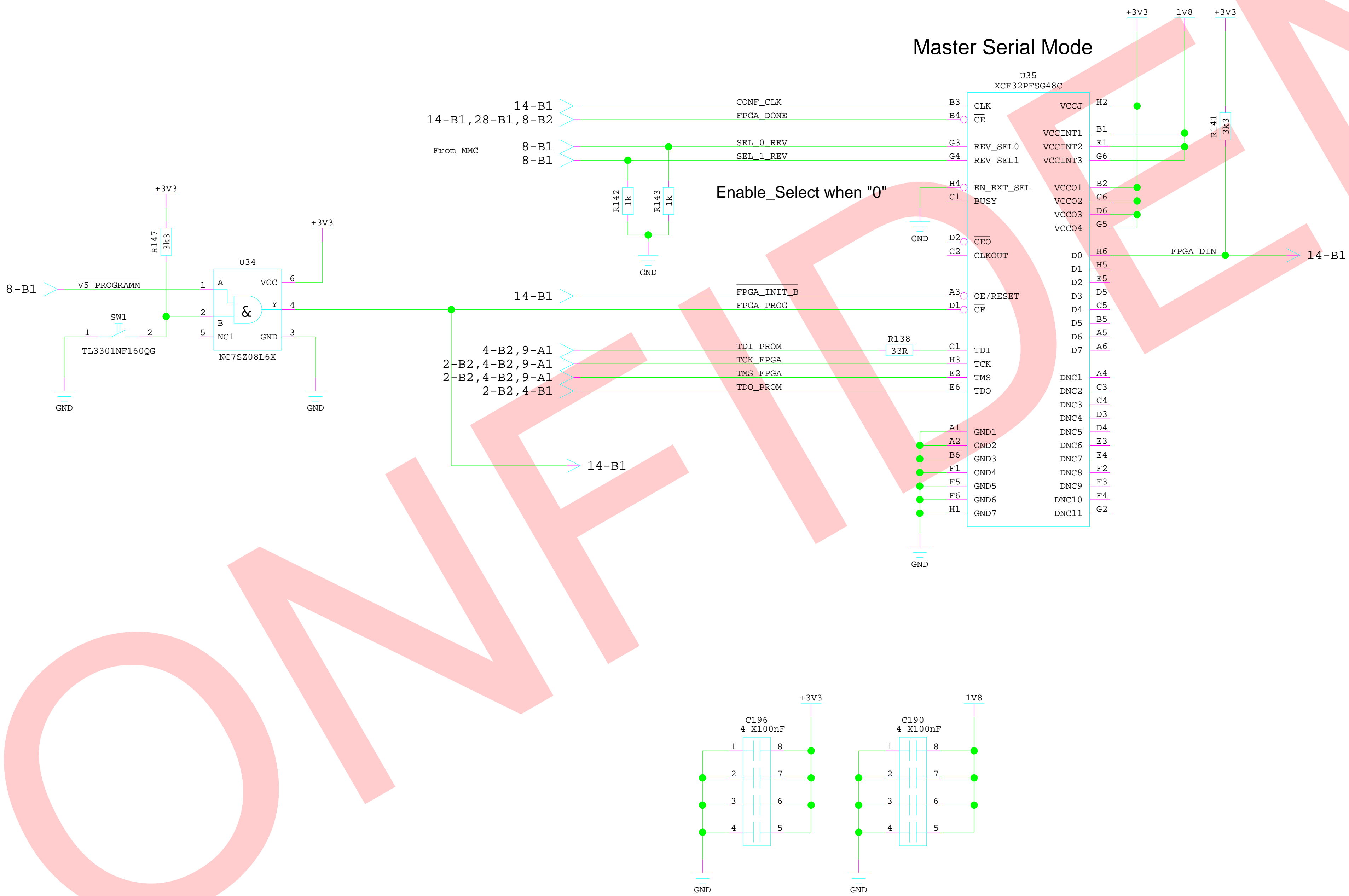
There are three main power supply voltages, VADJ, 3P3V and 12P0V

PG_C2M – Power Good Carrier Card. This signal asserts high by the carrier card when power supplies, VADJ, 12P0V, 3P3V, are within tolerance.

Developer:	Vetrov P.	Project: FLASH Double DAMC		
Drawn by:	Vetrov P.	Schematic: schematic2		
Layouter:	Vetrov P.	Sheet:		
Changed of sch:	Vetrov P.	DESY-FEA	Notkestrasse 85 D-22607 Hamburg	
Date Changed:	20.8.2009	PCB No: 8423	Rev: 00	Size: A3
Date of prod. data:		PCB name: DAMC2	Sheet: 3 of 29	

ispFlash

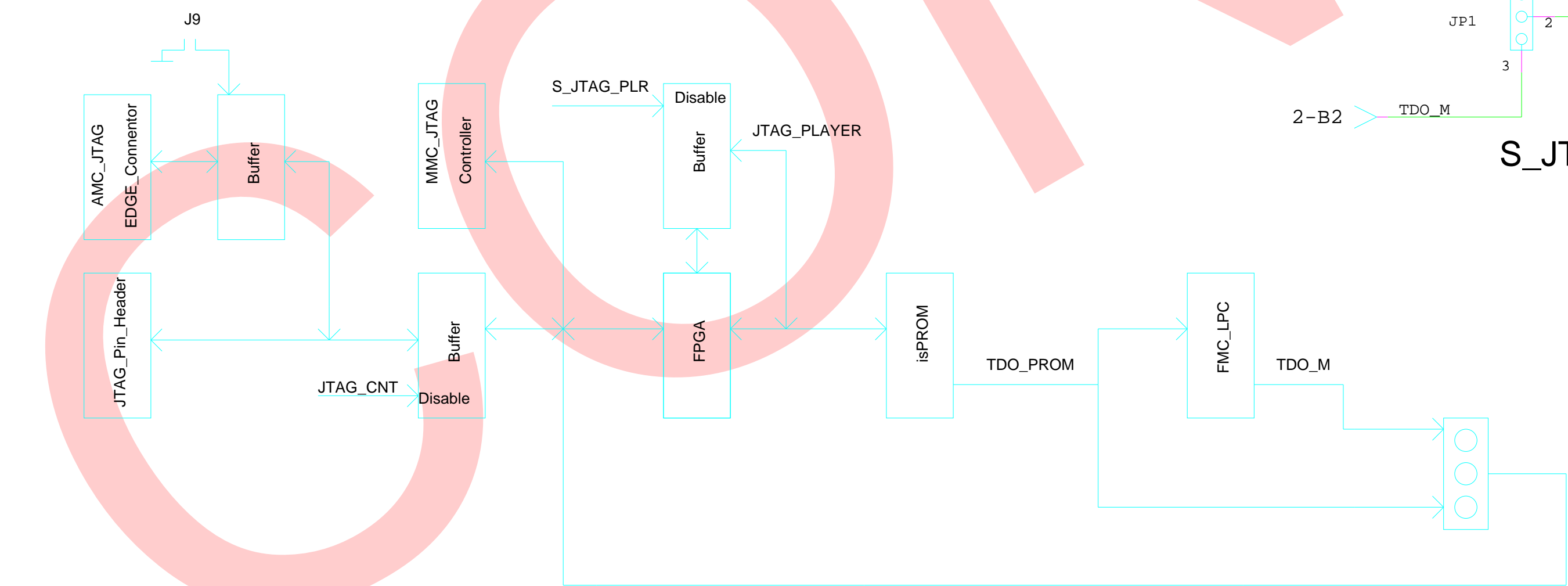
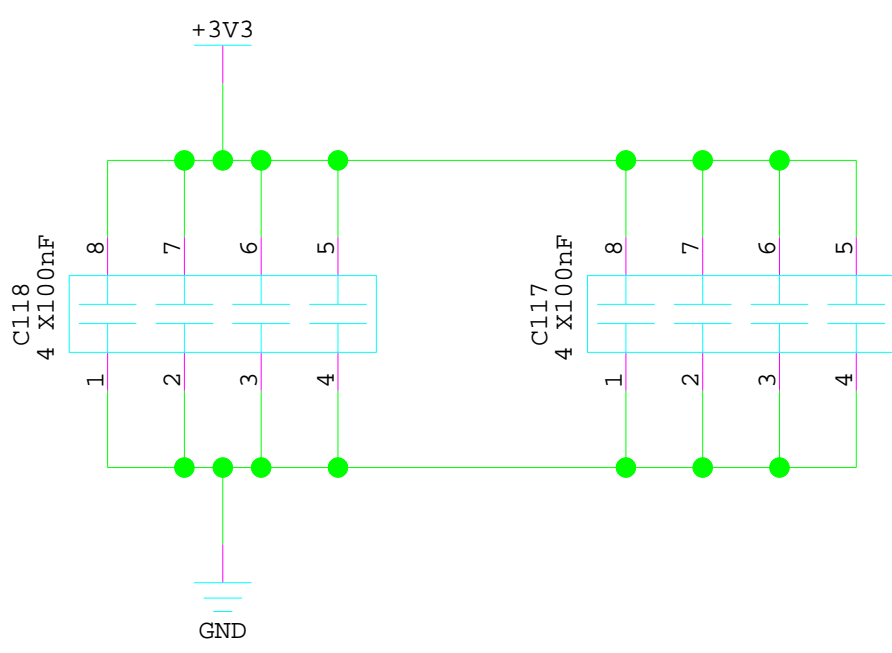
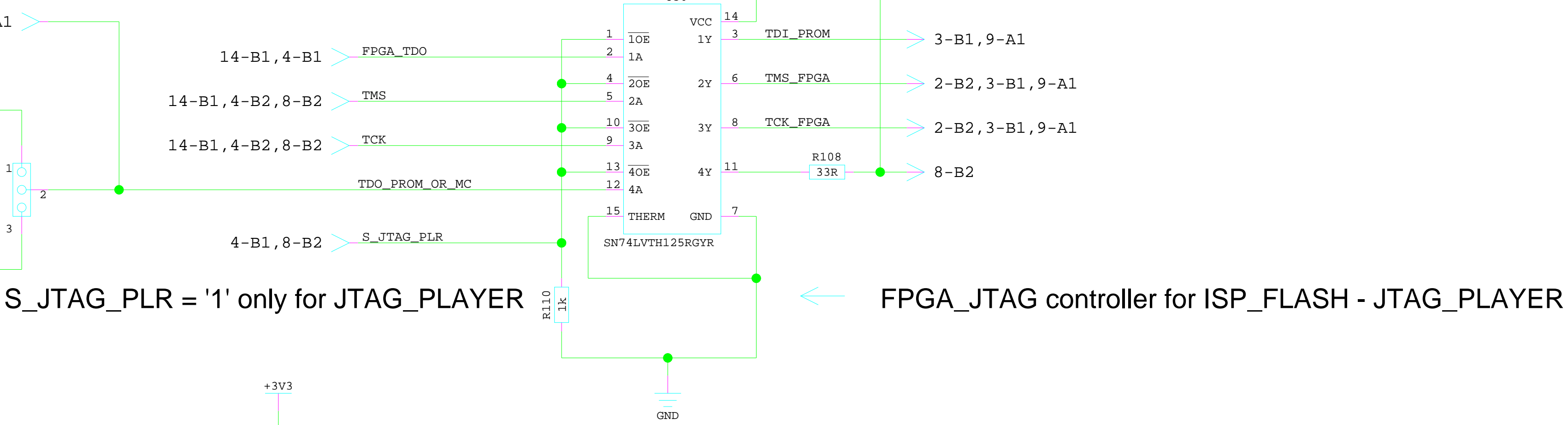
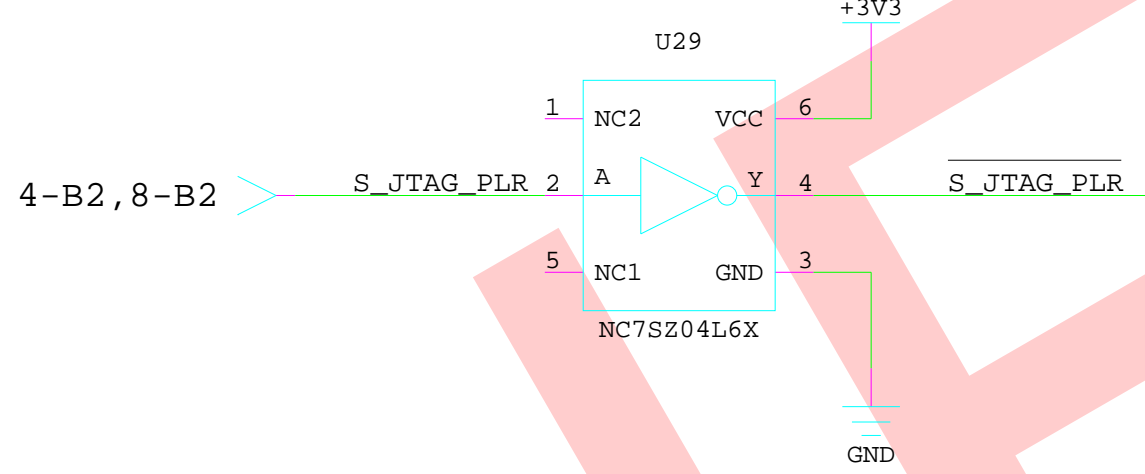
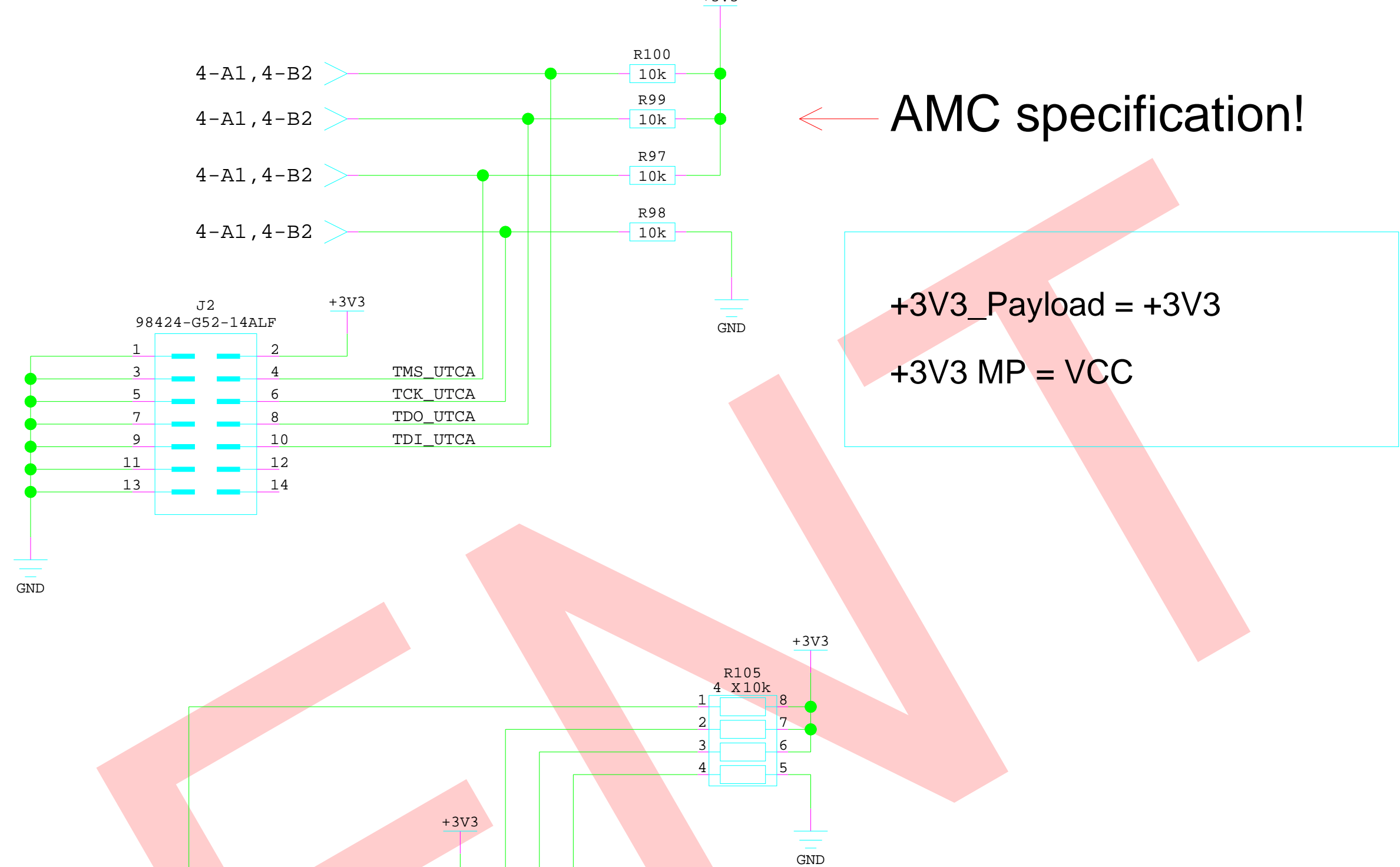
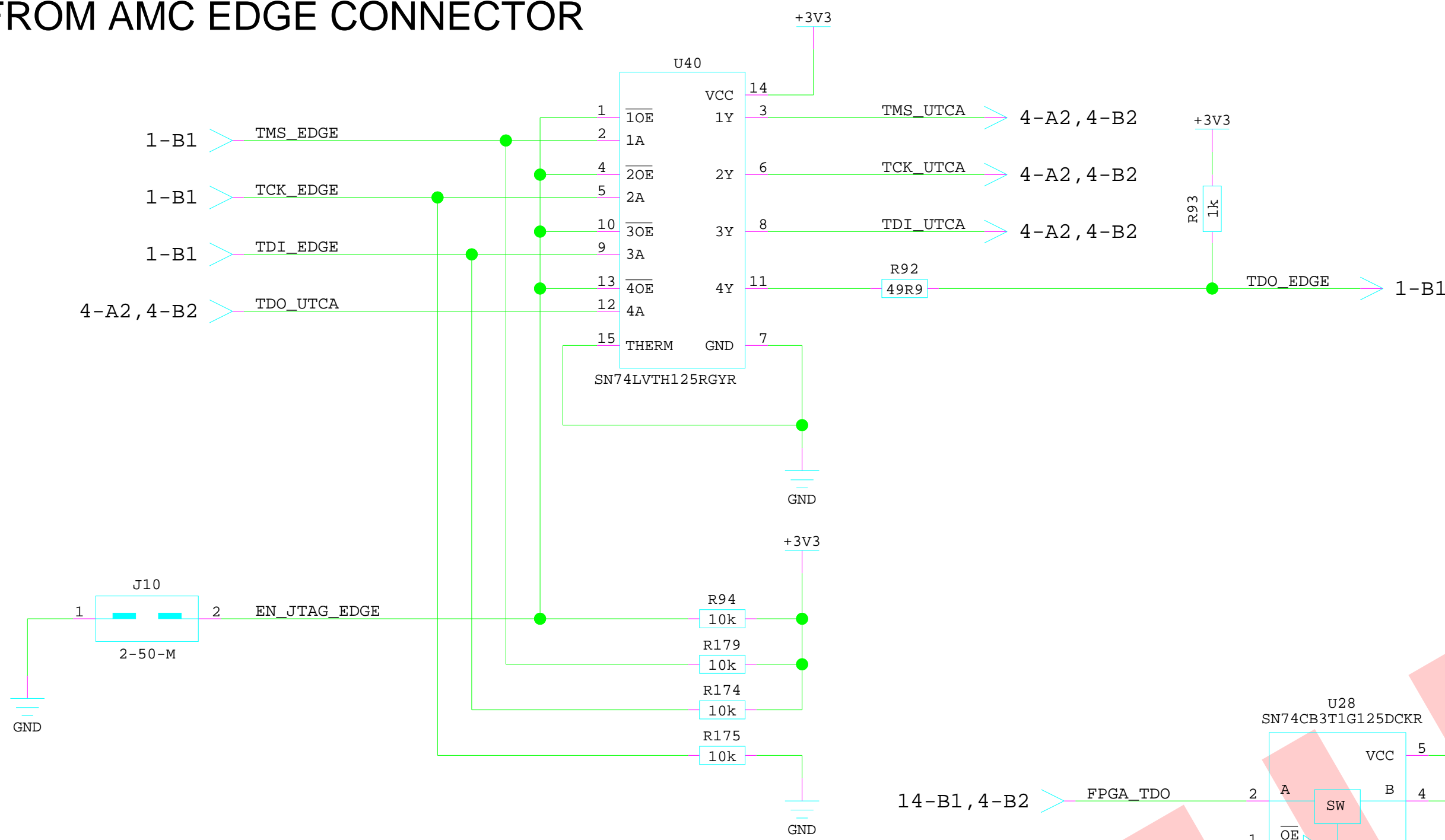
+3V3_Payload = +3V3
+3V3 MP = VCC



Developer:	Vetrov P.	ProjectFLASH Double DAMC			
		Schematic2			
Drawn by:	Vetrov P.	Sheet:			
Layouter:	Vetrov P.	DESY-FEA		Notkestrasse 85	
Changed of sch:	Vetrov P.			D-22607 Hamburg	
Date Changed:	20.8.2009	PCB No: 8423		Rev: 00	Size:A3
Date of prod. data:		PCB name:DAMC2		Sheet: 4 of 29	

JTAG Chain

JTAG SIGNALS FROM AMC EDGE CONNECTOR



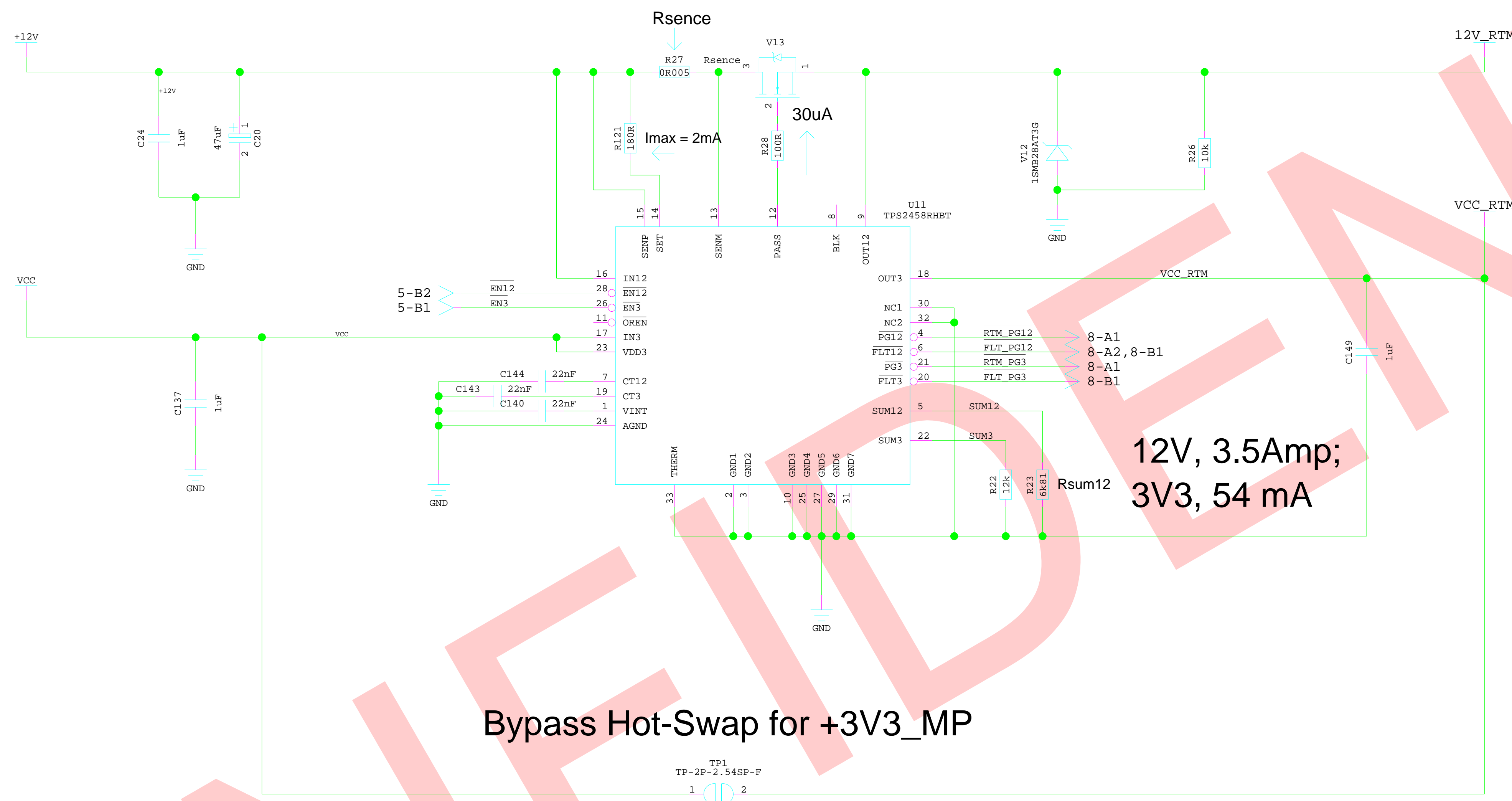
LVTH125's OUTPUT IN HIGH IMPEDANCE IF VCC <1.5V!!!!

If signal JTAG_CNT= "1", then JTAG signals will be got from MMC, otherwise from AMC edge connector or JTAG pin-header J3

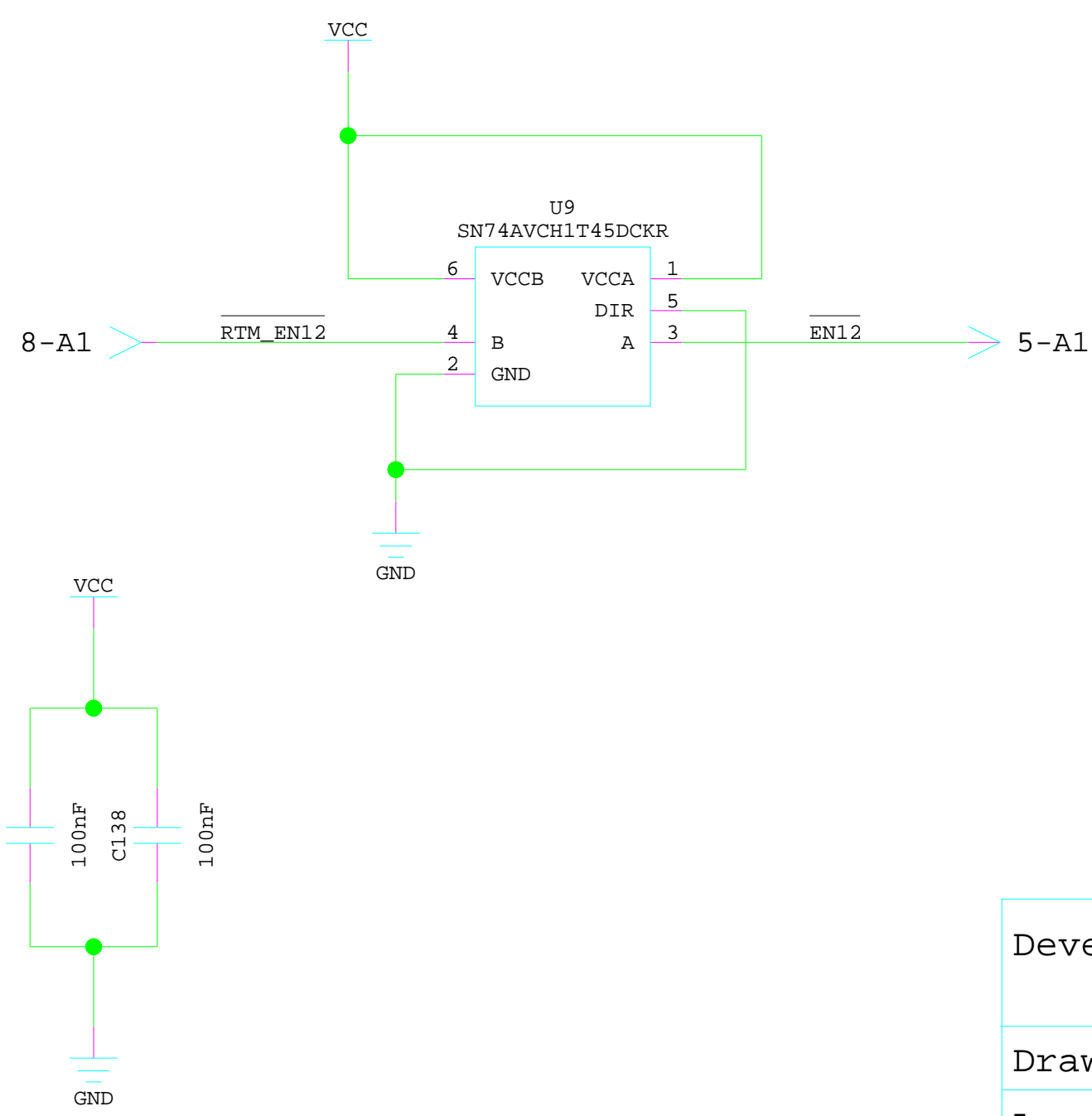
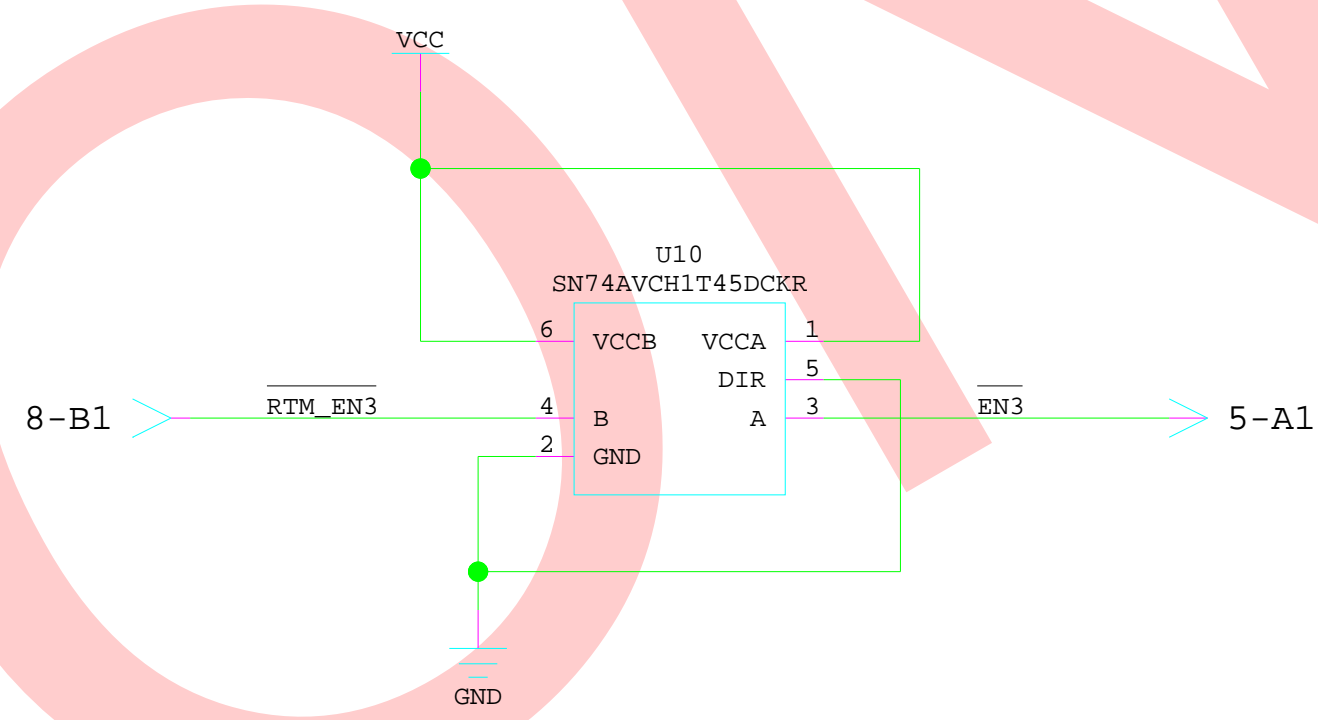
If FPGA_JTAG_PLAYER regime is set, then S_JTAG_PLR = '1' and ISP_FLASH will receive JTAG signals from XILINX and normal JTAG daisy chain will be finished on XILINX, that is FPGA_TDO will go to JTAG TDO.

Developer:	Vetrov P.	ProjectFLASH Double DAMC			
Drawn by:	Vetrov P.	Schematic2			
Layouter:	Vetrov P.	Sheet:			
Changed of sch:	Vetrov P.	DESY-FEA	Notkestrasse 85 D-22607 Hamburg		
Date Changed:	20.8.2009	PCB No: 8423	Rev: 00	Size:A3	
Date of prod. data:		PCB name:DAMC2	Sheet: 5 of 29		

uRTM Hot Swap CONTROLLER



Bypass Hot-Swap for +3V3_MP



Signals #RTM_EN12 and #RTM_EN3 are active low!
Signals #RTM_EN12 and #RTM_EN3 have internal pull-up

Developer:	Vetrov P.	ProjectFLASH Double DAMC			
Drawn by:	Vetrov P.	Schematic2			
Layouter:	Vetrov P.	Sheet:			
Changed of sch:	Vetrov P.	DESY-FEA	Notkestrasse 85 D-22607 Hamburg		
Date Changed:	20.8.2009	PCB No: 8423	Rev: 00	Size:A3	
Date of prod. data:		PCB name:DAMC2	Sheet: 6 of 29		

Interface to FMC (LPC) connector



Developer:	Vetrov P.	ProjectFLASH Double DAMC			
		Schematic2			
Drawn by:	Vetrov P.	Sheet:			
Layer:	Vetrov P.	DESY-FEA		Notkestrasse 85	
Changed of sch:	Vetrov P.			D-22607 Hamburg	
Date Changed:	20.8.2009	PCB No: 8423		Rev: 00	Size:A3
Date of prod. data:		PCB name:DAMC2		Sheet: 7 of 29	

PCIExpress Clock

True Table

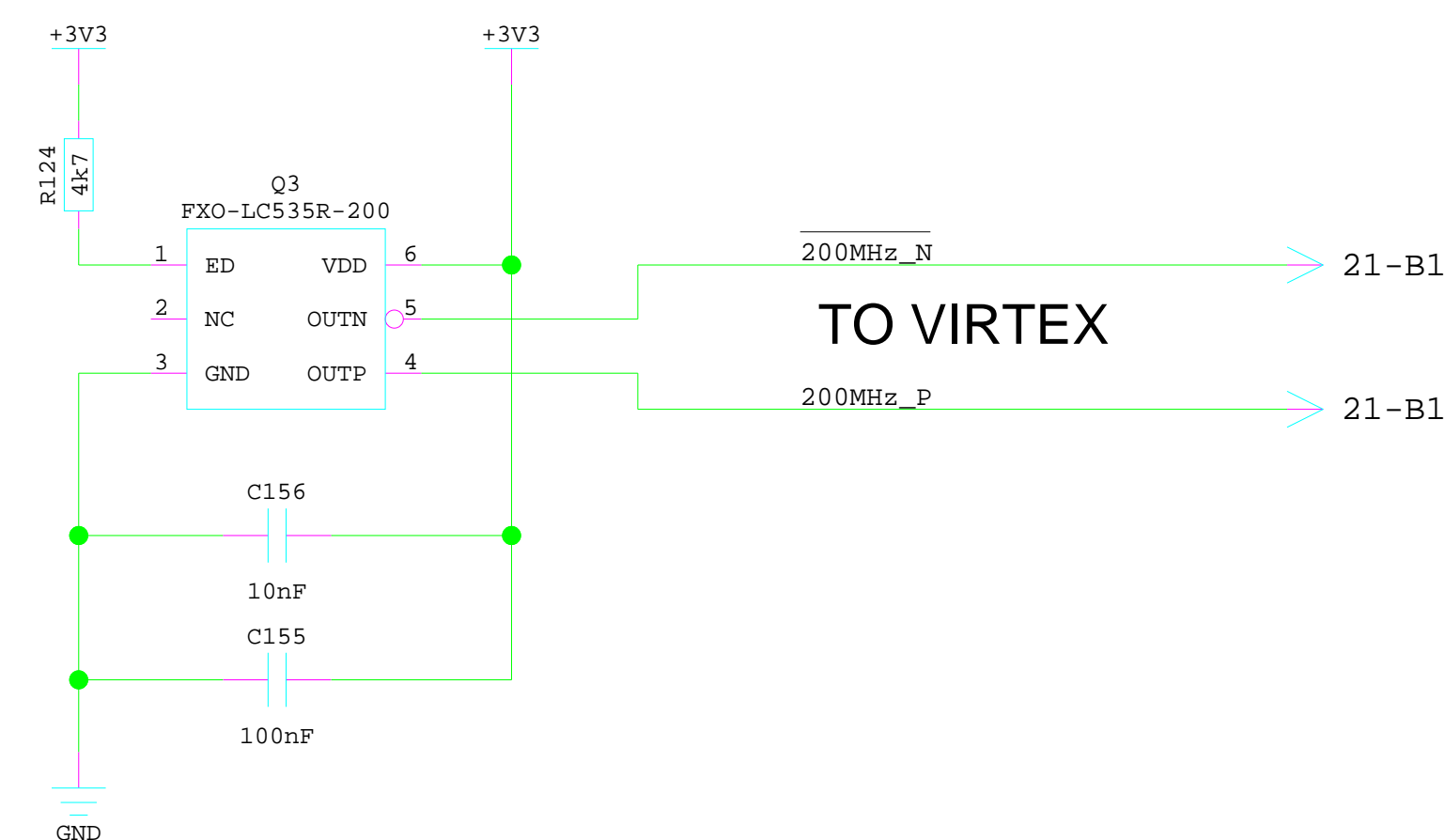
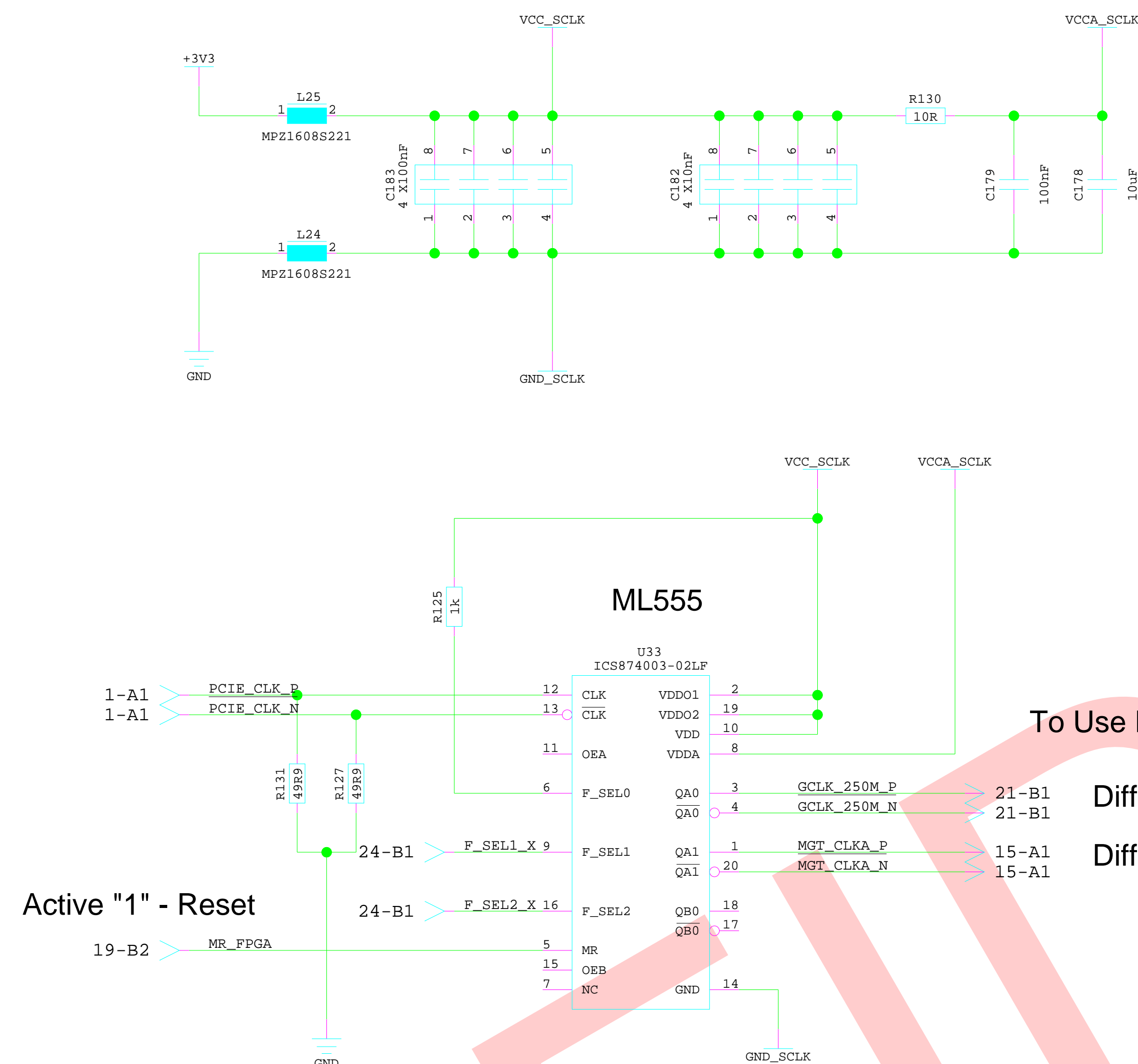
Inputs			Outputs	
F_SEL2	F_SEL1	F_SEL0	QA0/nQA0, QA1/nQA1	QB0/nQB0
0	0	0	/2	/2
1	0	0	/5	/2
0	1	0	/4	/2
1	1	0	/2	/4
0	0	1	/2	/5
1	0	1	/5	/4
0	1	1	/4	/5
1	1	1	/4	/4

To Use Differential Termination Attribute in FPGA for supporting LVDS signals

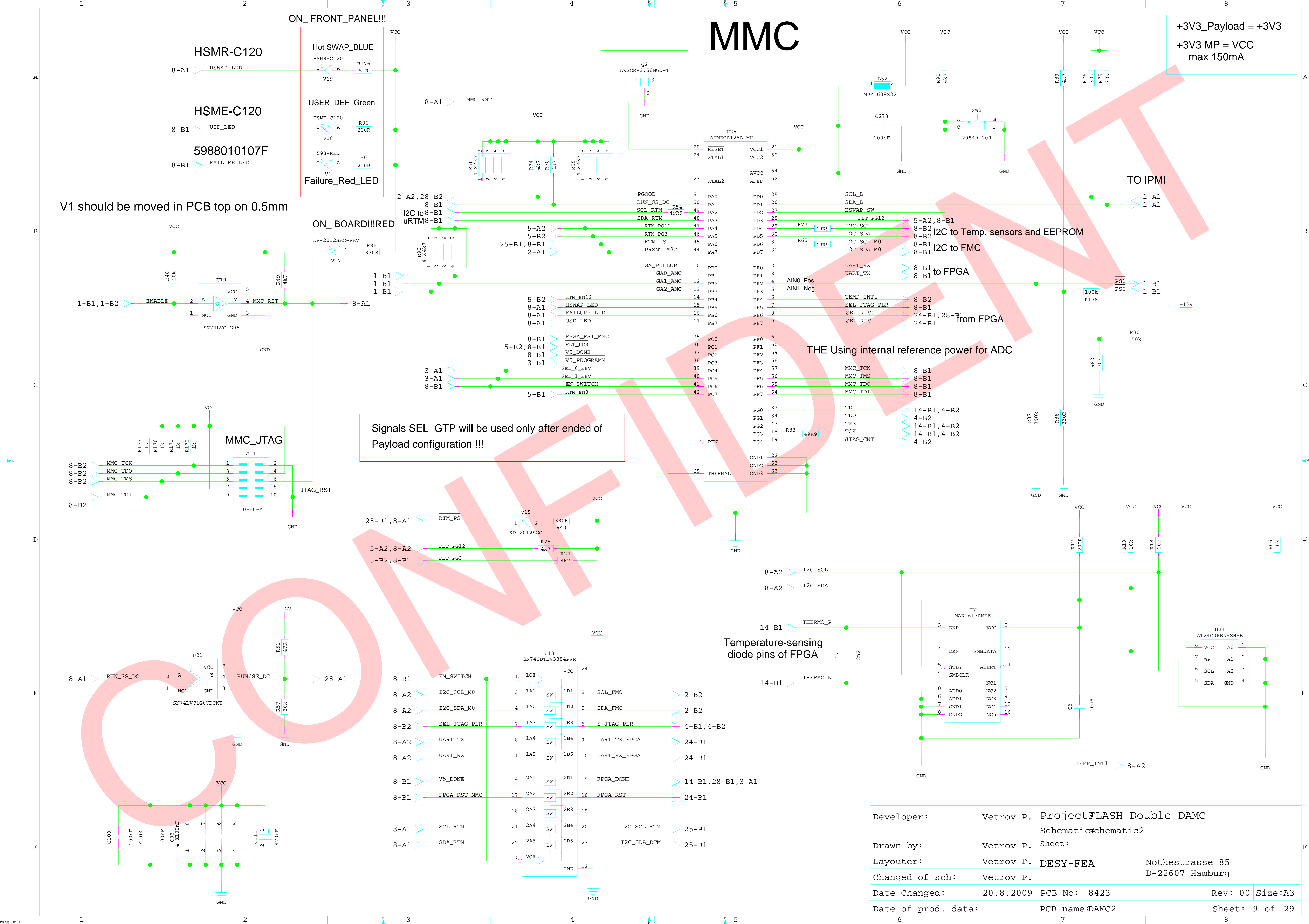
Differential Global Clock input of FPGA(GCLK) - 250MHz

Differential reference clock for GTP transceiver(MGT_REFCLK) - 250MHz

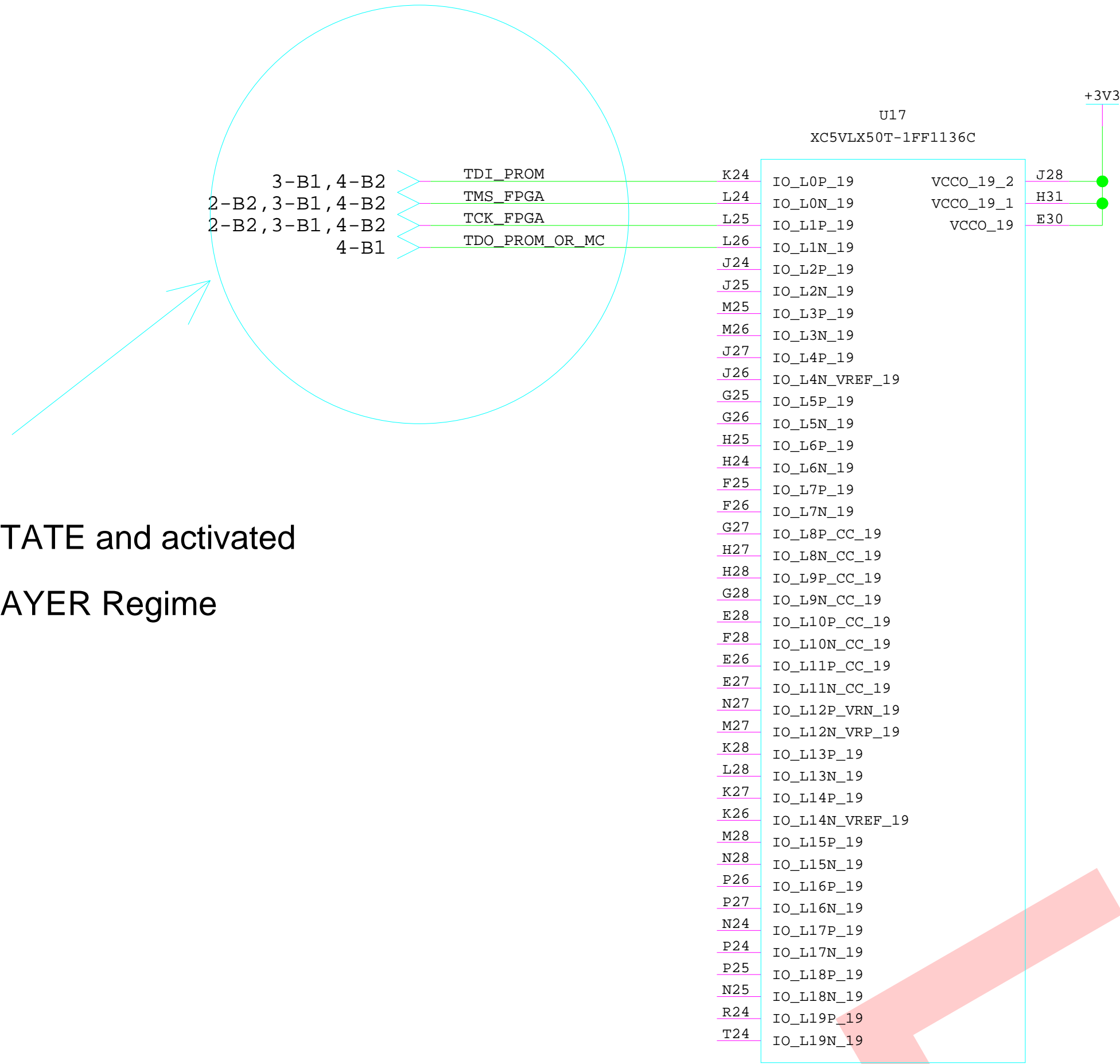
IODELAY CLOCK



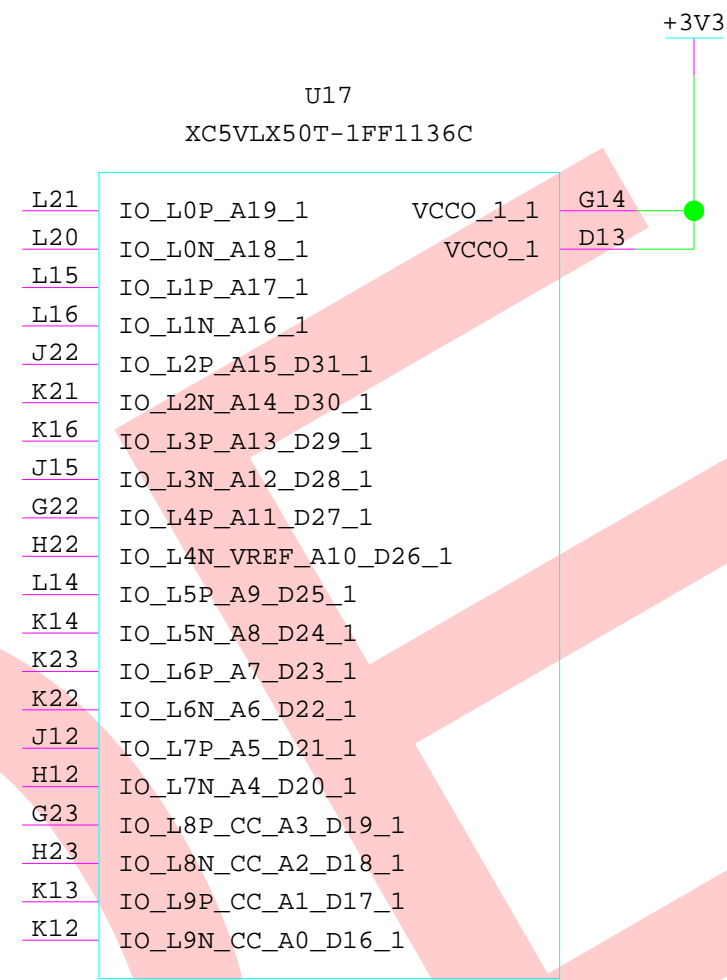
Developer:	Vetrov P.	Project: FLASH Double DAMC		
Drawn by:	Vetrov P.	Schematic: schematic2		
Layouter:	Vetrov P.	Sheet:		
Changed of sch:	Vetrov P.	DESY-FEA	Notkestrasse 85 D-22607 Hamburg	
Date Changed:	20.8.2009	PCB No: 8423	Rev: 00	Size: A3
Date of prod. data:		PCB name: DAMC2	Sheet: 8 of 29	



SPARE VIRTEX-5 BANKS



Shall be in TRI STATE and activated
only in JTAG_PLAYER Regime



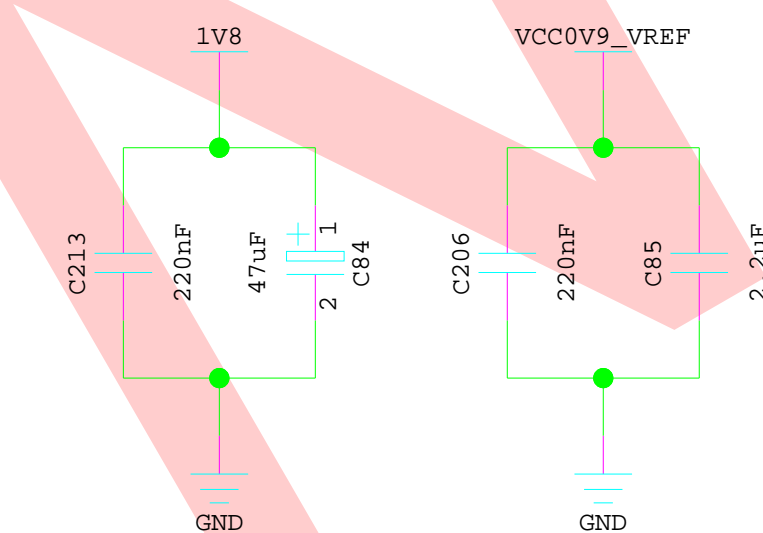
VDD = 1V8;
Vref = 1/2 VDD = 0V9

Developer:	Vetrov P.	ProjectFLASH Double DAMC			
		Schematic2			
Drawn by:	Vetrov P.	Sheet:			
Layouter:	Vetrov P.	DESY-FEA Notkestrasse 85 D-22607 Hamburg			
Changed of sch:	Vetrov P.				
Date Changed:	20.8.2009	PCB No: 8423		Rev: 00	Size:A3
Date of prod. data:		PCB name:DAMC2		Sheet:10 of 29	

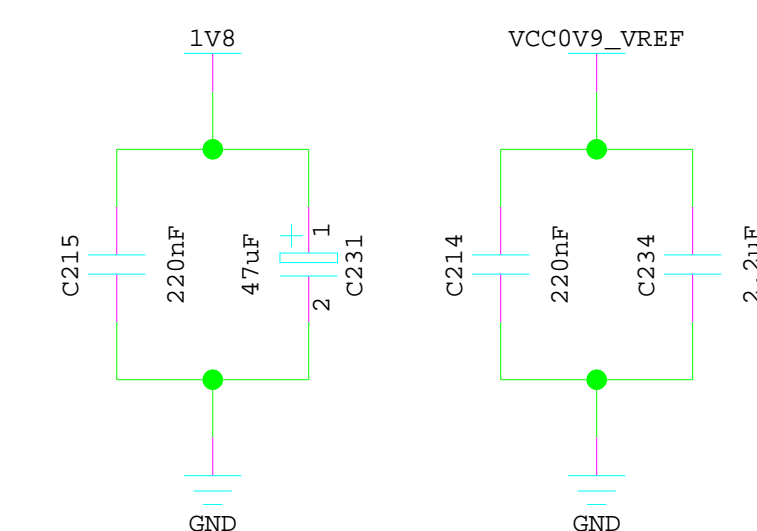
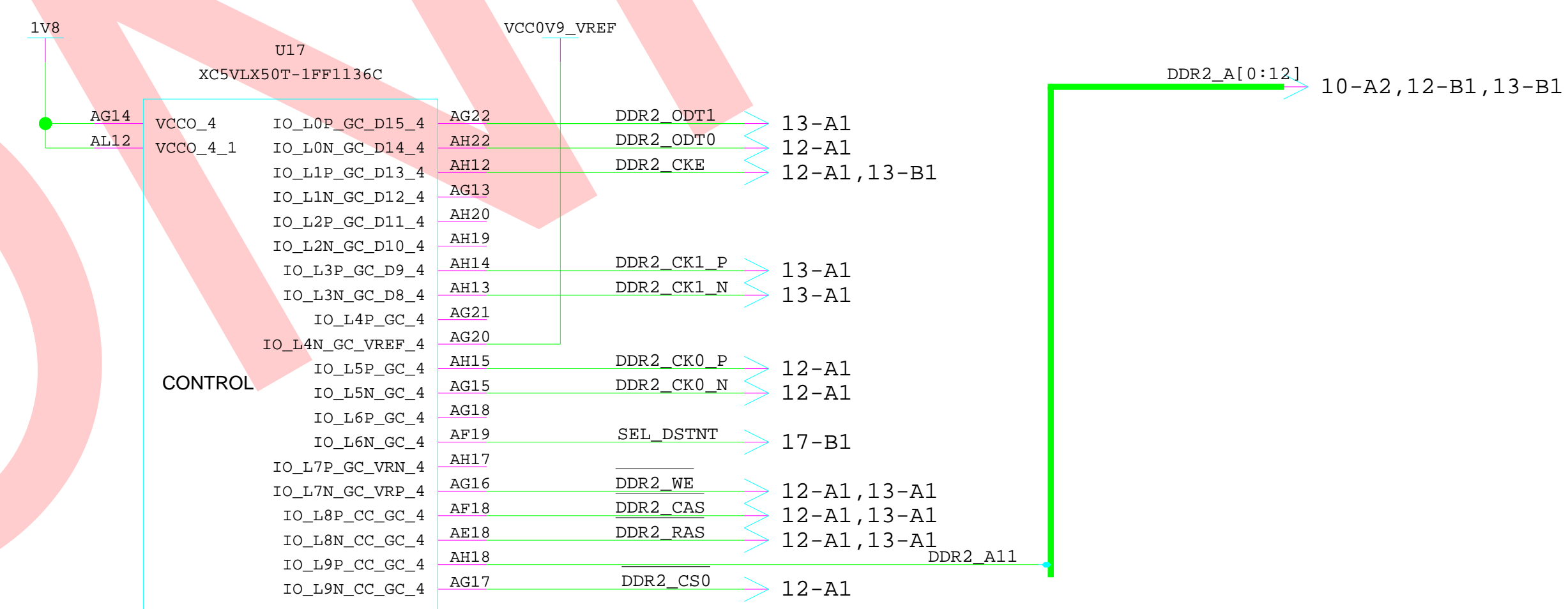
Revision Numbers, should be connected to MMC - sel_rev!

Signal	Connection
AE13	12-A1, 13-B1
AE12	12-A1, 13-B1
AF23	12-A1, 13-B1
AG23	12-A1, 13-B1
AF13	12-A1, 13-B1
AG12	12-A1, 13-B1
AE22	12-A1, 13-B1
AE23	12-A1, 13-B1
AE14	12-A1, 13-B1
AF14	12-A1, 13-B1
AF20	12-A1, 13-B1
AF21	12-A1, 13-B1
AF15	12-A1, 13-B1
AE16	12-A1, 13-B1
AE21	12-A1, 13-B1
AD20	12-A1, 13-B1
AF16	12-A1, 13-B1
AE17	12-A1, 13-B1
AE19	12-A1, 13-B1
AD19	12-A1, 13-B1

DDR2_A[0:12] → 10-B2, 12-B1, 13-B1

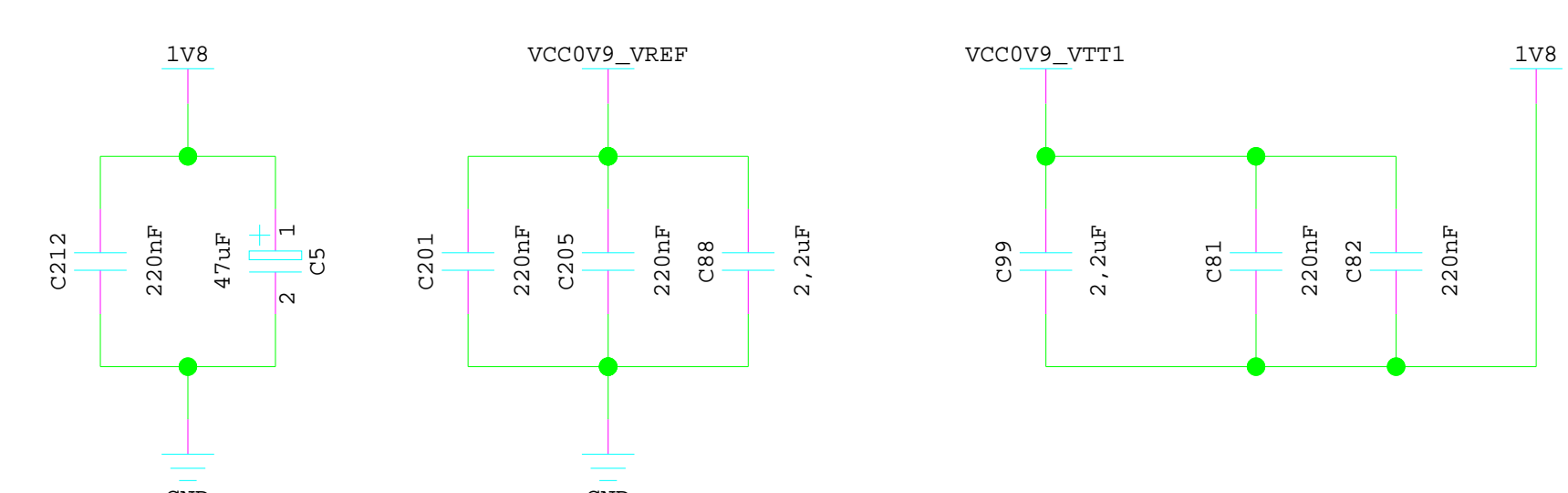
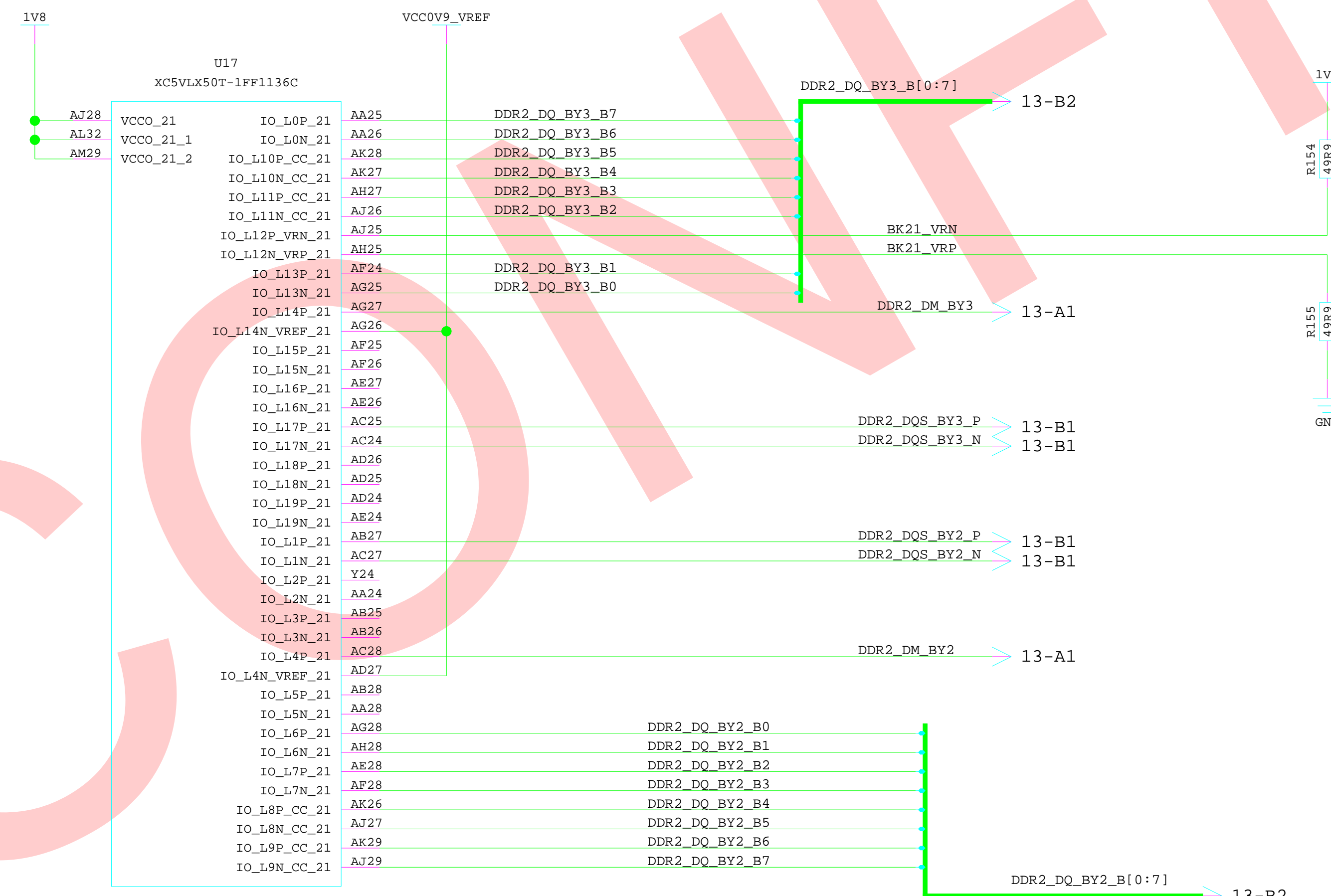
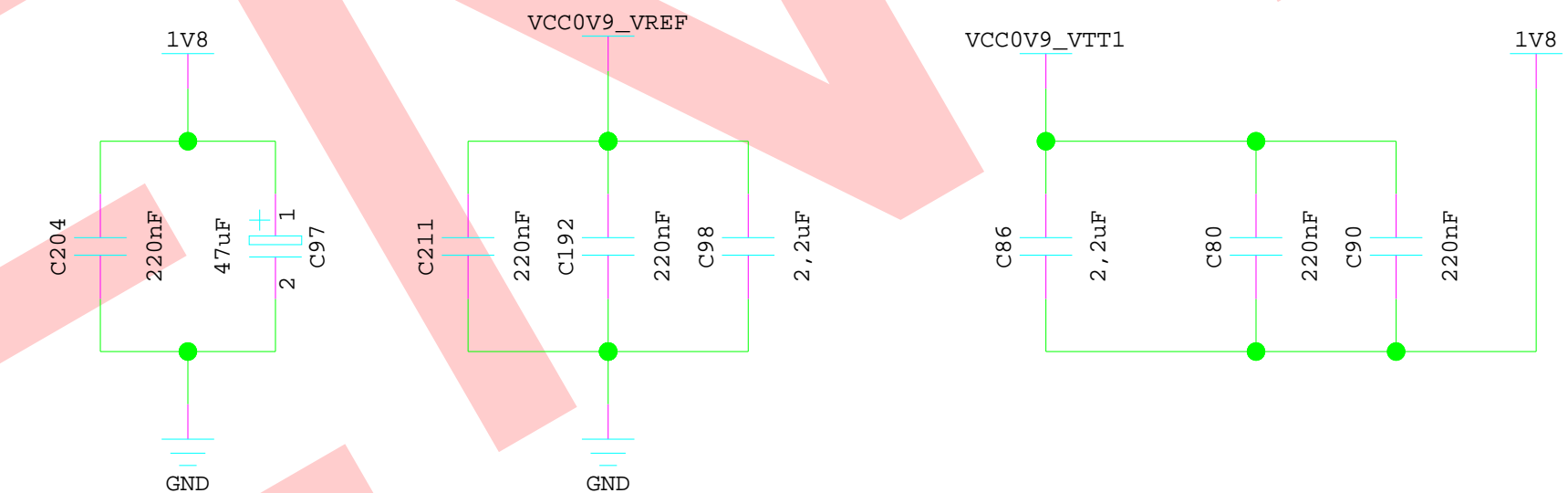
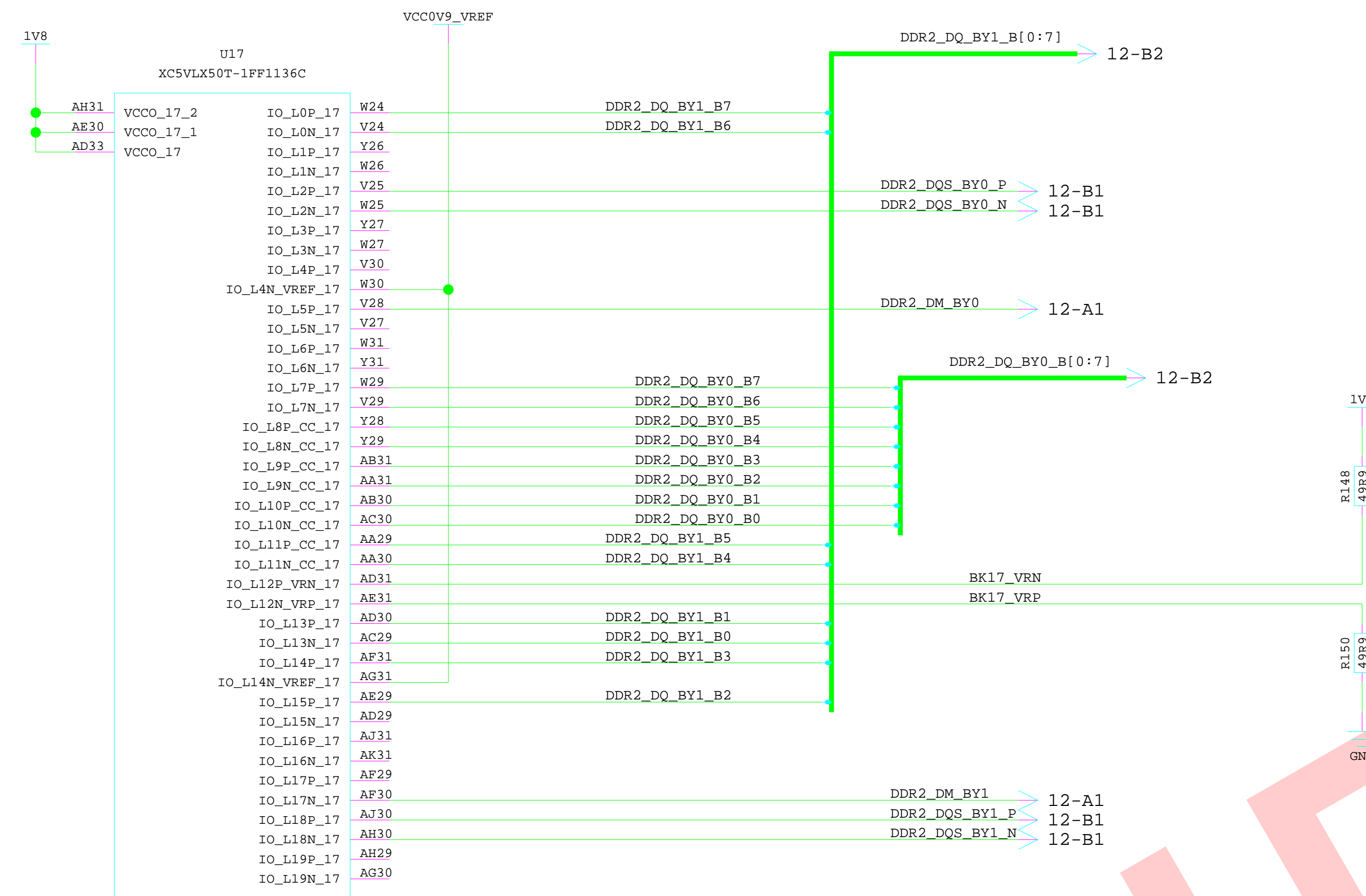


Note that DDR2 ODT does NOT act on the address/control signals, so its usually a good idea to continue to descrete terminate these signals at the memory end of the line.



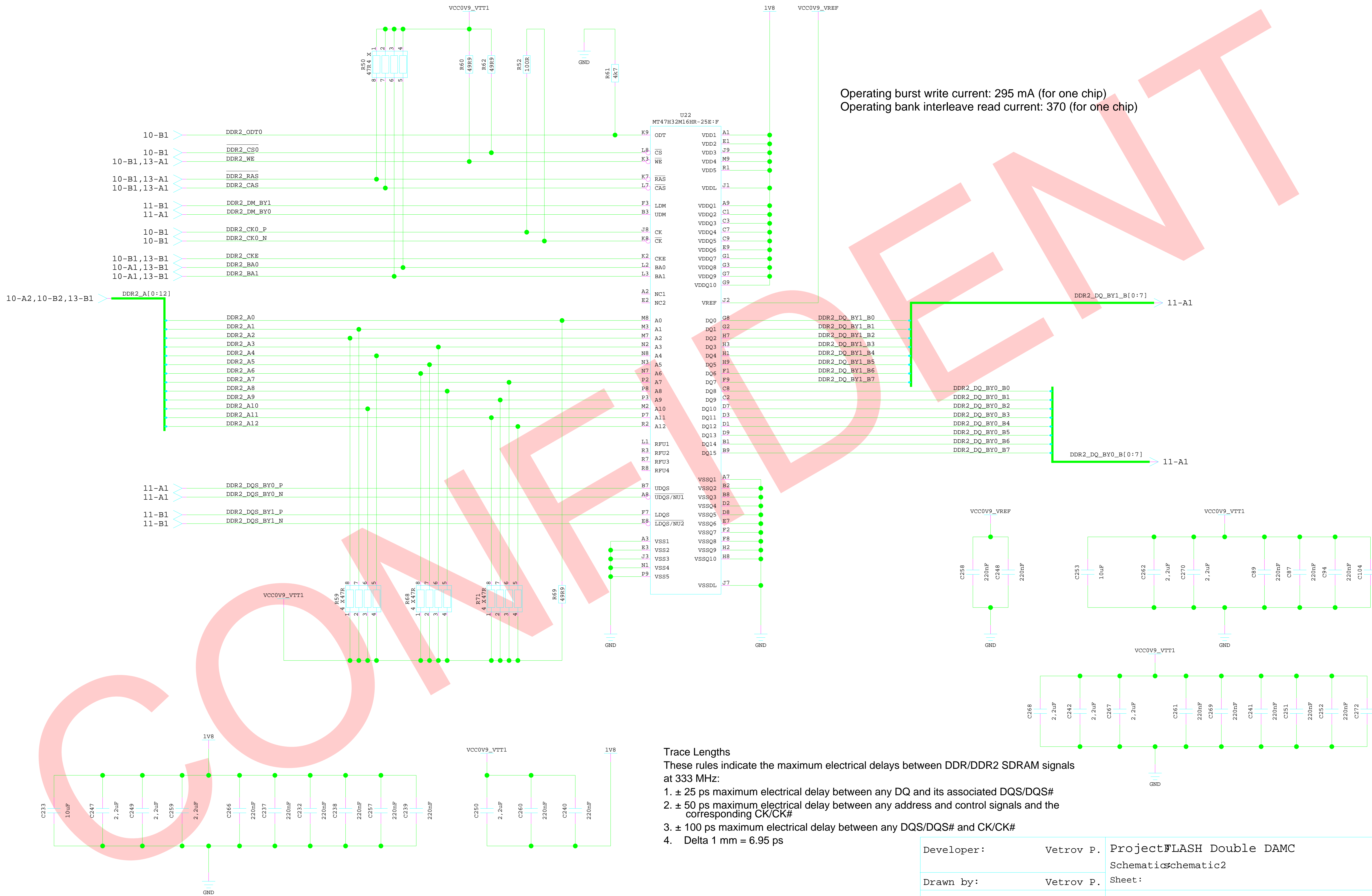
Developer:	Vetrov P.	Project:FLASH Double DAMC		
Drawn by:	Vetrov P.	Schematic:Schematic2		
Layouter:	Vetrov P.	Sheet:		
Changed of sch:	Vetrov P.	DESY-FEA	Notkestrasse 85	
Date Changed:	20.8.2009	PCB No: 8423	Rev: 00	Size:A3
Date of prod. data:		PCB name:DAMC2	Sheet:11 of 29	

DDR2 data and control signals



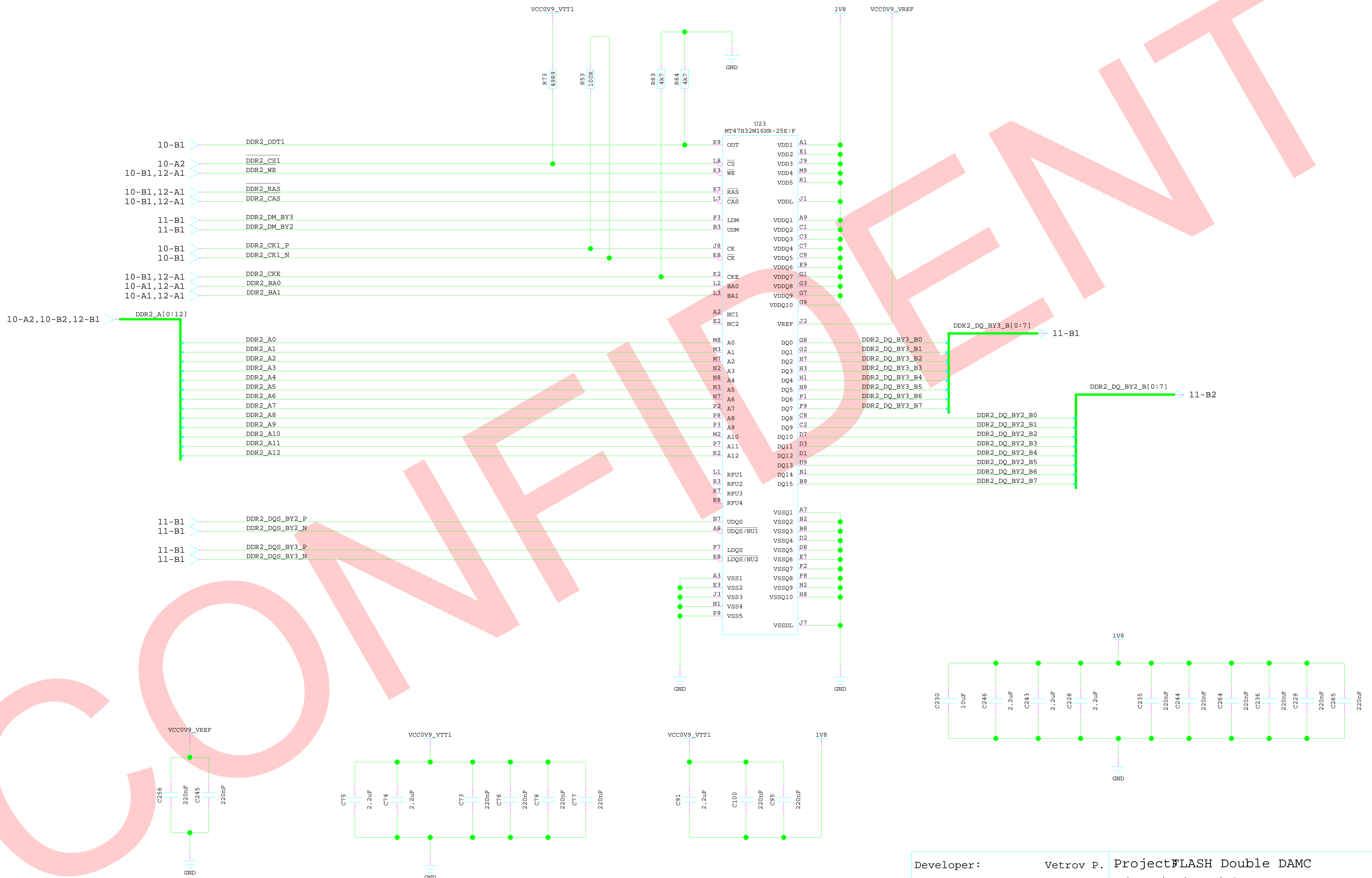
Developer:	Vetrov P.	ProjectFLASH Double DAMC Schematic2			
Drawn by:	Vetrov P.	Sheet:			
Layouter:	Vetrov P.	DESY-FEA		Notkestrasse 85	
Changed of sch:	Vetrov P.			D-22607 Hamburg	
Date Changed:	20.8.2009	PCB No: 8423		Rev: 00	Size:A3
Date of prod. data:		PCB name:DAMC2		Sheet:12 of 29	

DDR2 Bytes 0&1 - ODT(64 MByte)



Developer:	Vetrov P.	ProjectFLASH Double DAMC			
		Schematic2			
Drawn by:	Vetrov P.	Sheet:			
Layouter:	Vetrov P.	DESY-FEA		Notkestrasse 85	
Changed of sch:	Vetrov P.			D-22607 Hamburg	
Date Changed:	20.8.2009	PCB No: 8423		Rev: 00	Size:A3
Date of prod. data:		PCB name:DAMC2		Sheet:13 of 29	

DDR2 Bytes 2&3 - ODT (+64MByte)

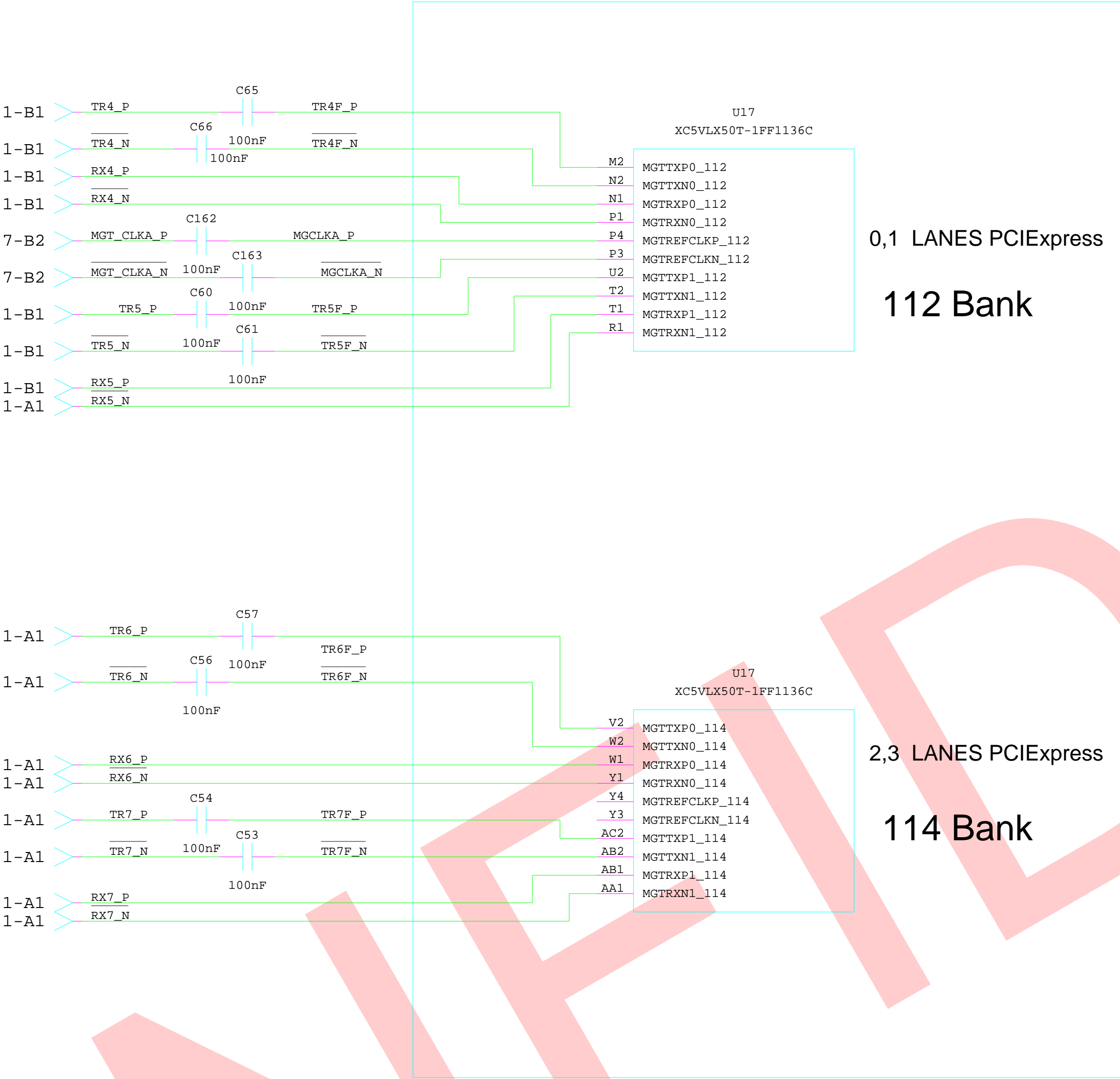


Developer:	Vetrov P.	ProjectFLASH Double DAMC		
Drawn by:	Vetrov P.	Schematic2		
Layouter:	Vetrov P.	Sheet:		
Changed of sch:	Vetrov P.	DESY-FEA Notkestrasse 85 D-22607 Hamburg		
Date Changed:	20.8.2009	PCB No: 8423	Rev: 00	Size:A3
Date of prod. data:		PCB name:DAMC2	Sheet:14 of 29	

Developer:	Vetrov P.	ProjectFLASH Double DAMC		
Drawn by:	Vetrov P.	Schematic2		
Layouter:	Vetrov P.	Sheet:		
Changed of sch:	Vetrov P.	DESY-FEA Notkestrasse 85 D-22607 Hamburg		
Date Changed:	20.8.2009	PCB No: 8423	Rev: 00	Size:A3
Date of prod. data:		PCB name:DAMC2	Sheet:15 of 29	

4 LANES PCIExpress to back plane

PCIE_GCLK_N/P



FOR GTP reference clock total jitter, peak-peak < 40 ps

Min. output clock jitter for VIRTEX-5 120 ps

AVCC 1.0V - 110mA per DUAL_GTP= 0.66A

AVCCPLL 1.2V - 60mA per DUAL_GTP = 0.36A

AVTTTX 1.2V - 90mA per DUAL_GTP = 0.09A * 6 = 0.54 A

AVTTTRX 1.2V - 50mA per DUAL_GTP = 0.003A

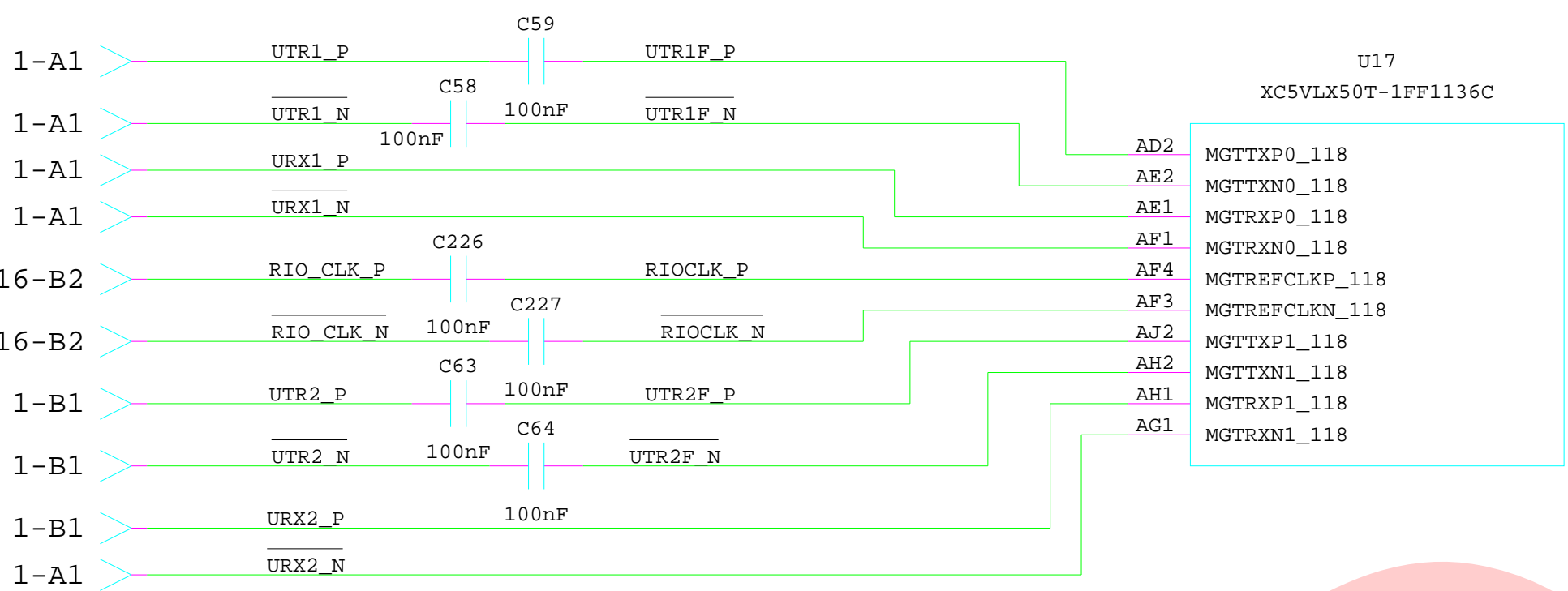
AVTTTRXC 1.2V - 0.5mA per DUAL_GTP = 0.003A

One Regulator = 1.152 A

Look_DS202

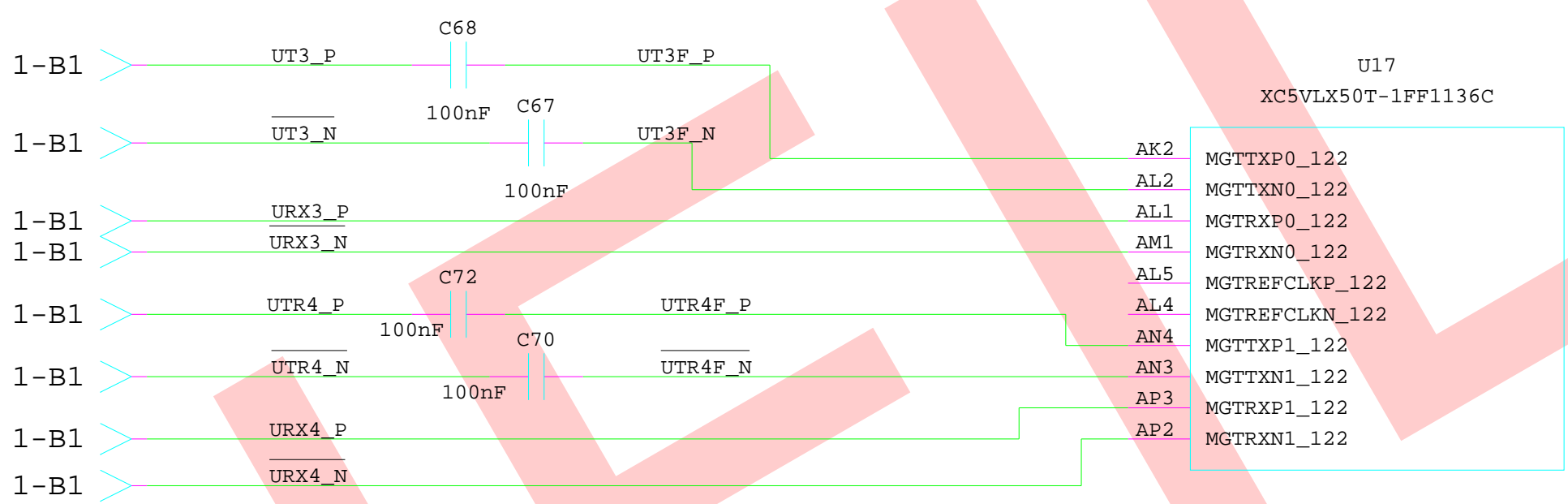
Developer:	Vetrov P.	ProjectFLASH Double DAMC			
		Schematic2			
Drawn by:	Vetrov P.	Sheet:			
Layouter:	Vetrov P.	DESY-FEA			
Changed of sch:	Vetrov P.	Notkestrasse 85			
		D-22607 Hamburg			
Date Changed:	20.8.2009	PCB No: 8423		Rev: 00	Size:A3
Date of prod. data:		PCB name:DAMC2		Sheet:16 of 29	

4 LANES to EDGE Connector - Ports 12-15



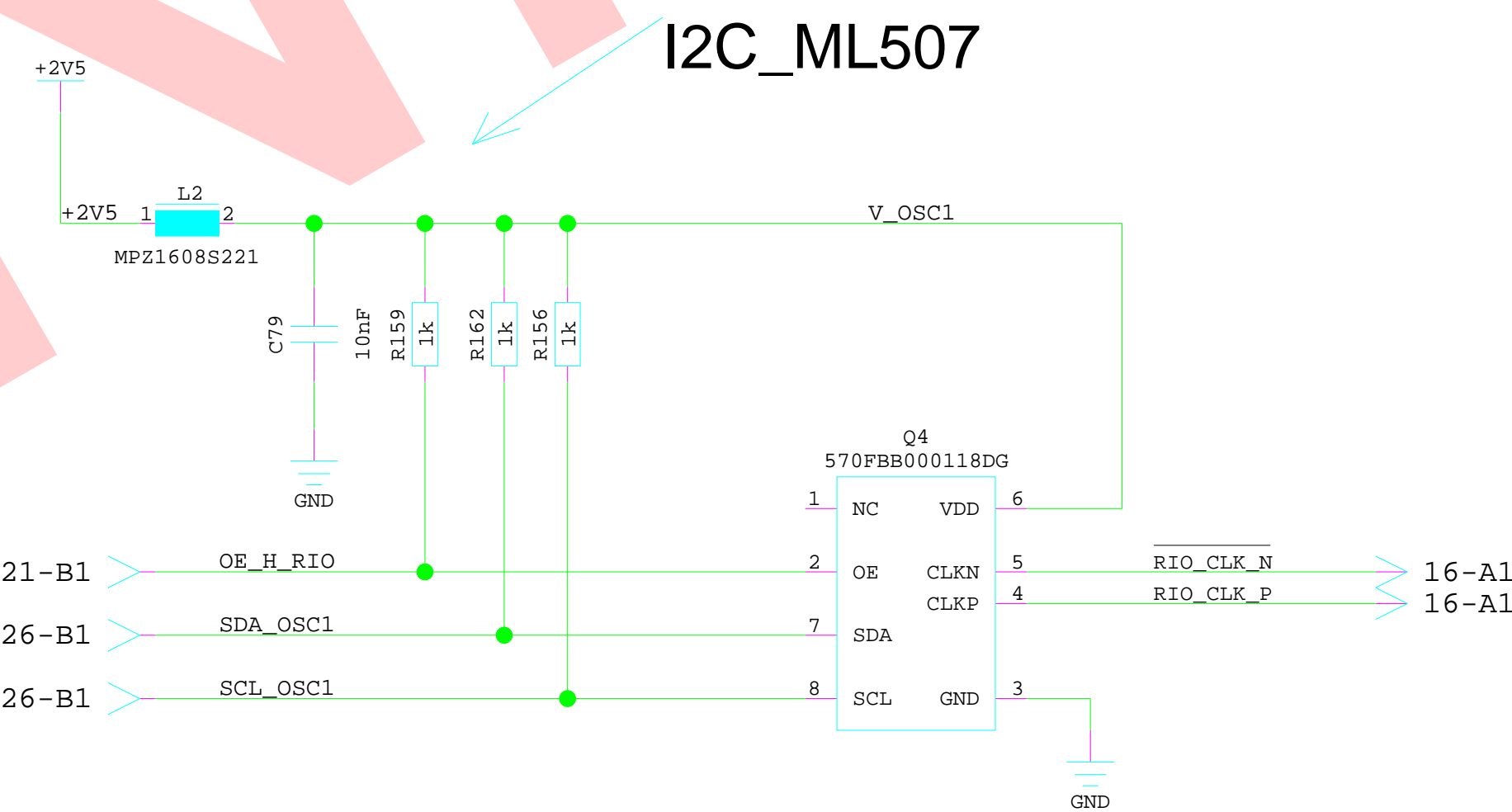
0,1 LANES RocketIO

118 Bank



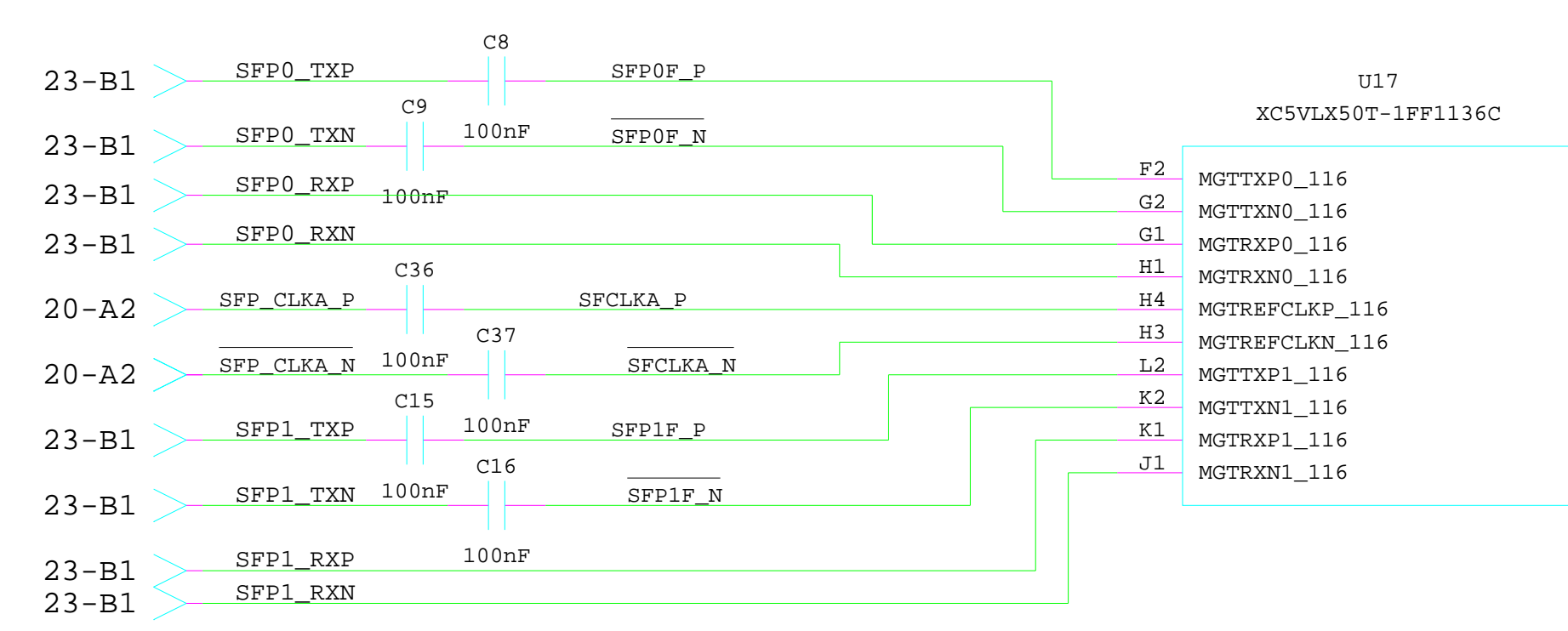
2,3 LANES RocketIO

122 Bank

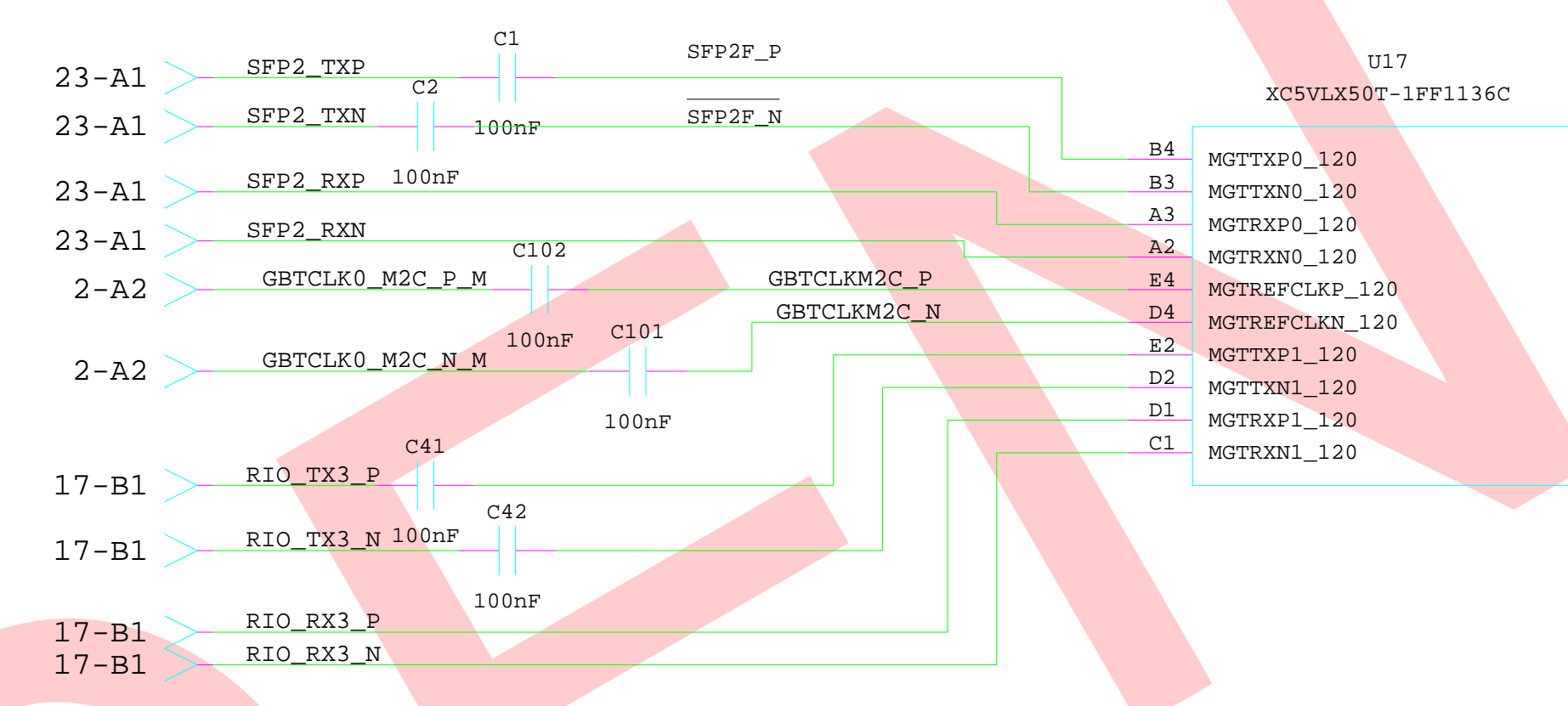


Developer:	Vetrov P.	ProjectFLASH Double DAMC			
		Schematic2			
Drawn by:	Vetrov P.	Sheet:			
Layouter:	Vetrov P.	DESY-FEA			
Changed of sch:	Vetrov P.	Notkestrasse 85 D-22607 Hamburg			
Date Changed:	20.8.2009	PCB No: 8423	Rev: 00	Size:A3	
Date of prod. data:		PCB name:DAMC2	Sheet:17 of 29		

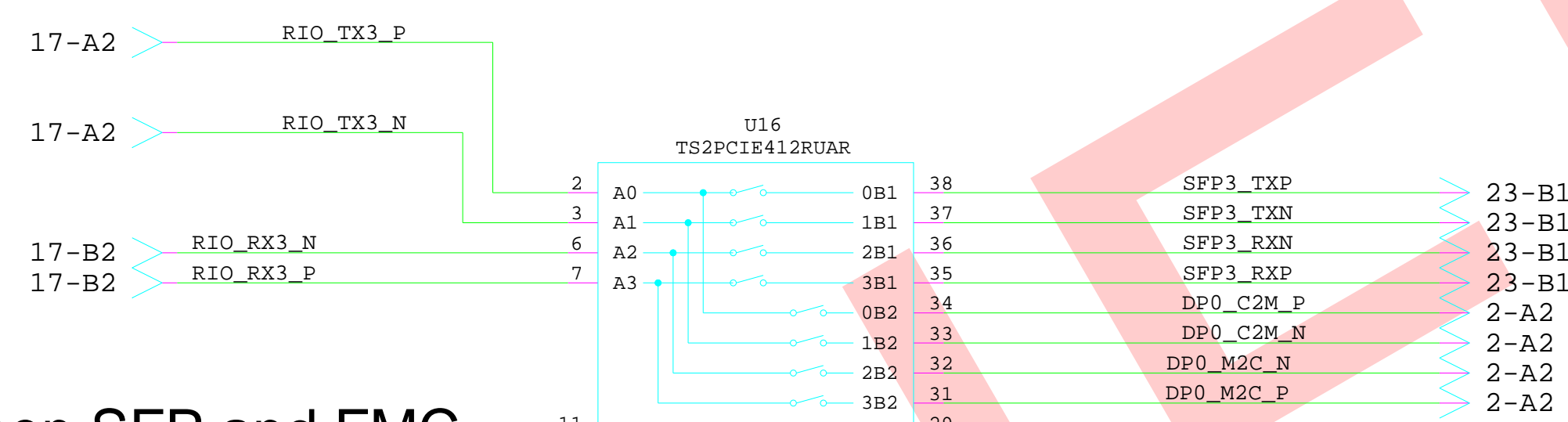
3 Lanes to SFP connectors and one to SFP or to FMC



clock for 4 LANES SFP
0,1 LANES SFP
116 Bank

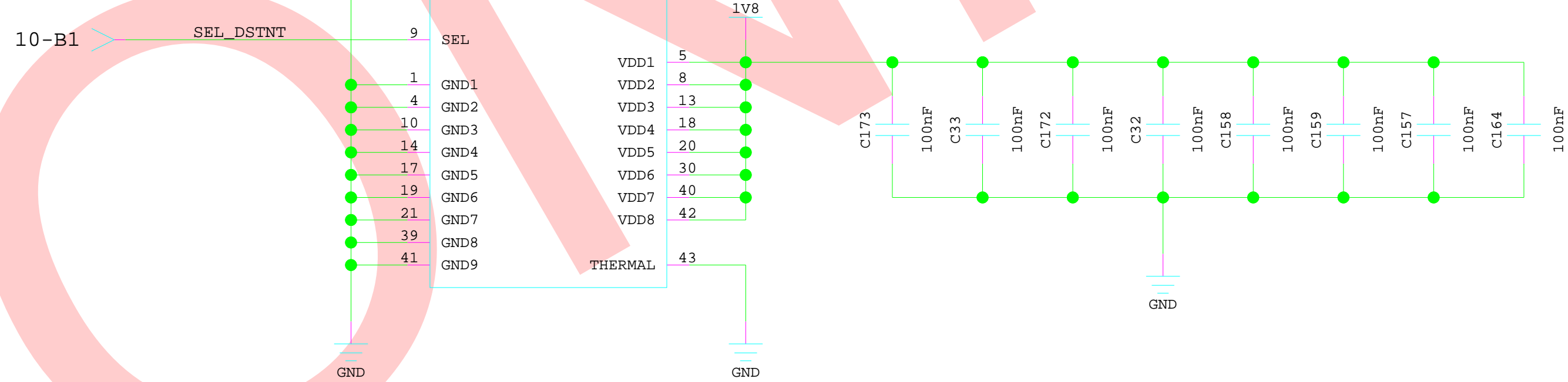


2,3 LANES SFP
120 Bank



SWITCH between SFP and FMC
Bandwidth over 3 Gbit/s

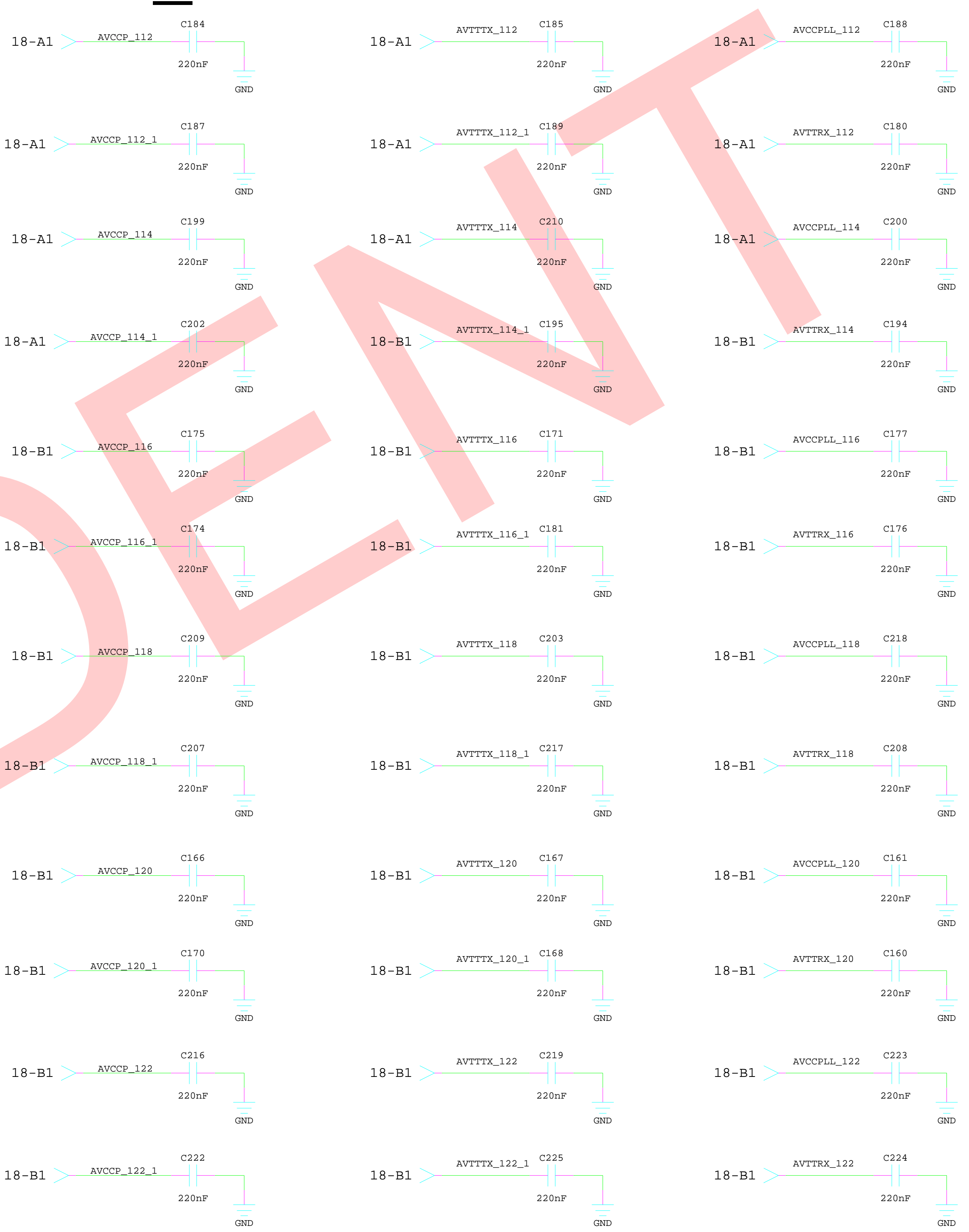
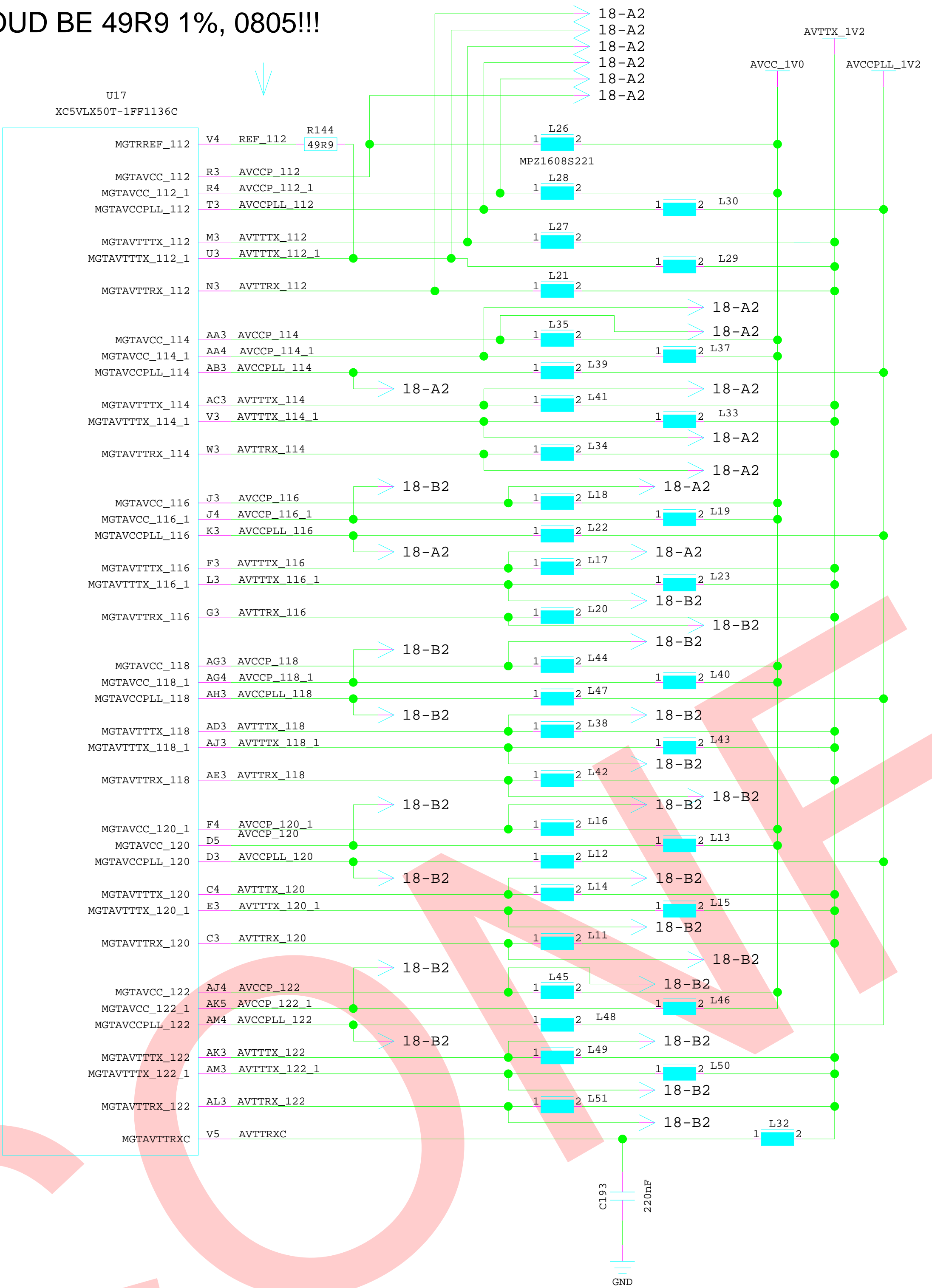
Reference clock needs to arrive at one of the GTP tiles chosen in the design and routed to the other GTP tiles. The reference clock arriving at one GTP tile can be routed to any other GTP tile that is up to three GTP tiles away in either the north or south direction. The GTP



Developer:	Vetrov P.	ProjectFLASH Double DAMC Schematic2			
Drawn by:	Vetrov P.	Sheet:			
Layouter:	Vetrov P.	DESY-FEA		Notkestrasse 85	
Changed of sch:	Vetrov P.			D-22607 Hamburg	
Date Changed:	20.8.2009	PCB No: 8423		Rev: 00	Size:A3
Date of prod. data:		PCB name:DAMC2		Sheet:18 of 29	

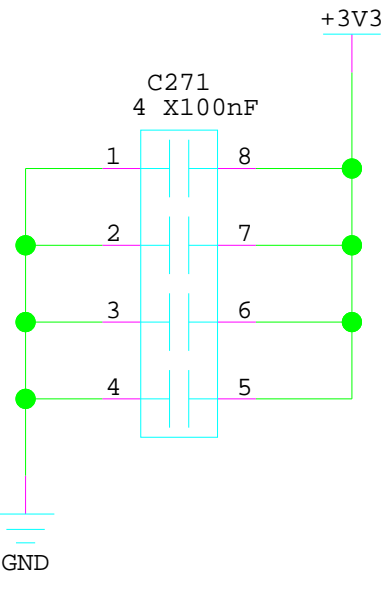
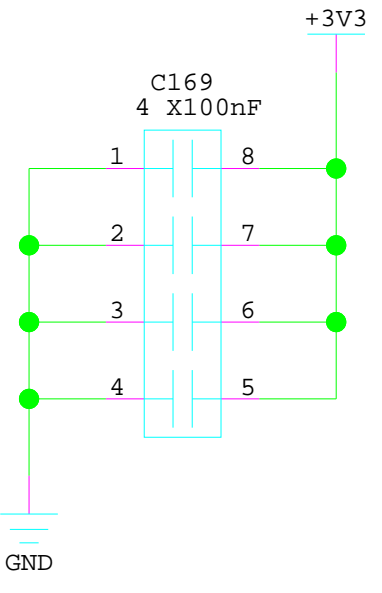
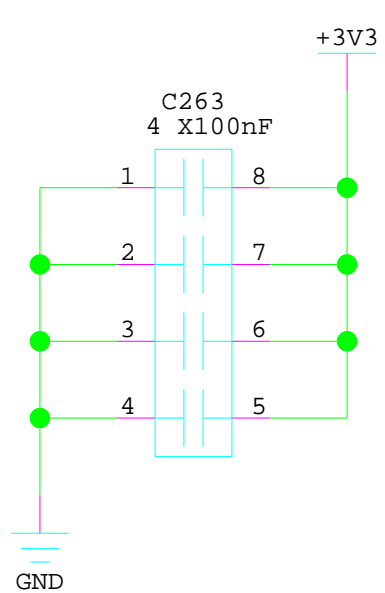
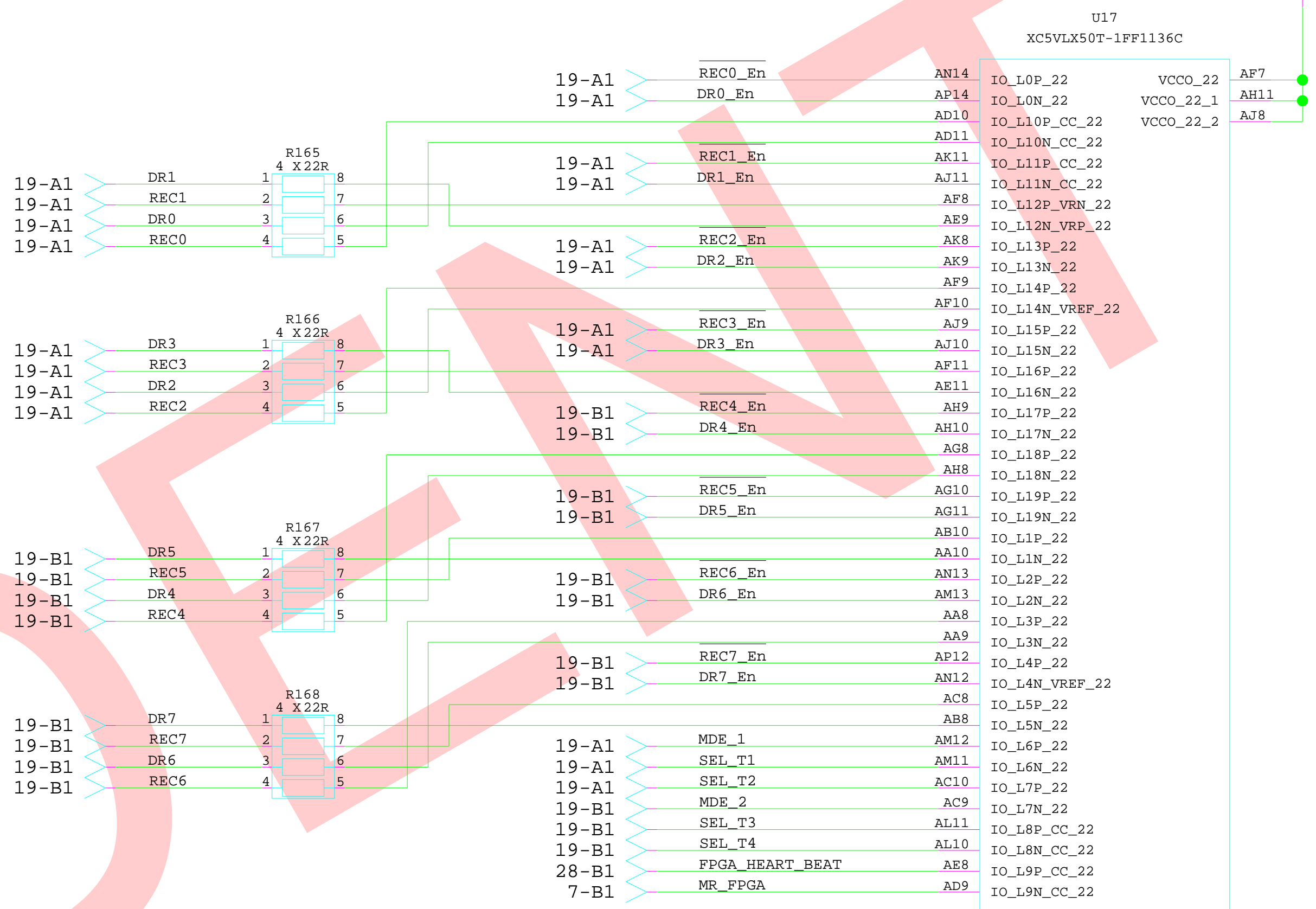
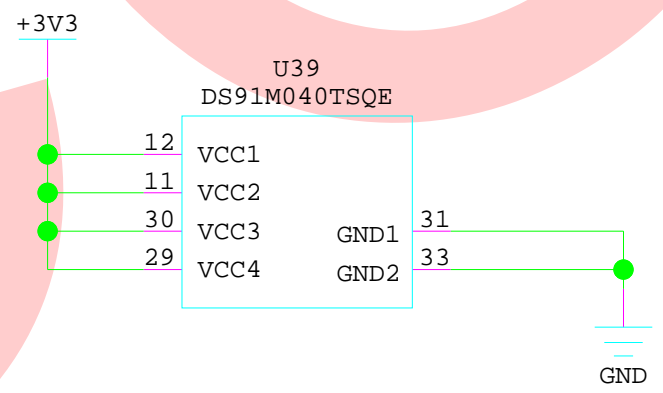
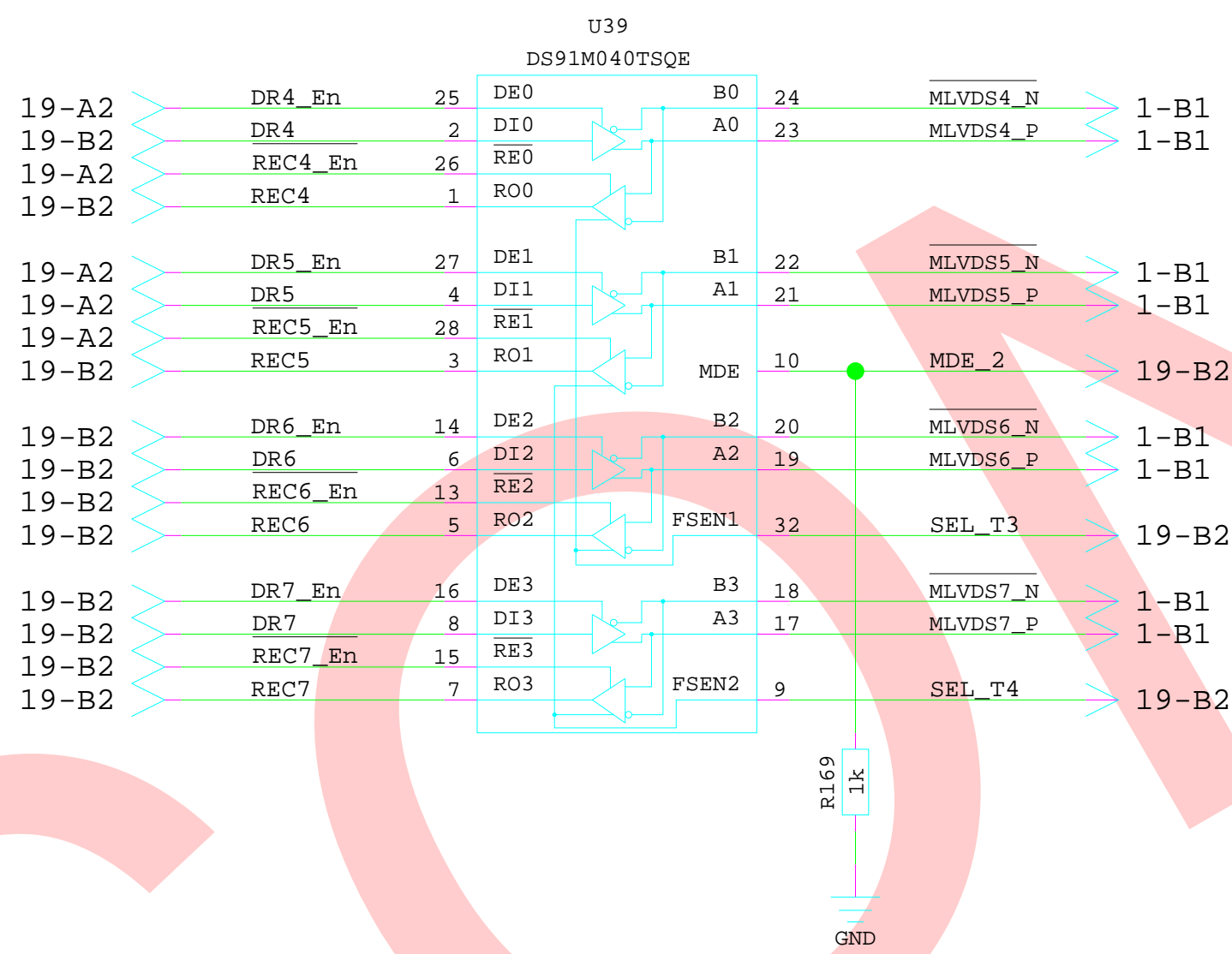
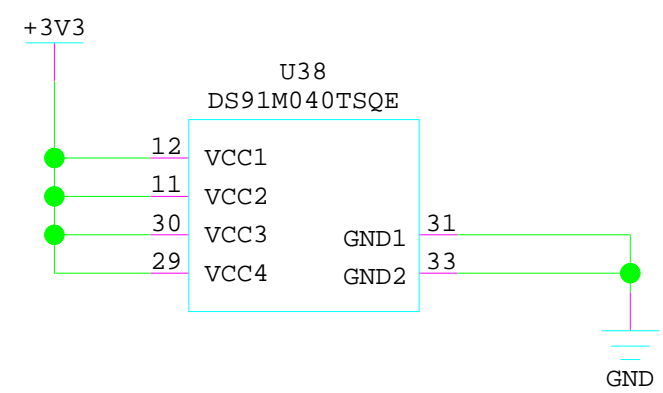
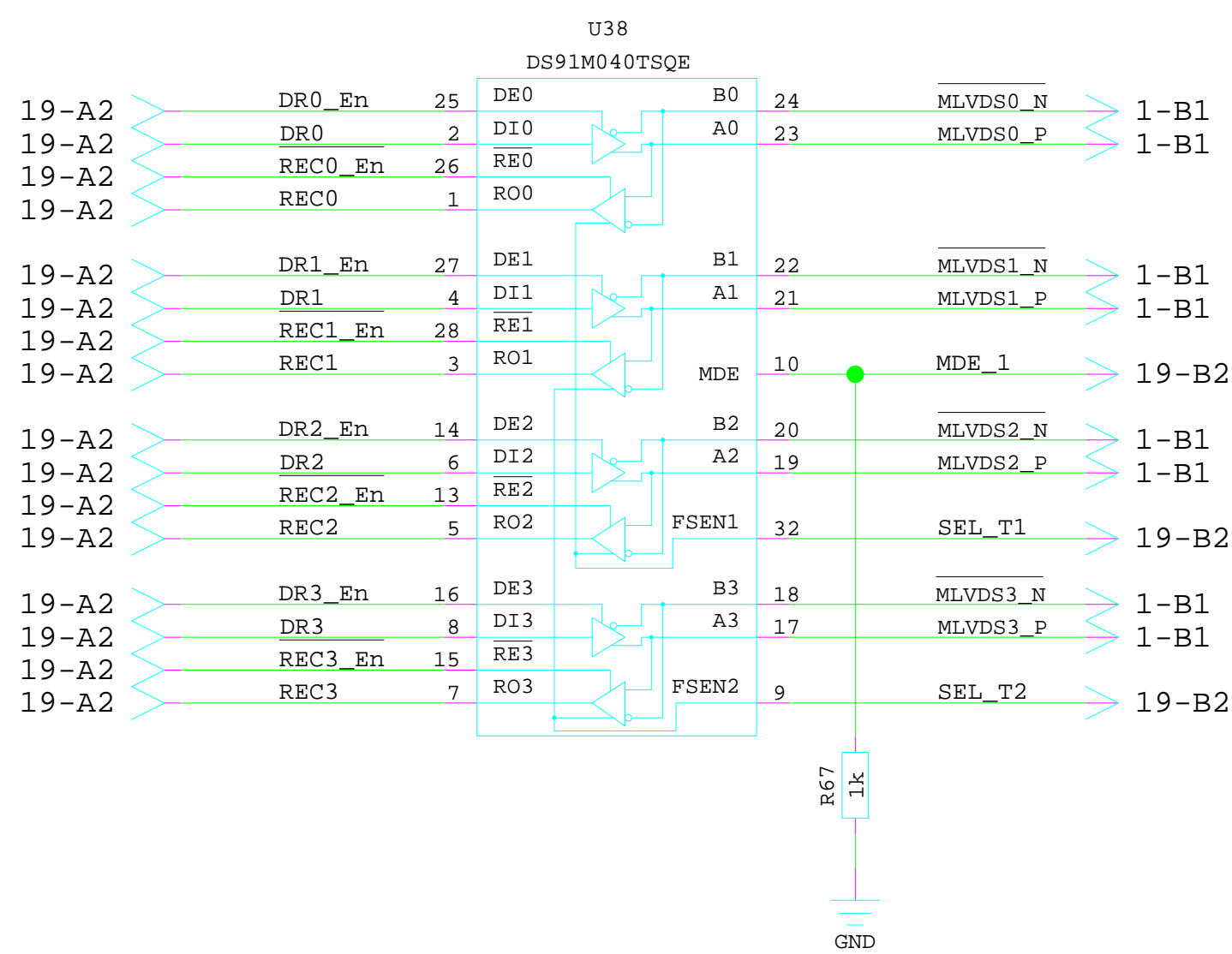
Powers for GTP and GTP_SWITCH

IT SHOUD BE 49R9 1%, 0805!!!



Developer:	Vetrov P.	ProjectFLASH Double DAMC			
		Schematic2			
Drawn by:	Vetrov P.	Sheet:			
Layouter:	Vetrov P.	DESY-FEA		Notkestrasse 85	
Changed of sch:	Vetrov P.			D-22607 Hamburg	
Date Changed:	20.8.2009	PCB No: 8423		Rev: 00	Size:A3
Date of prod. data:		PCB name:DAMC2		Sheet:19 of 29	

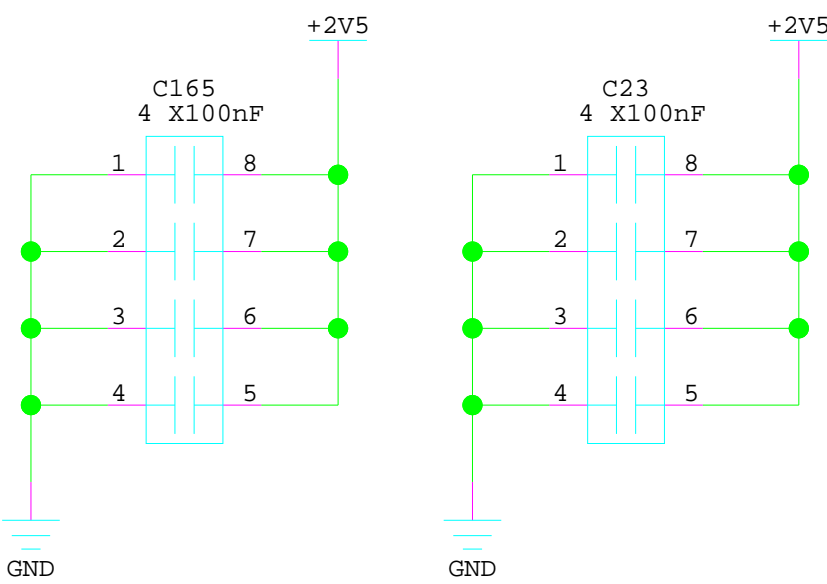
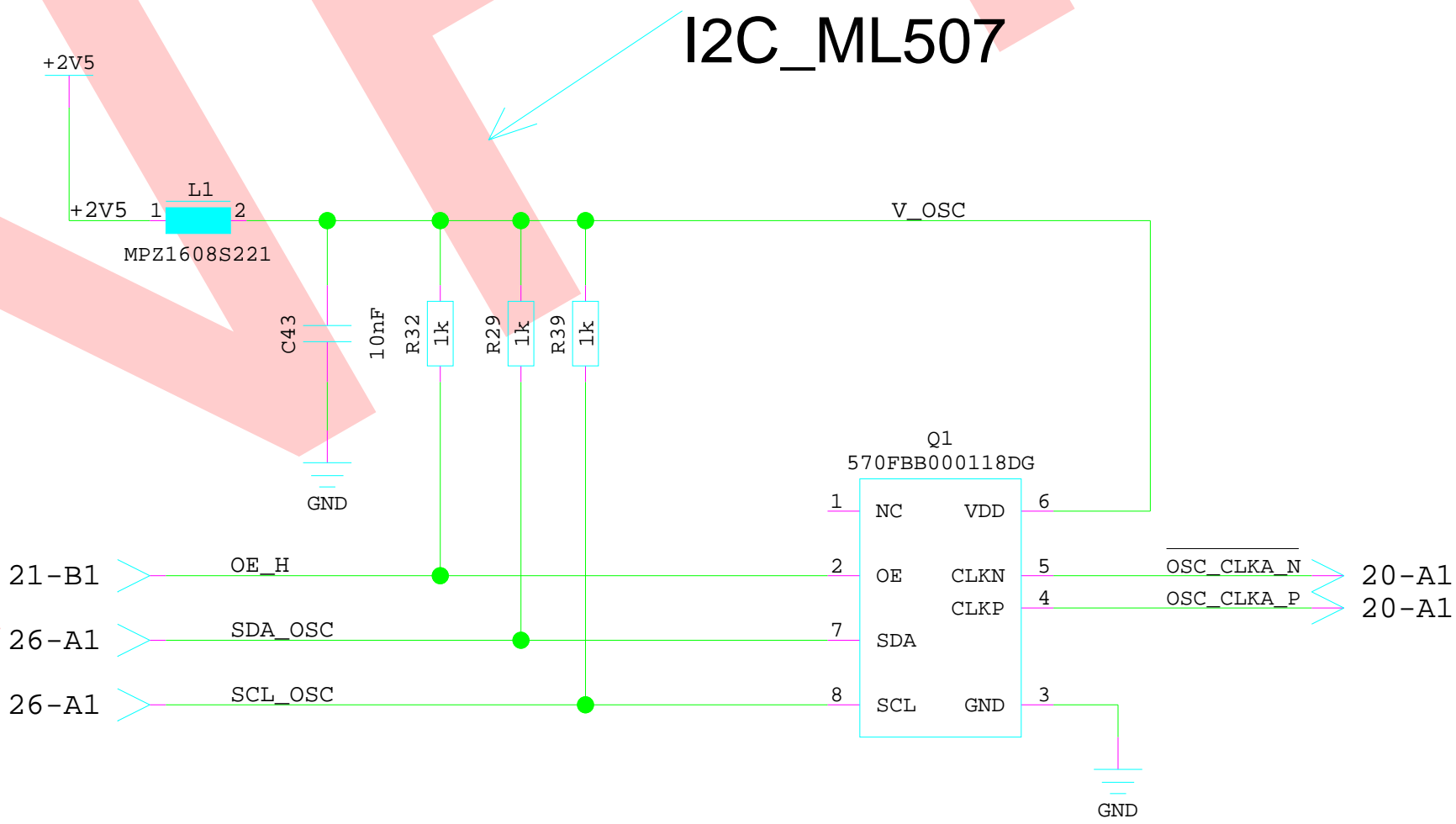
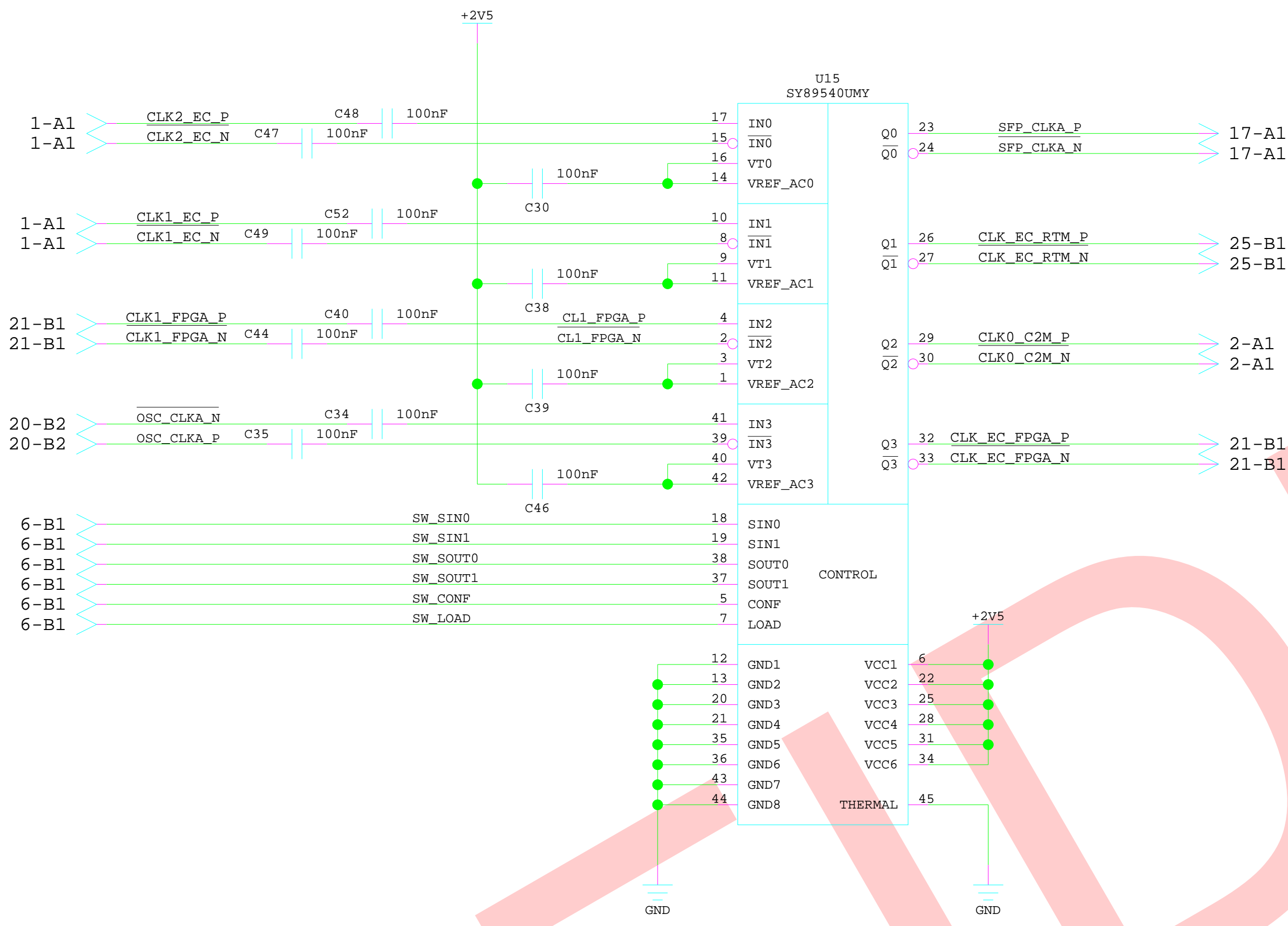
MLVDS bus to Edge Connector



Developer:	Vetrov P.	ProjectFLASH Double DAMC			
		Schematic2			
Drawn by:	Vetrov P.	Sheet:			
Layouter:	Vetrov P.	DESY-FEA Notkestrasse 85			
Changed of sch:	Vetrov P.	D-22607 Hamburg			
Date Changed:	20.8.2009	PCB No: 8423		Rev: 00	Size:A3
Date of prod. data:		PCB name:DAMC2		Sheet:20 of 29	

LOW JITTER CLOCK Crosspoint Switch

Ultra Low Jitter design: < 10 ps deterministic jitter



570FBB000118DG SMD Crystal Oscillator 156.25MHz

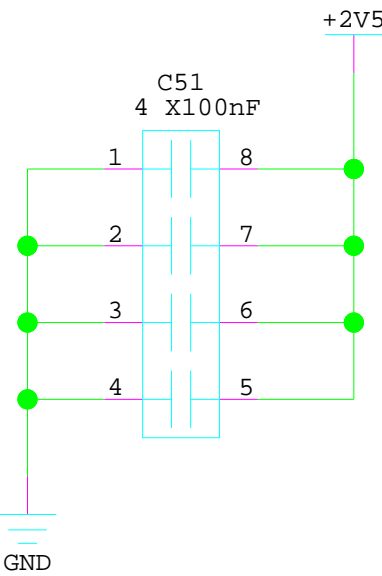
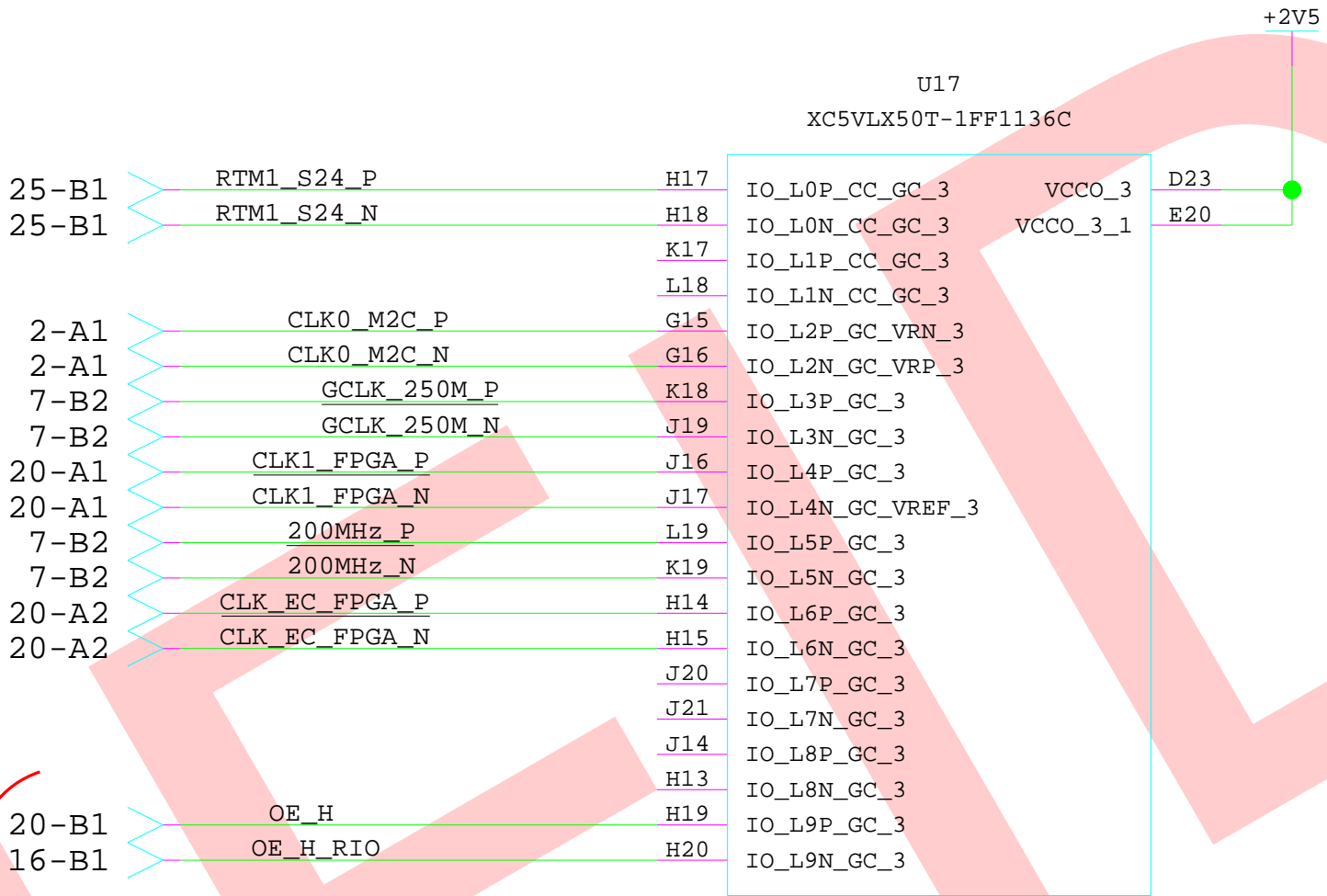
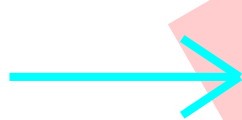
Any-rate programmable output frequencies from 10 to 945 MHz and select frequencies to 1.4 GHz

Frequency Range Supported (MHz): 10 - 810

Developer:	Vetrov P.	ProjectFLASH Double DAMC			
		Schematic2			
Drawn by:	Vetrov P.	Sheet:			
Layouter:	Vetrov P.	DESY-FEA			
Changed of sch:	Vetrov P.	Notkestrasse 85 D-22607 Hamburg			
Date Changed:	20.8.2009	PCB No: 8423		Rev: 00	Size:A3
Date of prod. data:		PCB name:DAMC2		Sheet:21 of 29	

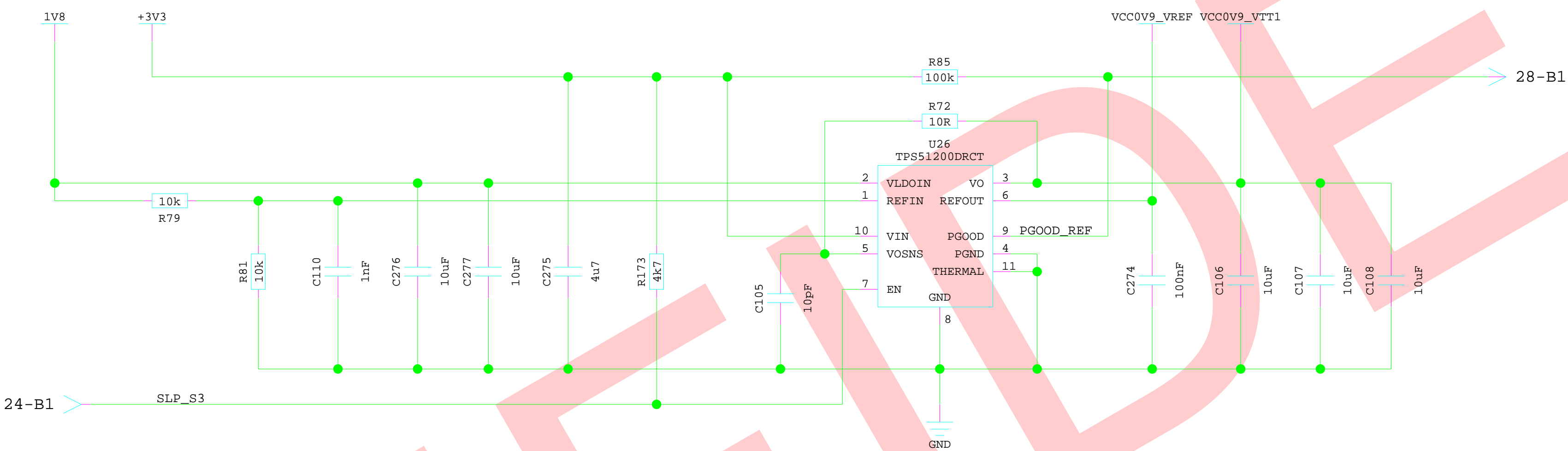
GLOBAL CLOCKS

Single ended



Developer:	Vetrov P.	ProjectFLASH Double DAMC			
		Schematic2			
Drawn by:	Vetrov P.	Sheet:			
Layouter:	Vetrov P.	DESY-FEA Notkestrasse 85			
Changed of sch:	Vetrov P.	D-22607 Hamburg			
Date Changed:	20.8.2009	PCB No: 8423		Rev: 00	Size:A3
Date of prod. data:		PCB name:DAMC2		Sheet:22 of 29	

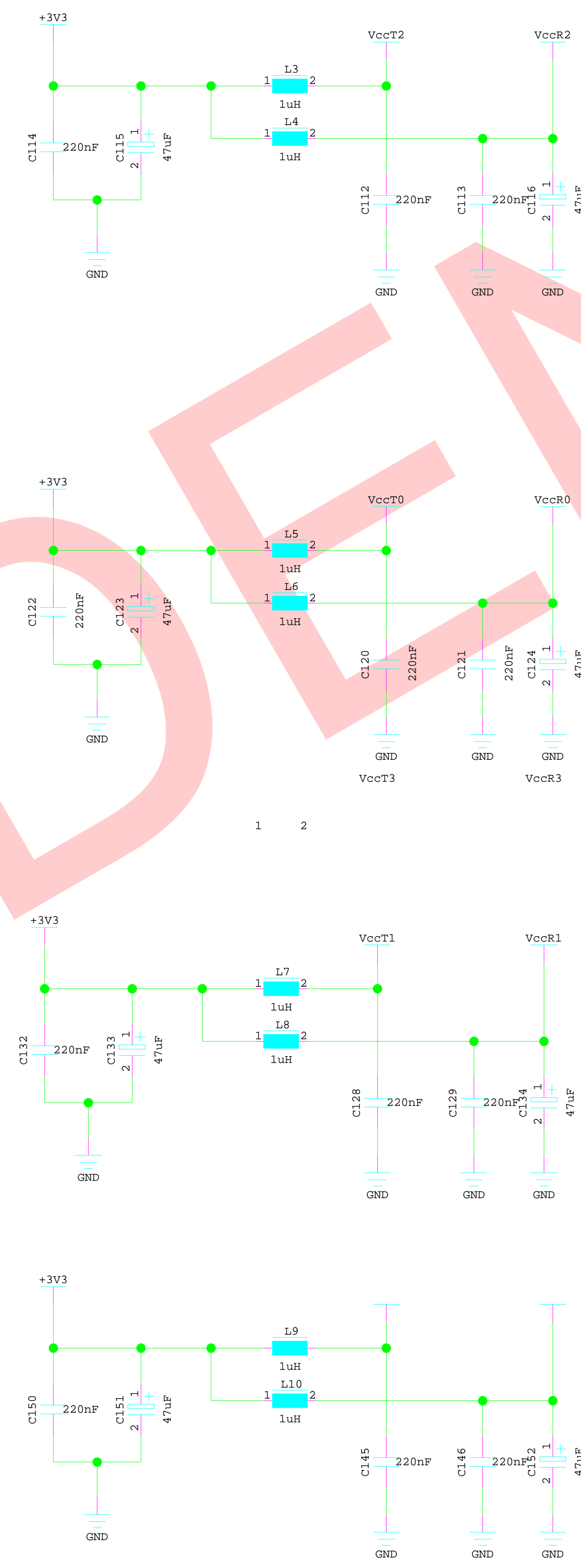
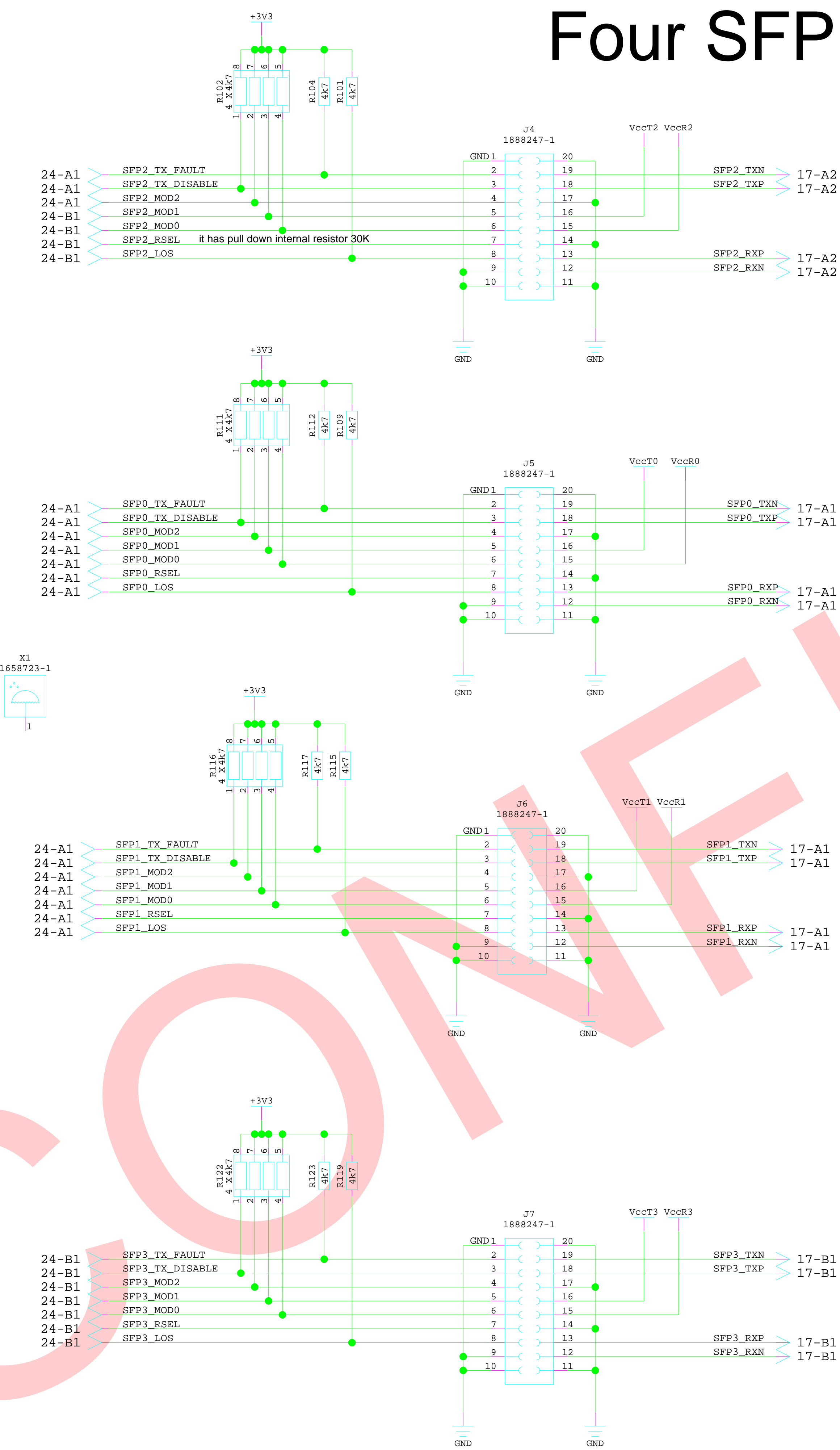
Termination Regulator for DDR2 MEMORY



ML505

Developer:	Vetrov P.	ProjectFLASH Double DAMC			
		Schematic2			
Drawn by:	Vetrov P.	Sheet:			
Layouter:	Vetrov P.	DESY-FEA Notkestrasse 85			
Changed of sch:	Vetrov P.	D-22607 Hamburg			
Date Changed:	20.8.2009	PCB No: 8423		Rev: 00	Size:A3
Date of prod. data:		PCB name:DAMC2		Sheet:23 of 29	

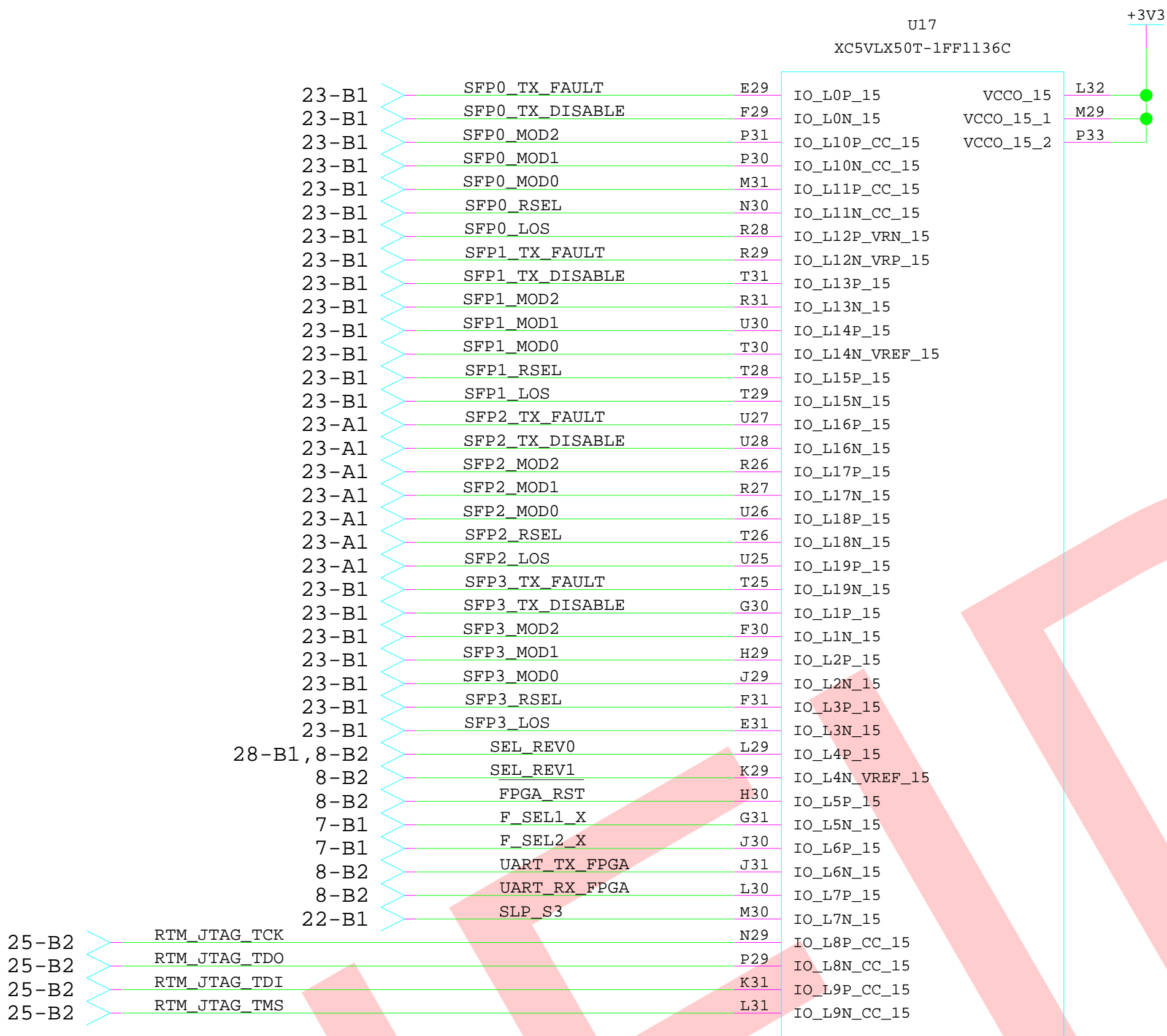
Four SFP connectors



SET 1uH BEAD 1210!!!

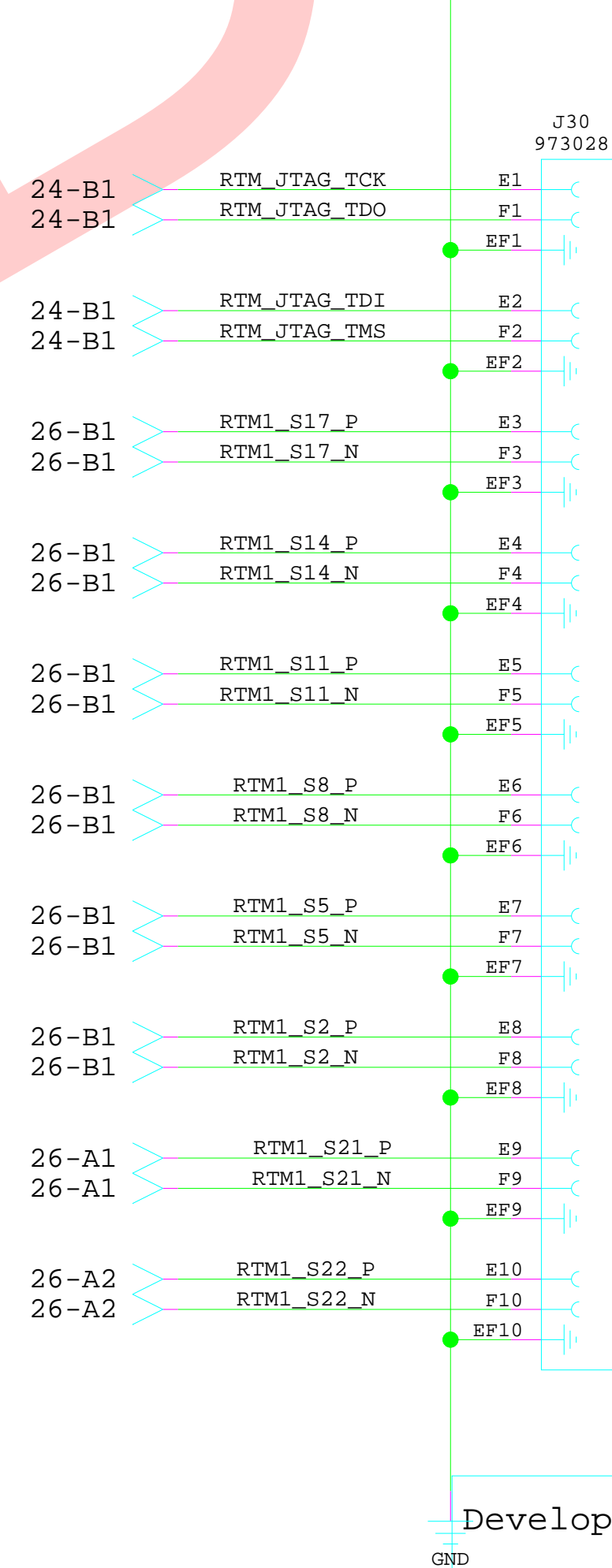
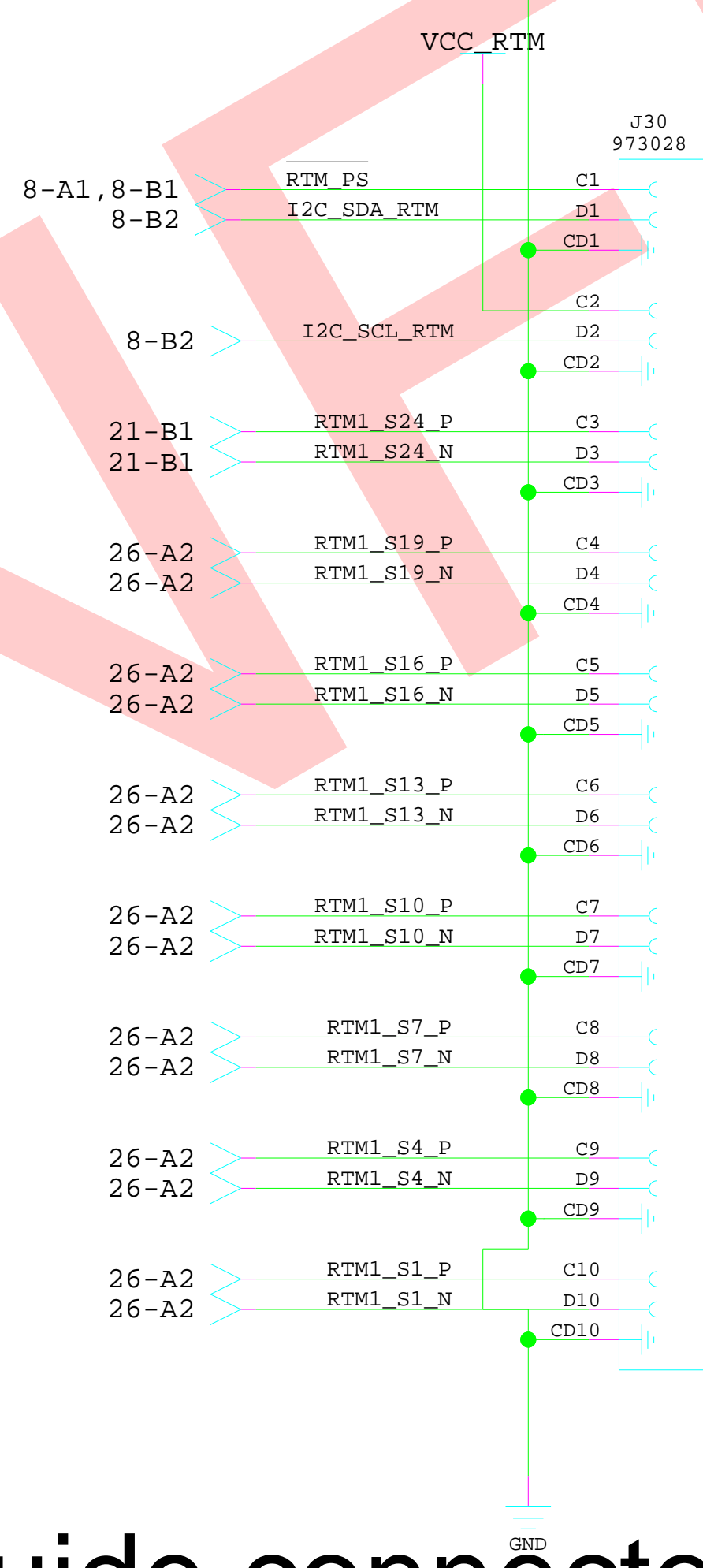
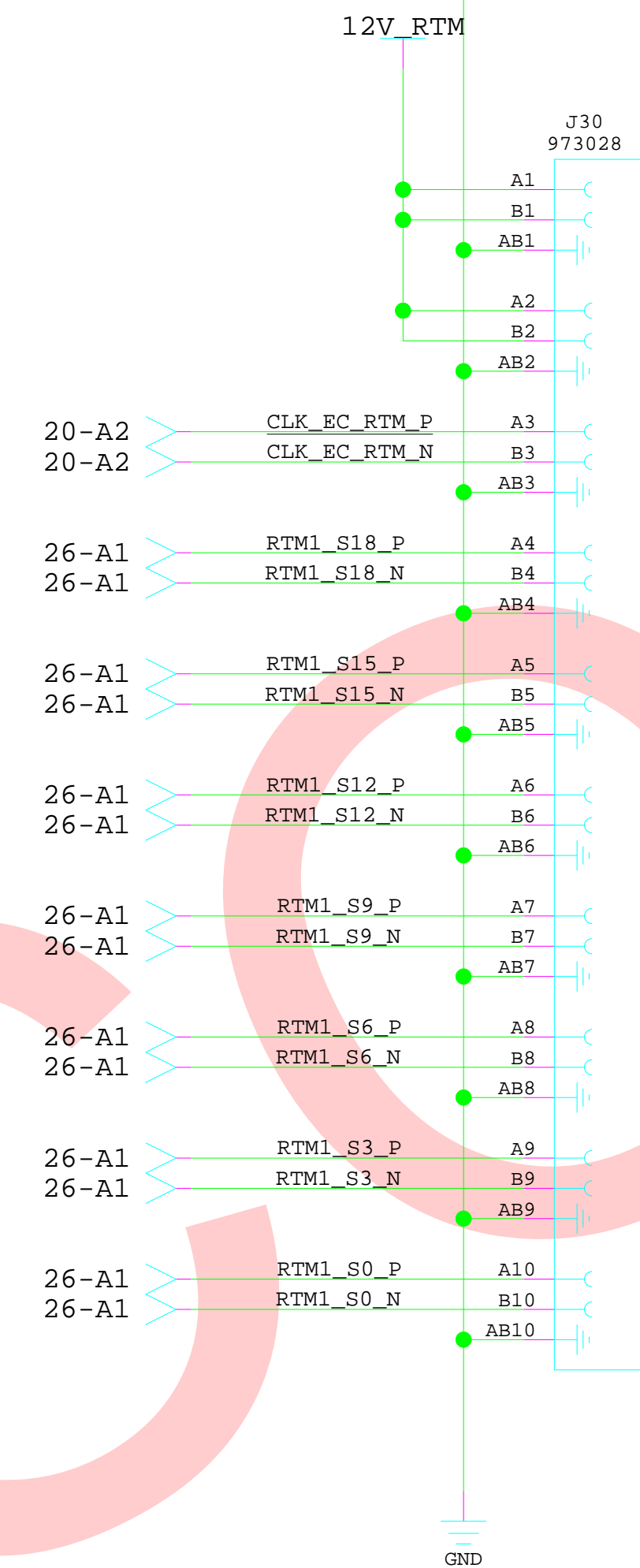
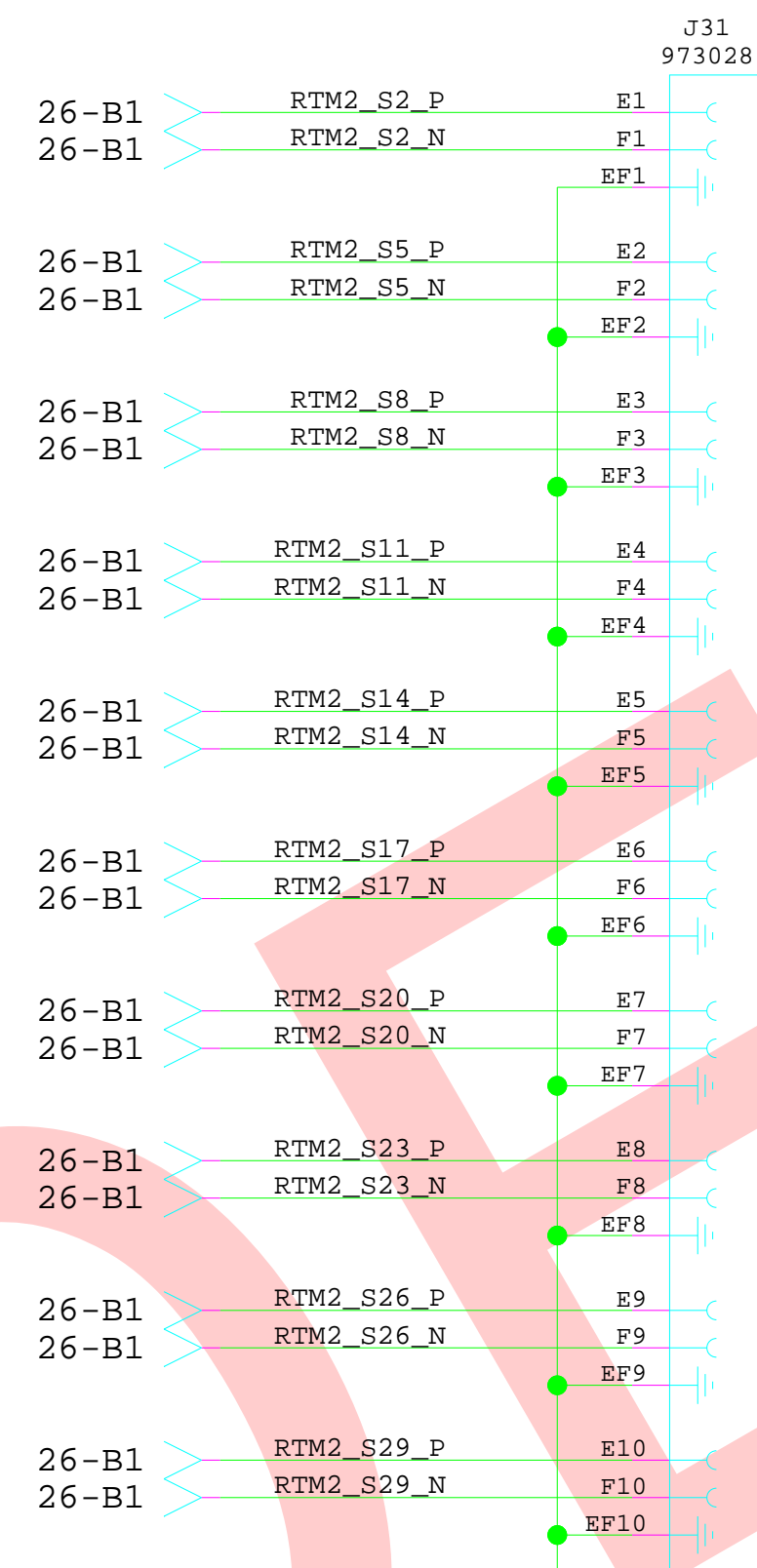
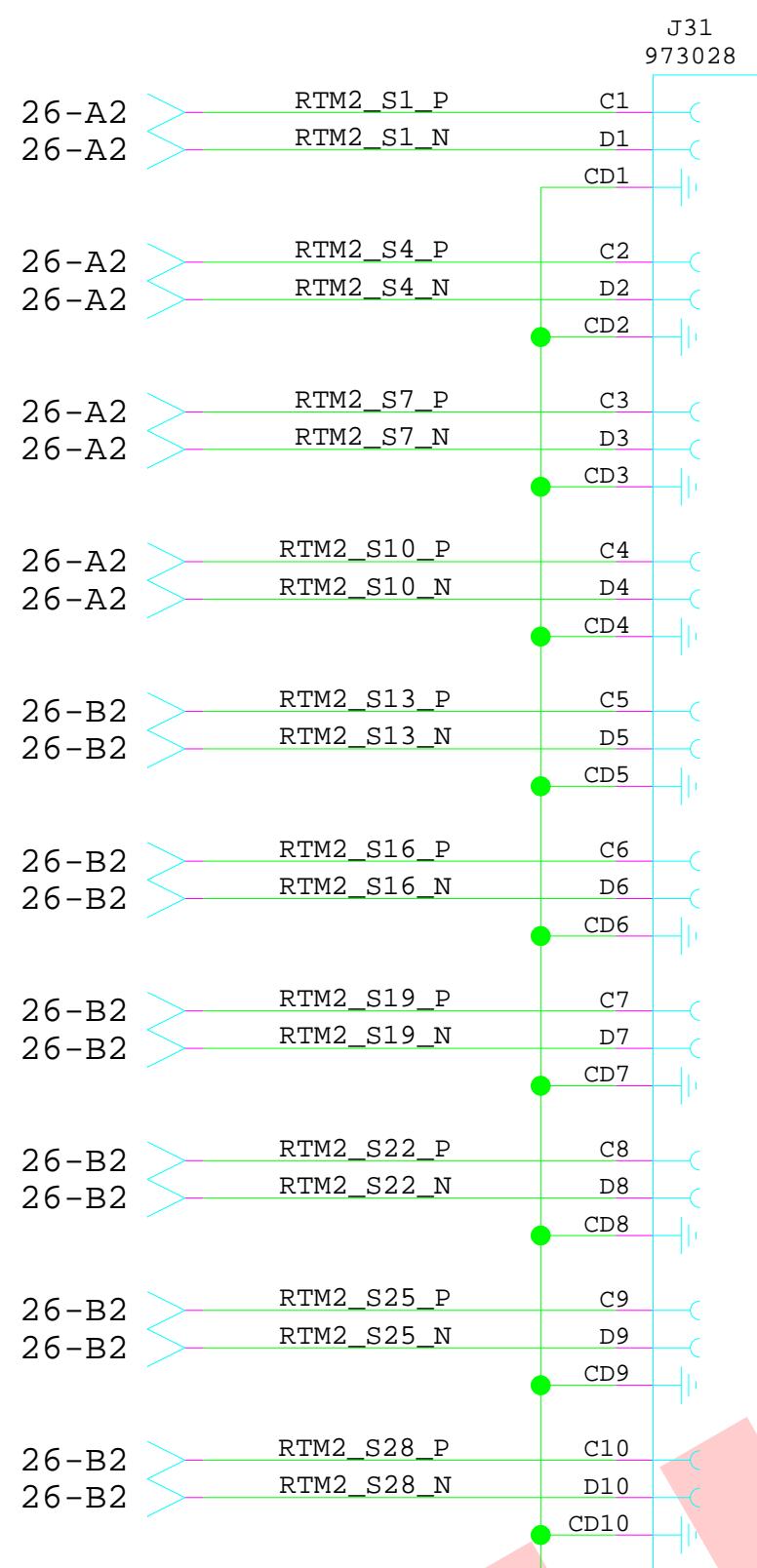
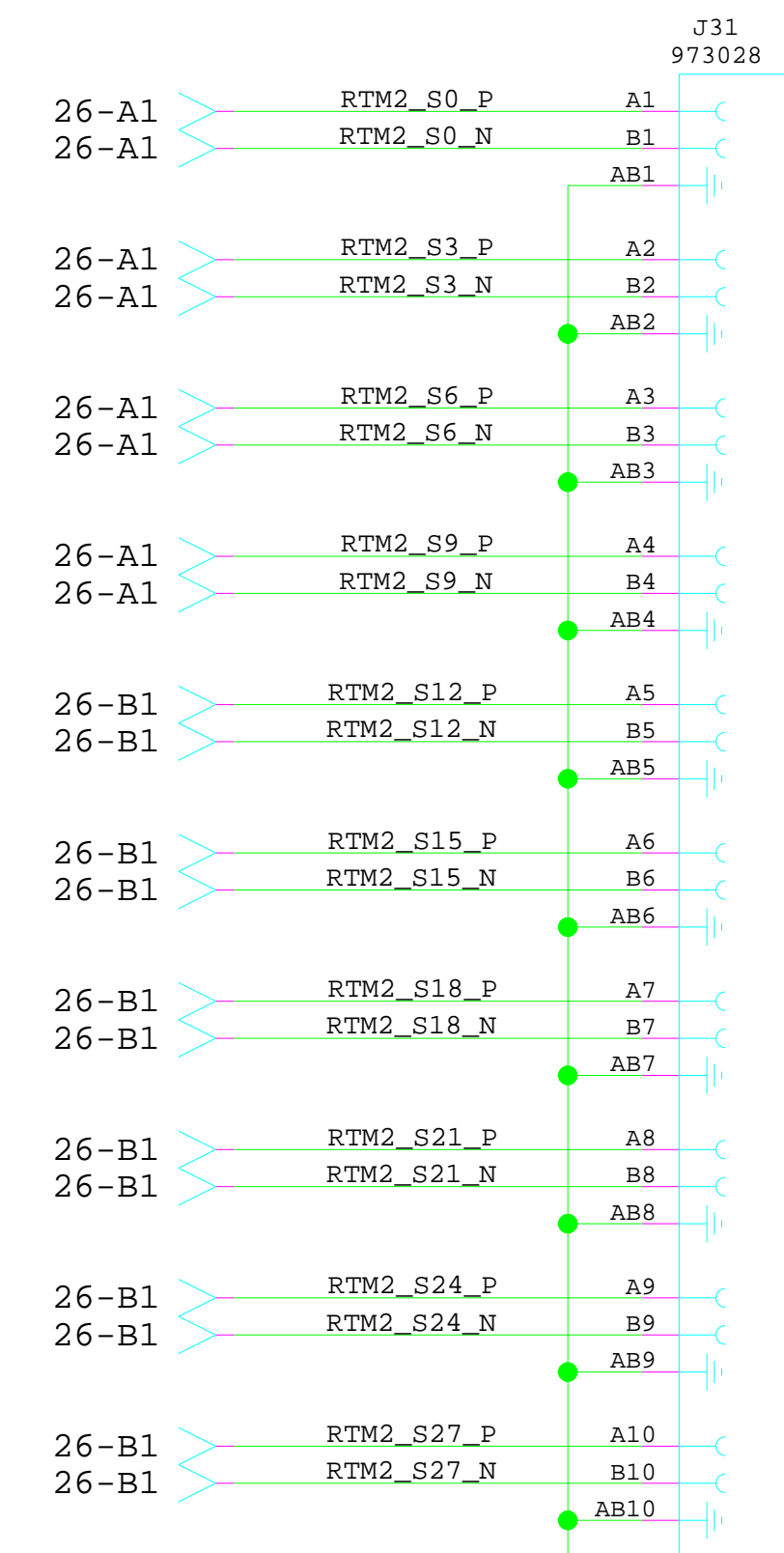
Developer:	Vetrov P.	ProjectFLASH Double DAMC			
		Schematic2			
Drawn by:	Vetrov P.	Sheet:			
Layouter:	Vetrov P.	DESY-FEA			
Changed of sch:	Vetrov P.	Notkestrasse 85 D-22607 Hamburg			
Date Changed:	20.8.2009	PCB No: 8423		Rev: 00	Size:A3
Date of prod. data:		PCB name:DAMC2		Sheet:24 of 29	

SFP CONTROLLER



Developer:	Vetrov P.	ProjectFLASH Double DAMC			
		Schematic2			
Drawn by:	Vetrov P.	Sheet:			
Layouter:	Vetrov P.	DESY-FEA Notkestrasse 85			
Changed of sch:	Vetrov P.	D-22607 Hamburg			
Date Changed:	20.8.2009	PCB No: 8423	Rev: 00	Size:A3	
Date of prod. data:		PCB name:DAMC2	Sheet:25	of 29	

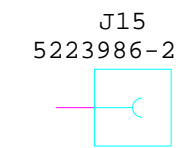
Two connectors to RTM, 3 Amp/12V



Top connector

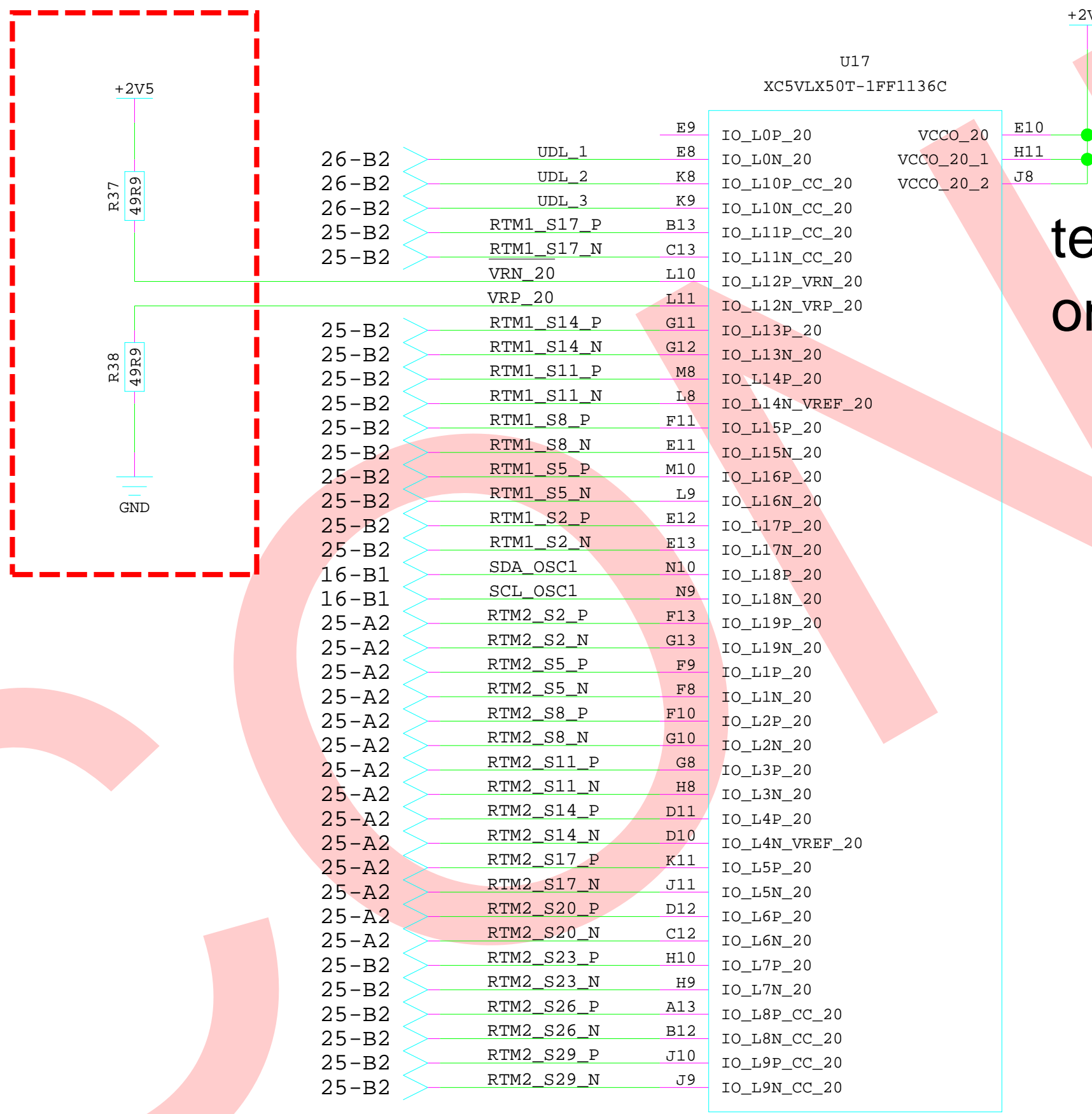
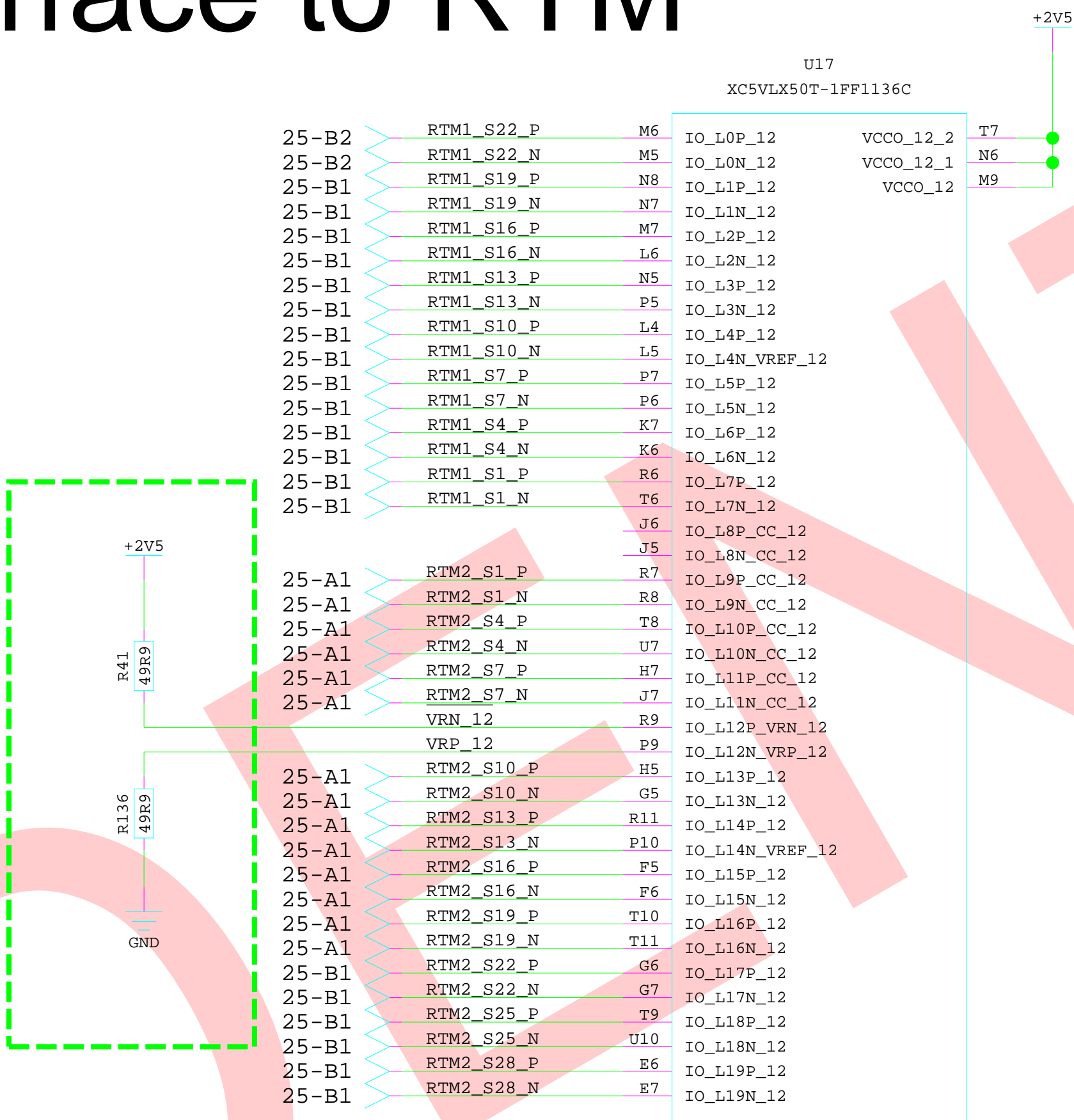
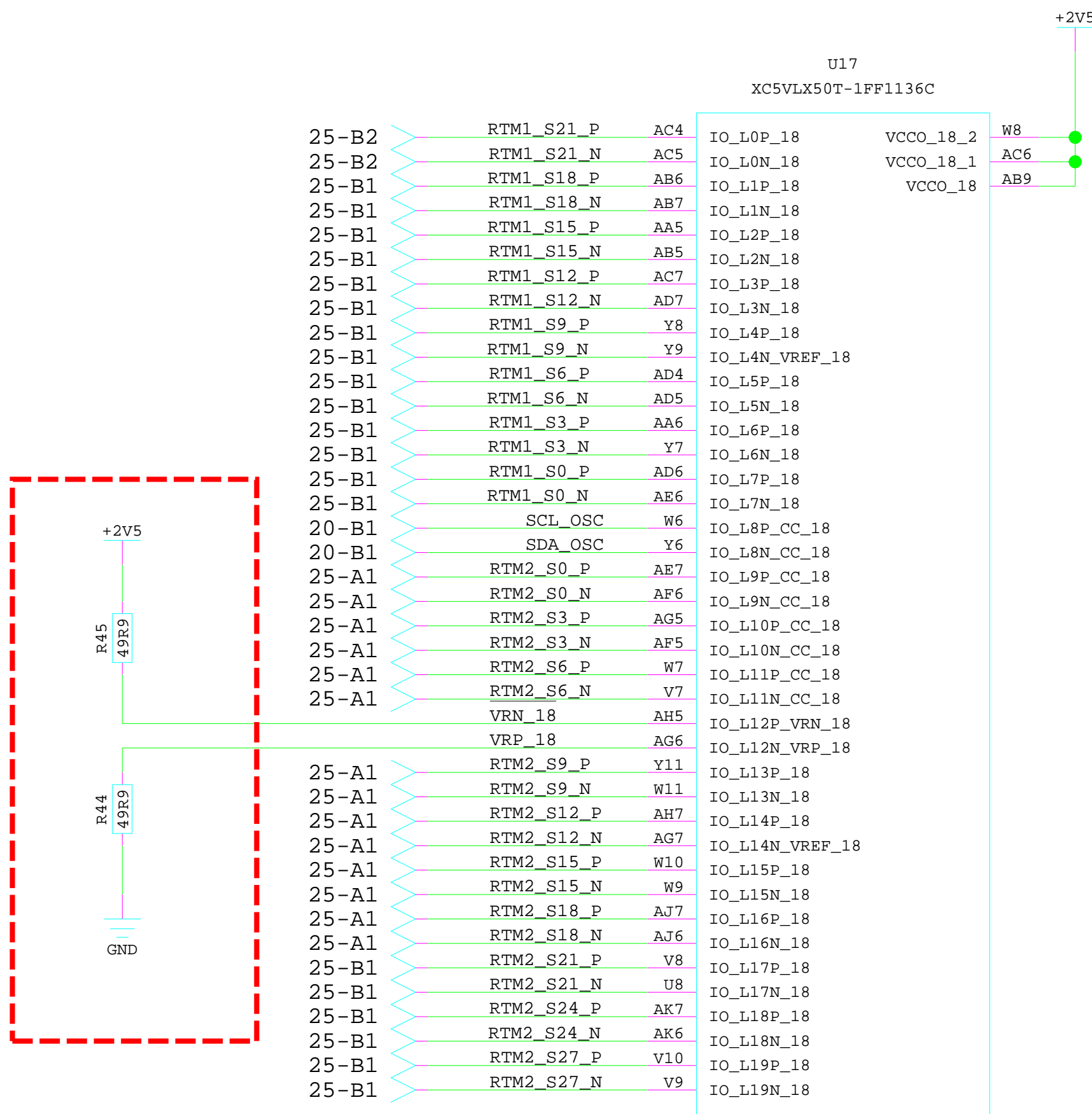
Bottom connector

Guide connector



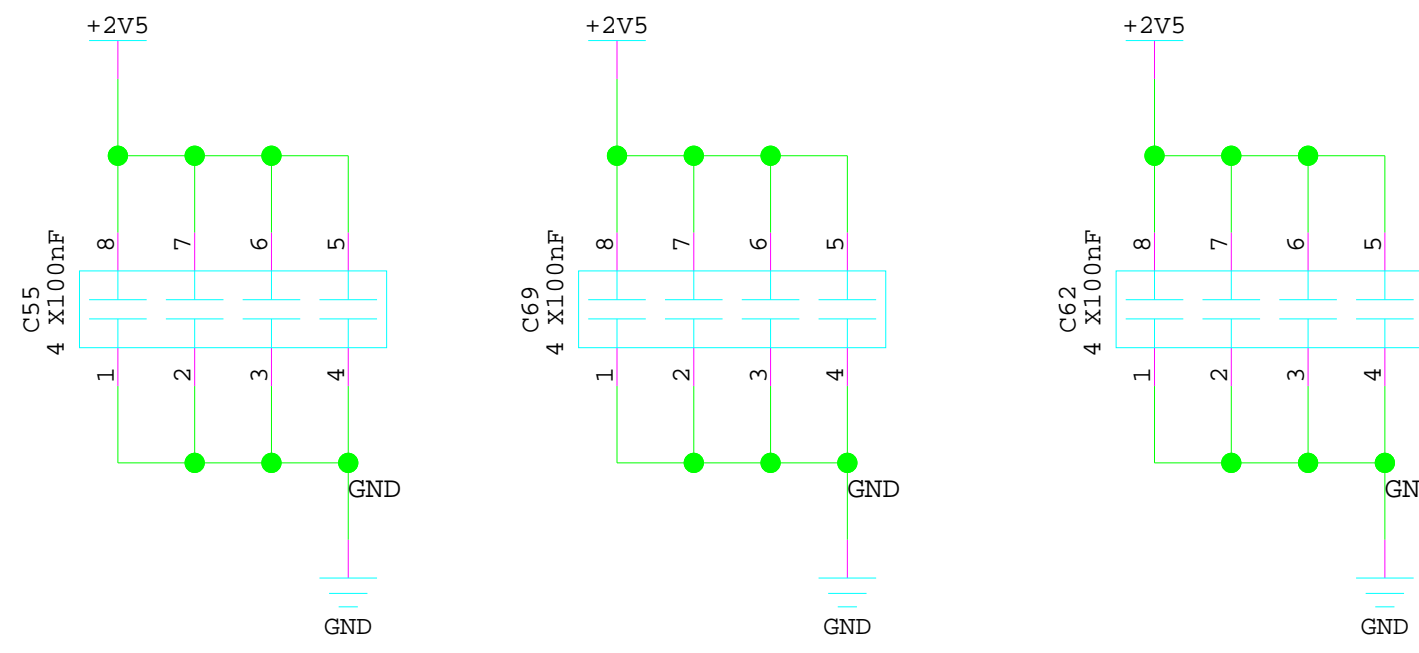
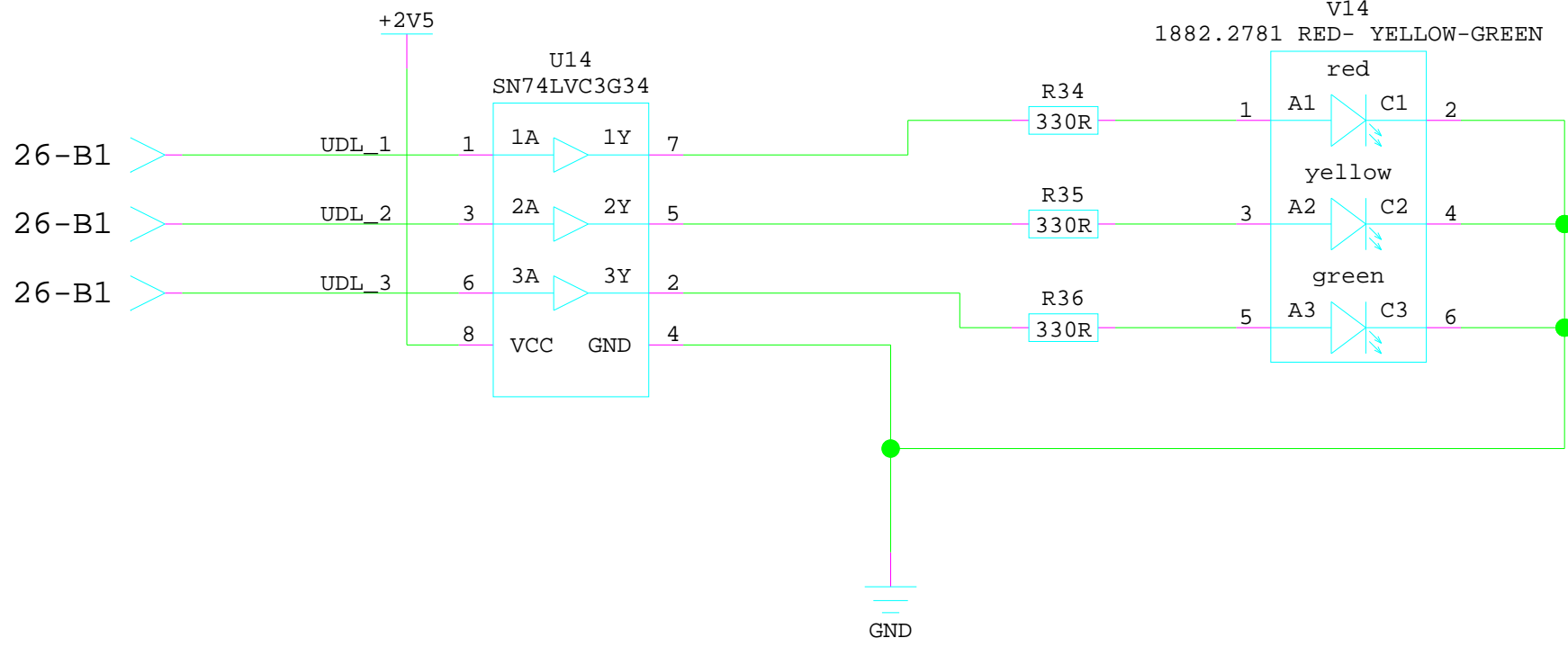
Developer:	Vetrov P.	ProjectFLASH Double DAMC			
Drawn by:	Vetrov P.	Schematic2			
Layouter:	Vetrov P.	Sheet:			
Changed of sch:	Vetrov P.	DESY-FEA	Notkestrasse 85 D-22607 Hamburg		
Date Changed:	20.8.2009	PCB No: 8423	Rev: 00	Size:A3	
Date of prod. data:		PCB name:DAMC2	Sheet:26 of 29		

2V5 Interface to RTM



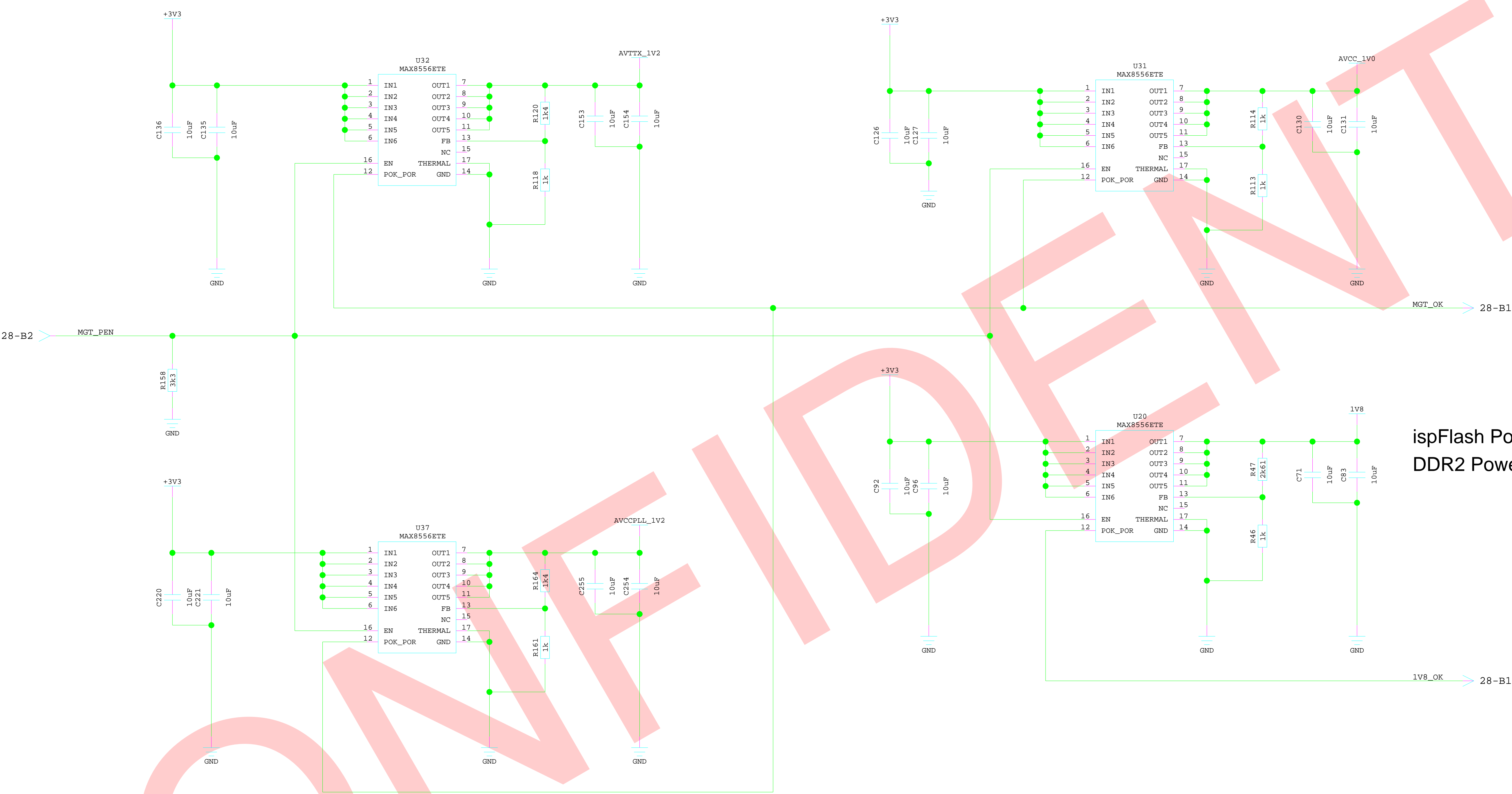
termination banks 12,18, 20!
only one pair of Ref. Resistors can be used for

USER DEFINED LEDs



Developer:	Vetrov P.	ProjectFLASH Double DAMC			
Drawn by:	Vetrov P.	Schematic2			
Layouter:	Vetrov P.	Sheet:			
Changed of sch:	Vetrov P.	DESY-FEA			
Date Changed:	20.8.2009	Notkestrasse 85		D-22607 Hamburg	
Date of prod. data:		PCB No: 8423		Rev: 00	Size:A3
		PCB name:DAMC2		Sheet:27 of 29	

Power for GTP, DDR2 and ispFlash



ispFlash Power,
DDR2 Power

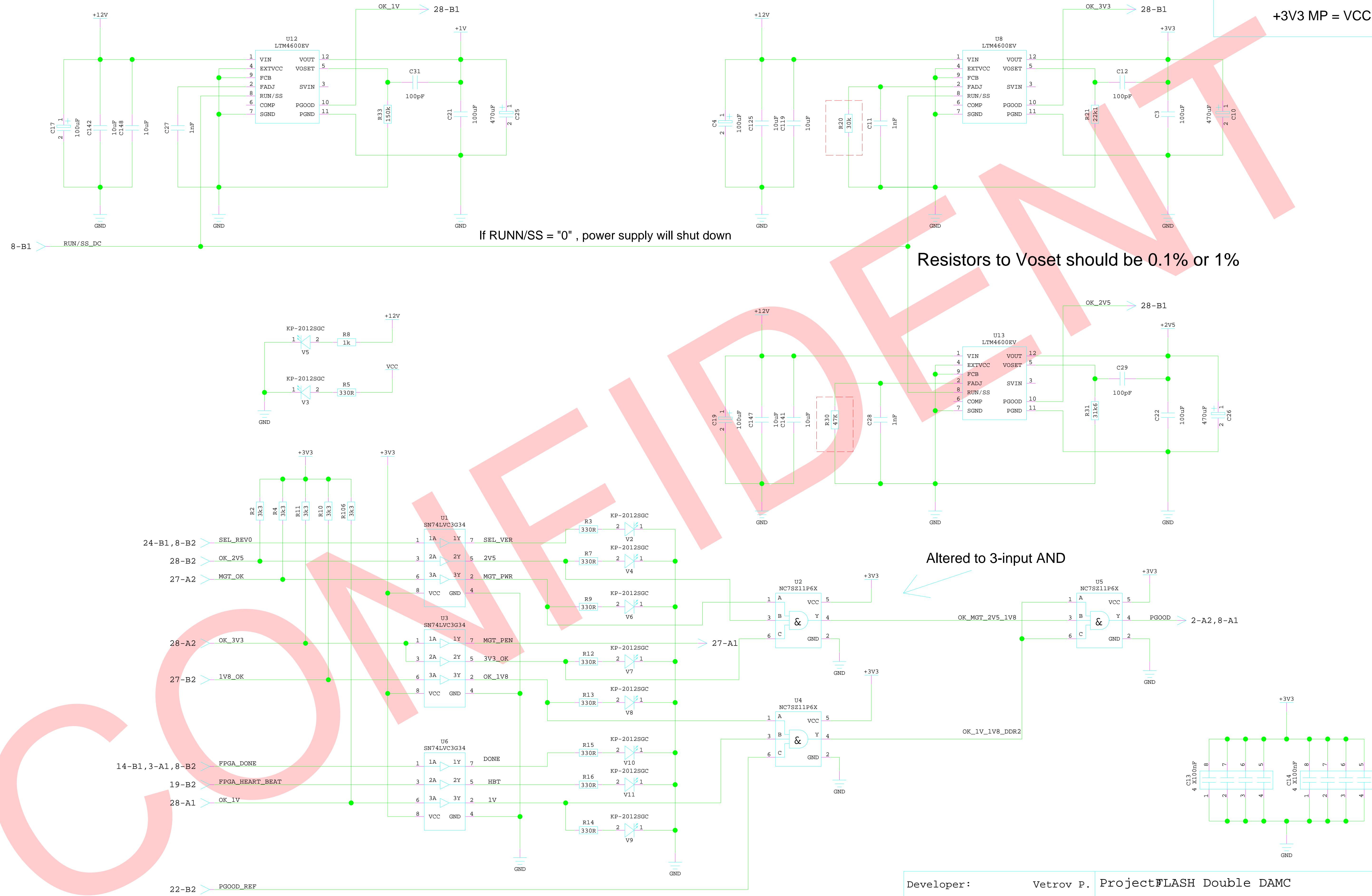
MAXIMUM Dropout Voltage is 0.1V if current is 4Ampers
Start-up voltage rampe to VDD no longer than 500us

Developer:	Vetrov P.	ProjectFLASH Double DAMC Schematic2			
Drawn by:	Vetrov P.	Sheet:			
Layouter:	Vetrov P.	DESY-FEA Notkestrasse 85 D-22607 Hamburg			
Changed of sch:	Vetrov P.				
Date Changed:	20.8.2009	PCB No: 8423		Rev: 00	Size:A3
Date of prod. data:		PCB name:DAMC2		Sheet:28 of 29	

Main Power for DAMC+FMC+uRTM

+3V3_Payload = +3V3

+3V3 MP = VCC



If RUNN/SS = "0" , power supply will shut down

Resistors to Vosest should be 0.1% or 1%

Altered to 3-input AND

Developer:	Vetrov P.	ProjectFLASH Double DAMC			
		Schematic2			
Drawn by:	Vetrov P.	Sheet:			
Layouter:	Vetrov P.	DESY-FEA		Notkestrasse 85	
Changed of sch:	Vetrov P.			D-22607 Hamburg	
Date Changed:	20.8.2009	PCB No: 8423		Rev: 00	Size:A3
Date of prod. data:		PCB name:DAMC2		Sheet:29 of 29	