

# CC RTM JITTER REPORT

UCL XFEL Team

## *INTRODUCTION*

The clock and control RTM has a requirement of “low jitter” for the 99 MHz clock it sends to the FEE units. Initial measurements [1] suggested that the jitter on the 99 MHz is “relatively high” and the cause of it is the DC/DC converter on-board which provides the 3.3 V power rail to all the chips related to the FEM clock and data transmission. This report aims to summarise the current jitter situation in a systematic way and presents the modifications to the power design of the RTM and the corresponding improvements in the jitter metric. By this way a more detailed understanding of the effect of the power topology on the jitter is obtained. Additionally, in light of these measurements, proposals for the power topology for the next design iteration of the CC RTM are presented as conclusions.

## *MEASUREMENT SET-UP*

The 99 MHz clock is observed at the RTM's final output to the FEEs, more specifically at the first output of the 1:16 LVDS fanout buffer chip on-board. An 800 MHz bandwidth active differential probe (PICO Technology) is attached to the test points TP2 and TP4 to get the clock waveform. The particular FEE channel that the observed clock belongs to is terminated on the other end of a 15m CAT6 cable in order to achieve the LVDS signal. The jitter measurements were taken on the Agilent MSO scope by using Agilent supplied jitter analysis software, EZJIT. Figure 1 shows the experiment setup.

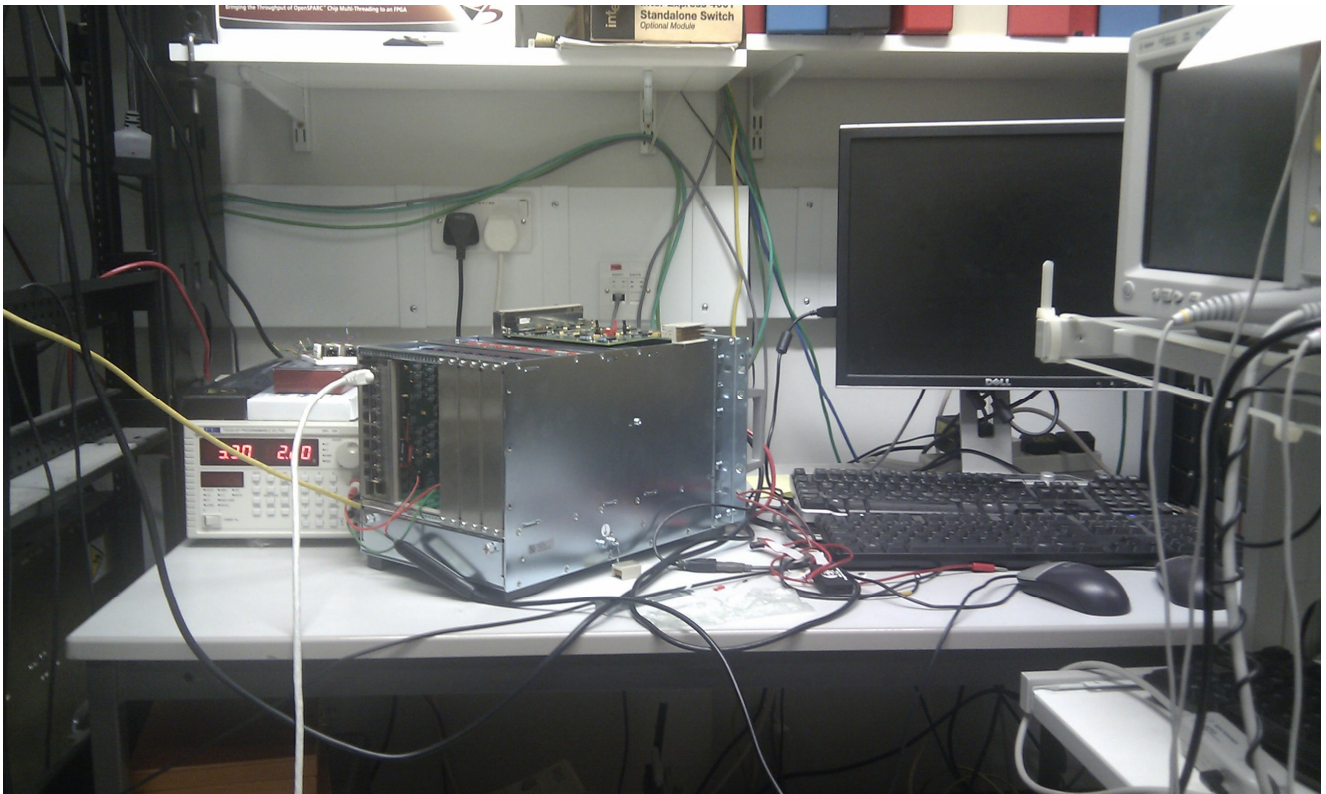


Figure 1: The experiment setup

The clock that is measured in terms of jitter performance is the on-board generated 99 MHz clock not the multiplied backplane clock coming from the timing receiver. The previous results [1] suggest the jitter performance for this clock is a bit worse than the backplane clock as the clock crystal is also affected by the various jitter generating mechanisms on the CC RTM. Therefore, we think this analysis

is valid as it measures the “worst case”.

## ***TYPES OF JITTER MEASURED***

1. **Time Interval Error (TIE):** TIE, also called the **phase jitter**, is defined as the phase difference between the signal being measured and the reference clock. EZJIT's analysis is based on variations of time-displacement of voltage transitions (in our case the rising edge of the clock) of the clock waveform relative to the ideal reference waveform. The time reference (clock reference) used for TIE measurements can be defined many different ways. One time reference commonly used for TIE measurements is a constant-frequency square wave with frequency and phase that is the best-fit to the measurement's source waveform. The scope determines the ideal frequency by measuring the frequencies of all the cycles in the waveform and taking the average.
2. **Period:** The period measurement is defined as the time between the middle threshold crossings of two consecutive, same polarity edges, which in our case are the rising edges of the clock.
3. **Cycle to cycle:** The cycle-to-cycle jitter measurement measures the period of the first cycle of the waveform and subtracts it from the period of the second cycle of the waveform for the first measurement result. Then, the second cycle is measured and subtracted from the third for the second measurement result. This operation continues until all of the cycles of the waveform have been measured. All of the measurement results are used to compute the statistics, which are the values accumulated over all of the trigger cycles that have occurred.
4. **Cycle to cycle – Duty Cycle:** This jitter measurement is done as in the cycle-to-cycle case this time calculating the duty cycle as the ratio of the positive pulse to the whole period multiplied by 100.

## ***THE DISPLAY OF JITTER***

The jitter display screen is divided up into 3 parts. In the top part the clock waveform is displayed. The middle part presents the histogram of the jitter, with the horizontal axis the jitter values and the vertical axis the number of readings at the particular jitter value. The third part contains the jitter spectrum with the horizontal axis the frequency and the vertical axis the jitter value at a particular frequency in picoseconds. For the TIE jitter measurements the spectrum is scaled such that each horizontal division corresponds to 500 KHz and each vertical corresponds to 125 ps. In the measurements below statistics about the histogram is presented. The standard deviation of the histogram graph corresponds to the RMS jitter. Additionally peak-to-peak value of the jitter is also presented. The shape of the histogram graph gives clues about the nature of the jitter. A Gaussian shape corresponds to a mostly random jitter behaviour where as a non-Gaussian shape with clearly visible peaks implies the presence of high deterministic jitter, which results from effects such as power rail noise, cross-talk and other possible interference.

## ***EXPERIMENTS***

1. **RTM card with LTM4600EV DC-DC converter :** This experiment demonstrates the jitter measurements on the 99 MHz clock generated by the CC RTM in its currently produced form with some extra capacitors added. As can be seen in the appendix this change does not affect the jitter measurement too much (there is a slight improvement), therefore we can say that this is representative of the current version of the RTM.

Figure 2 shows the jitter measurement display for the TIE. The histogram plot has two distant peaks which is a sign of heavy deterministic jitter. The standard deviation is 426.838 ps which is in accordance with the phase jitter presented in [1] for the same type of card. The jitter spectrum shows the frequencies that contribute to the jitter. There is a high peak at around ~780 KHz and a smaller one at the double of that frequency. This corresponds to the switching frequency of the DC-DC converter.

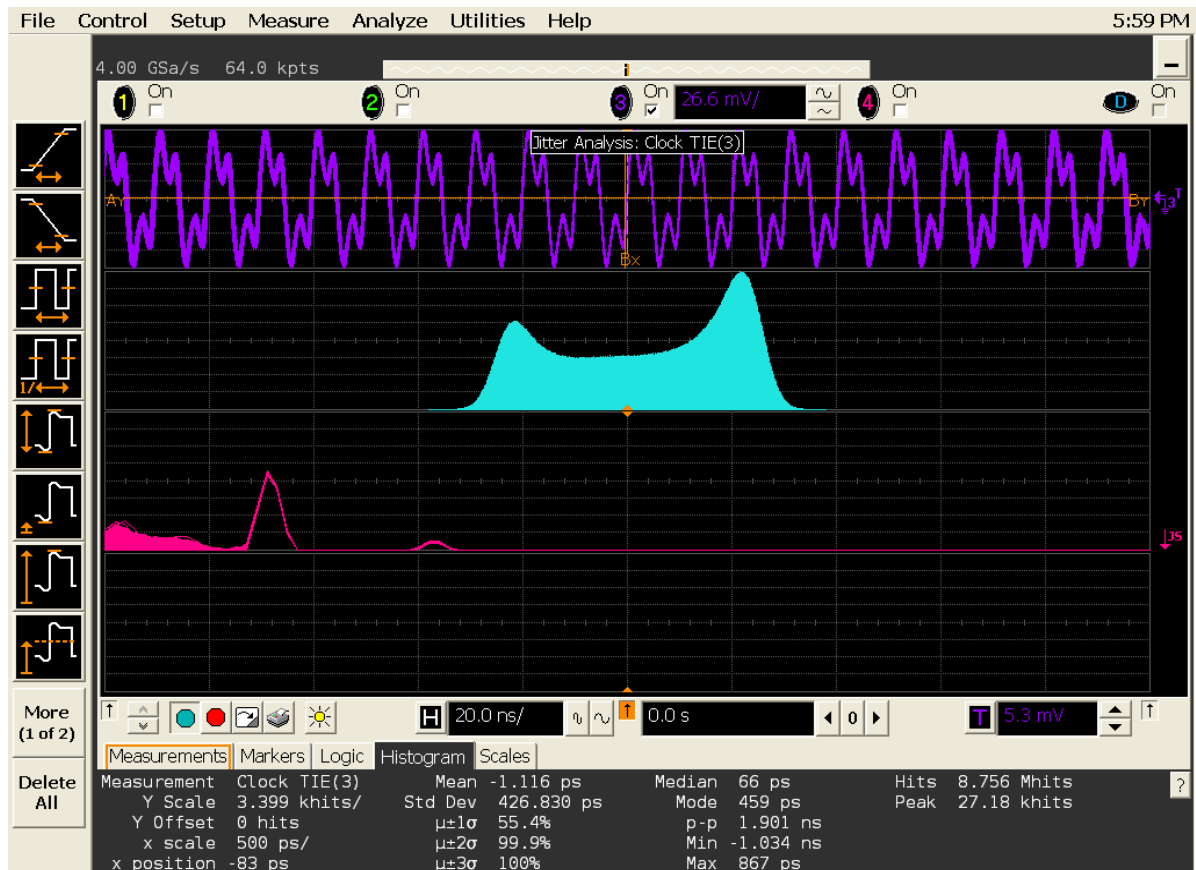


Figure 2: The TIE display for the RTM with LTM4600EV DC-DC converter

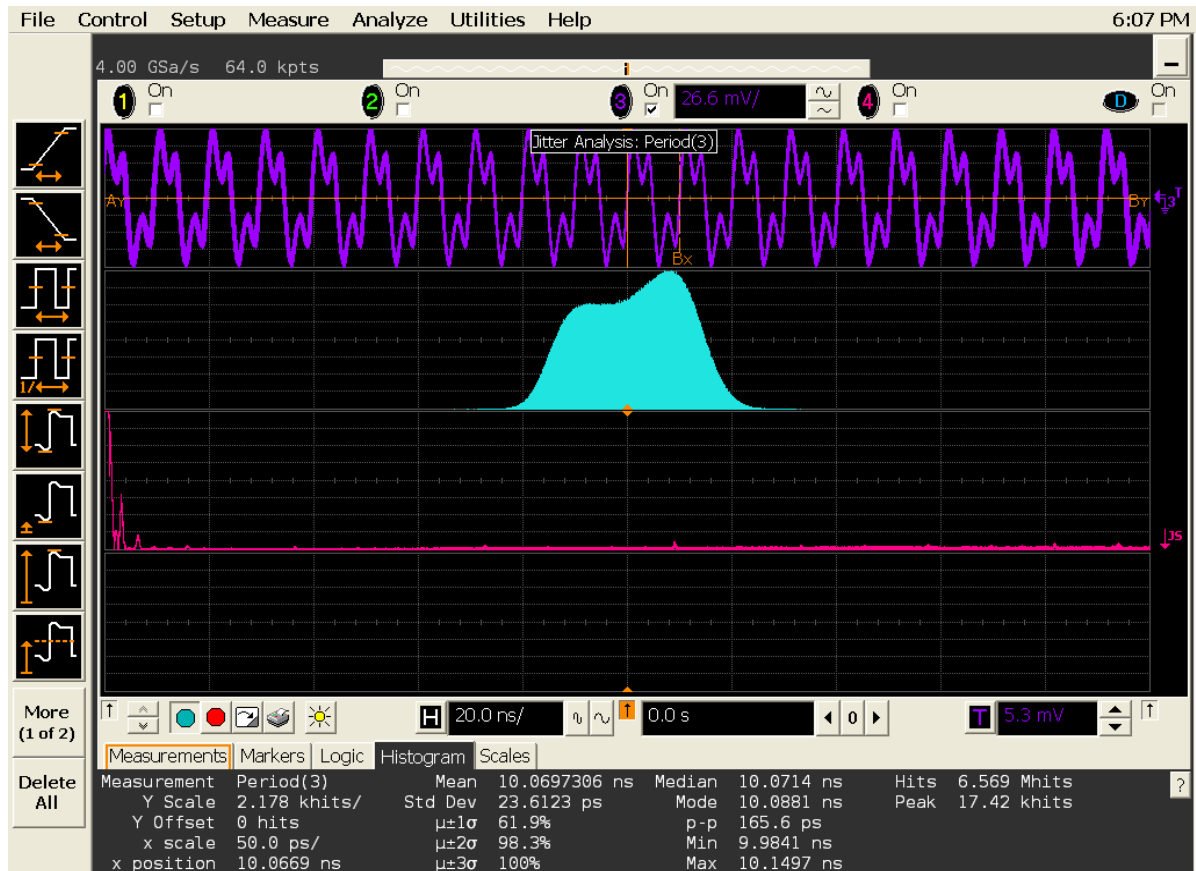


Figure 3: The period jitter display for the RTM with LTM4600EV DC-DC converter

Figure 3 shows the period jitter display. As can be seen from the histogram the shape is a distorted Gaussian which is in accordance with the TIE results. However, the period jitter value is much less as can be seen from the standard deviation figure. The spectrum of jitter is not scaled to 500 KHz per division on the horizontal axis (5 MHz per division). However the distant peaks corresponding to the same frequencies as in the TIE case can be seen.

Figure 4 presents the cycle-to-cycle jitter. The histogram in this case is a Gaussian and the standard deviation seems to be very small.

Figure 5 presents the cycle-to-cycle duty cycle jitter. The jitter values in this case are presented as pcms “milli-percentages”. The shape of the histogram is Gaussian implying little deterministic element in the jitter.

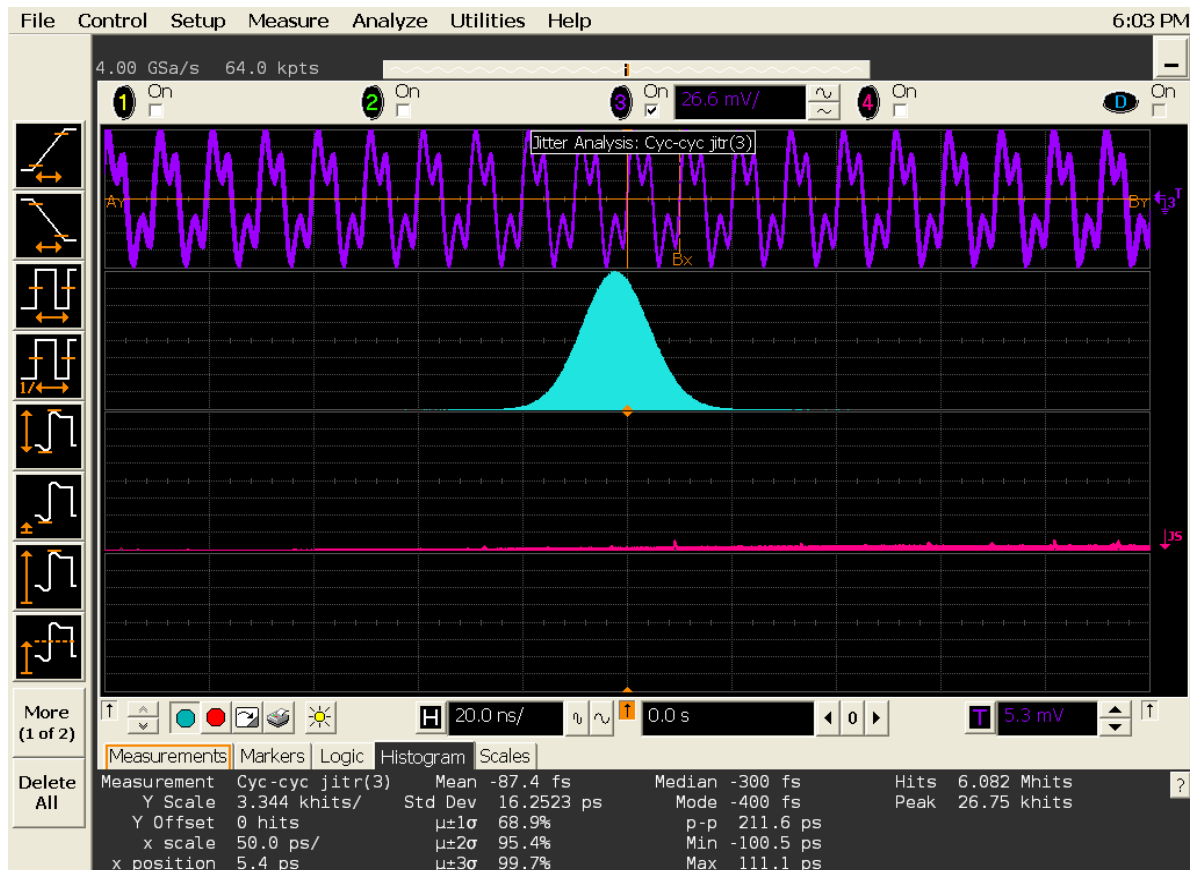


Figure 4: The cycle-to-cycle jitter display for the RTM with LTM4600EV DC-DC converter

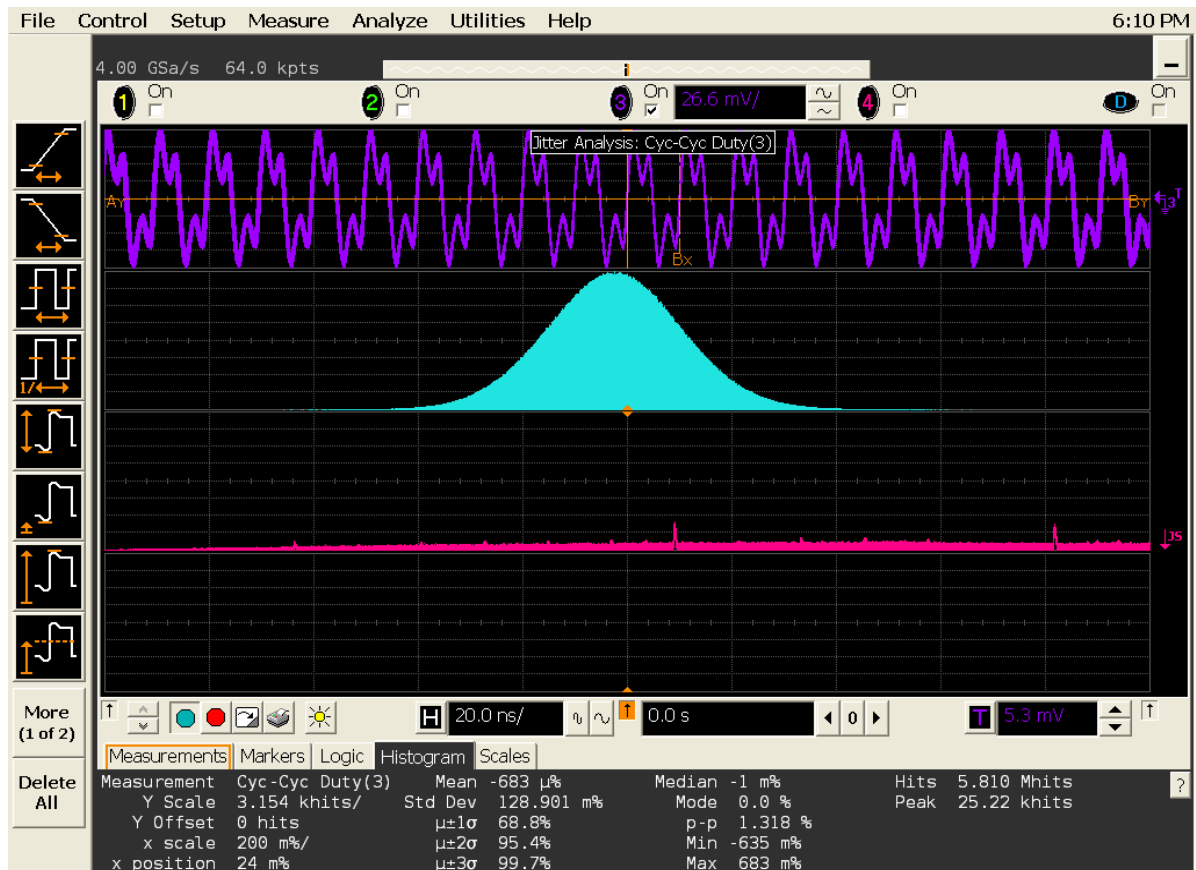


Figure 5: The cycle-to-cycle duty cycle display for the RTM with LTM4600EV DC-DC converter

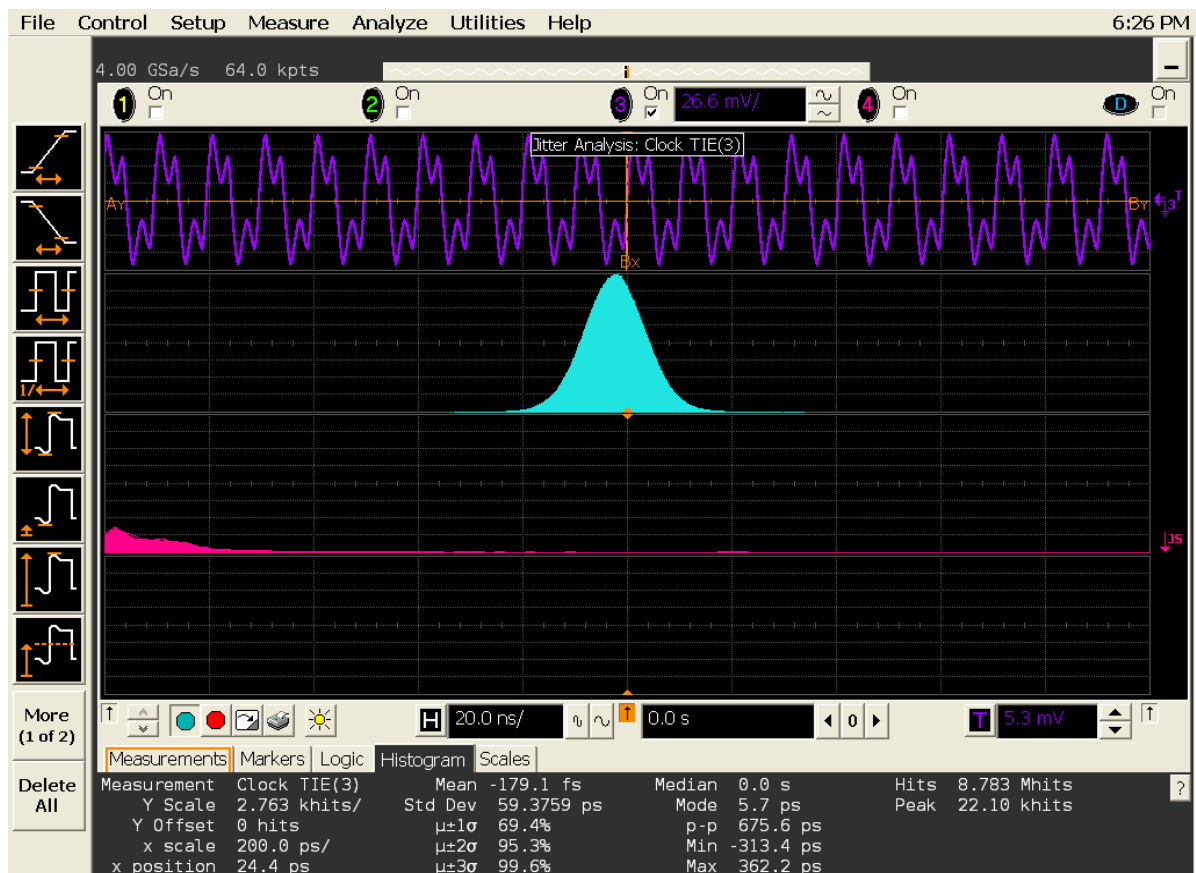


Figure 6: TIE display for the RTM (Card A) with an external power supply

2. RTM card with no on-board DC-DC converter: This experiment demonstrates the jitter performance of an RTM card, where the on board DC-DC converter is removed. From now on



we will call this card “Card A” and all the modifications to see the different experiment results are done to this board. In this particular case the 3.3V power to the board is supplied by an external DC power supply. As the results in [1] suggest, this represents the best jitter performance that can be achieved with the CC RTM. Therefore, we will use this result as a benchmark to compare the effects of the different modifications.

Figure 6 presents the TIE from which we can see that the histogram has a Gaussian shape. This implies that there is a minimal amount of deterministic jitter on the clock. The standard deviation is 59.4 ps which is in accordance with the result presented in [1] for the phase jitter. The jitter spectrum shows no discernible peak. Figure 7 shows the period jitter whose histogram has a Gaussian shape as well. The standard deviation is 9.6 ps which is also less than that of the case in the experiment 1.

Figure 8 and 9 show the results for the cycle-to-cycle and cycle-to-cycle duty cycle jitter measurements. The measurements show a better performance of these jitter metrics compared to the case in experiment 1, however the improvement does not seem to be too significant.

In the light of the observations so far, from now on only the performance results related to the TIE jitter measurement will be shown. We believe that this is the major jitter type that would cause concern for our application. Additionally, the period jitter seems to follow the same pattern as the TIE and the other jitter measurements have much higher percentage of random jitter to be affected by the changes in the power system topology.



Figure 7: The period jitter display for the RTM (Card A) with an external power supply



Figure 8: The cycle-to-cycle display for the RTM (Card A) with an external power supply

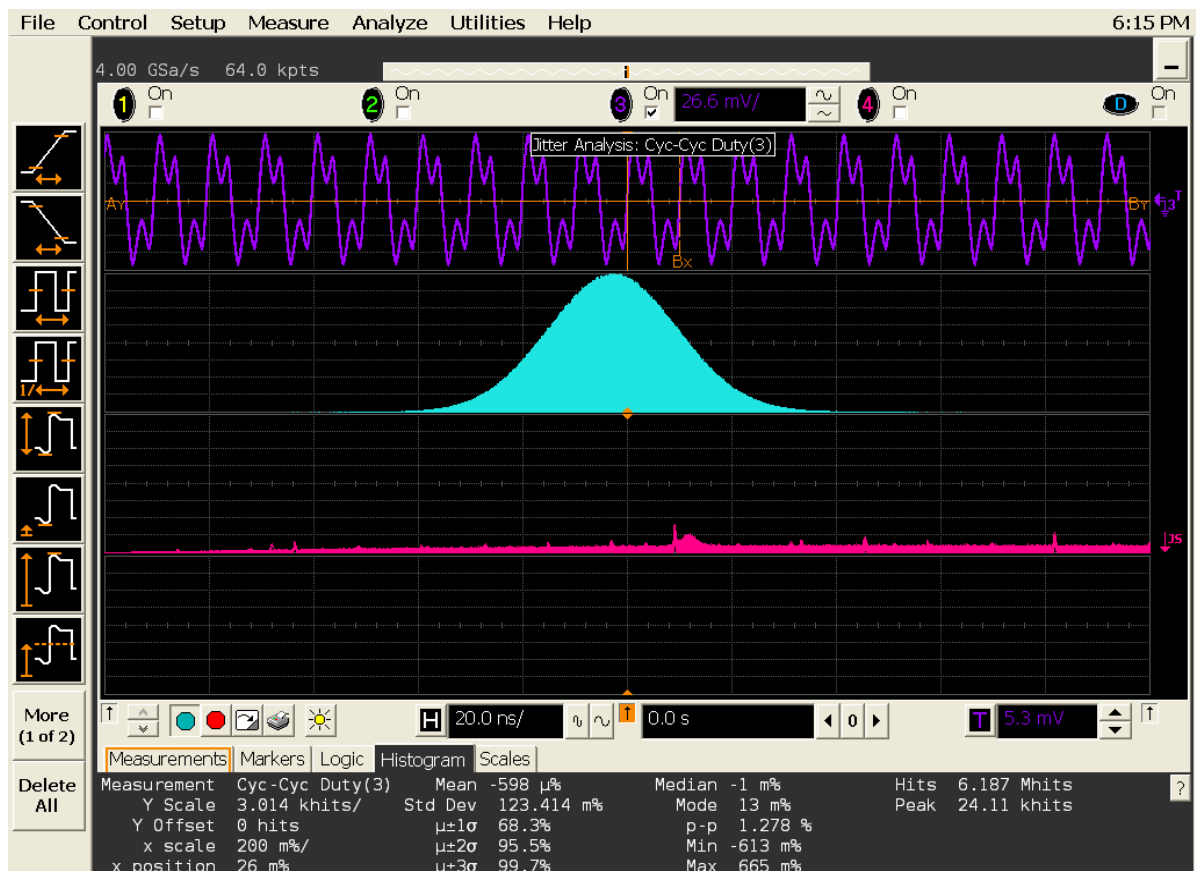


Figure 9: The cycle-to-cycle duty cycle display for the RTM (Card A) with an external power supply

- Card A with a different DC-DC converter: In this case we used a point-of-load style integrated DC-DC converter to power the 3.3 V rail. The chip, PTH12060, is mounted on a proto-board

cut-out with corresponding required circuitry (voltage set resistors, input/output capacitors) and attached to the CC RTM by short cables which on the input side connect to the 12 V input from the DAMC2 and on the output the 3.3 V rail of the CC RTM.

Figure 10 shows the TIE measurement results. From the histogram we see that the jitter is largely deterministic and the standard deviation is 305.6 ps which is also in accordance with [1]. The jitter spectrum shows a significant peak around 350 KHz which is the switching frequency for this DC-DC converter.

4. Card A with PTH12060 with a ferrite bead at the output: Making a modification to the circuitry in the experiment 3, a ferrite bead (Fair-rite 2773021447) is added to the output of the DC-DC converter in series with the connection to the CC RTM 3.3 V power rail. A 1  $\mu$ F ceramic capacitor is added in parallel.

Figure 11 shows the corresponding TIE measurement result.

5. Card A with PTH12060 with ferrites at both input and output: This case the same circuitry is added to the input 12 V as well and figure 11 shows the TIE measurement results.
6. Card A with PTH12060 with a 1 $\mu$ H & 1  $\mu$ F filter: For this experiment instead of the ferrite beads a 1 $\mu$ H choke is used in parallel with a 1  $\mu$ F capacitor as the filter to the power supply output. Figure 13 shows the TIE measurement from which we can see that the histogram has a Gaussian shape and the standard deviation value is close to the one in the measurement using the external power supply. The jitter spectrum also does not exhibit any major peaks.

Figure 14 shows the period jitter measurement in this case which has a Gaussian shape as well with a much reduced rms jitter (standard deviation).

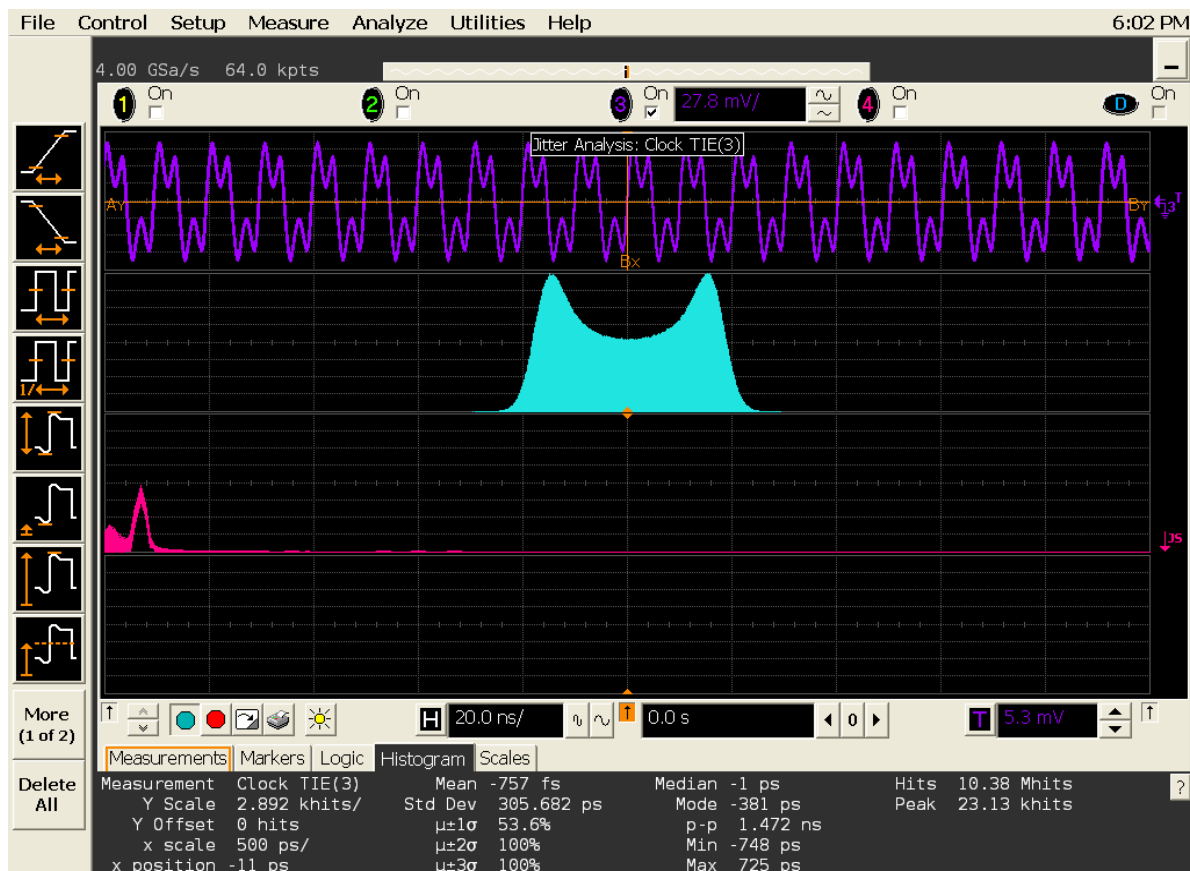


Figure 10: The TIE display for “Card A” with external PTH12060 DC-DC converter



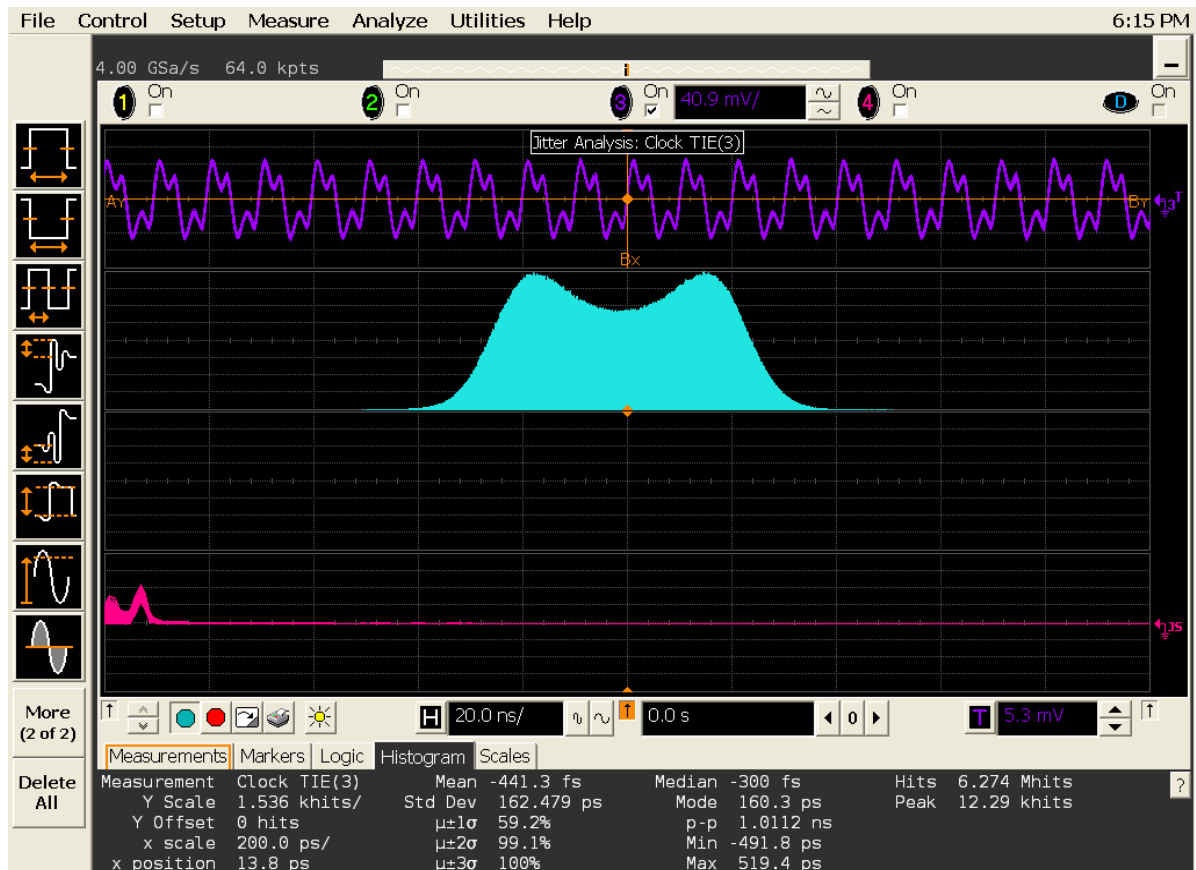


Figure 11: The TIE display for "Card A" with external PTH12060 DC-DC converter (ferrite bead at the output)

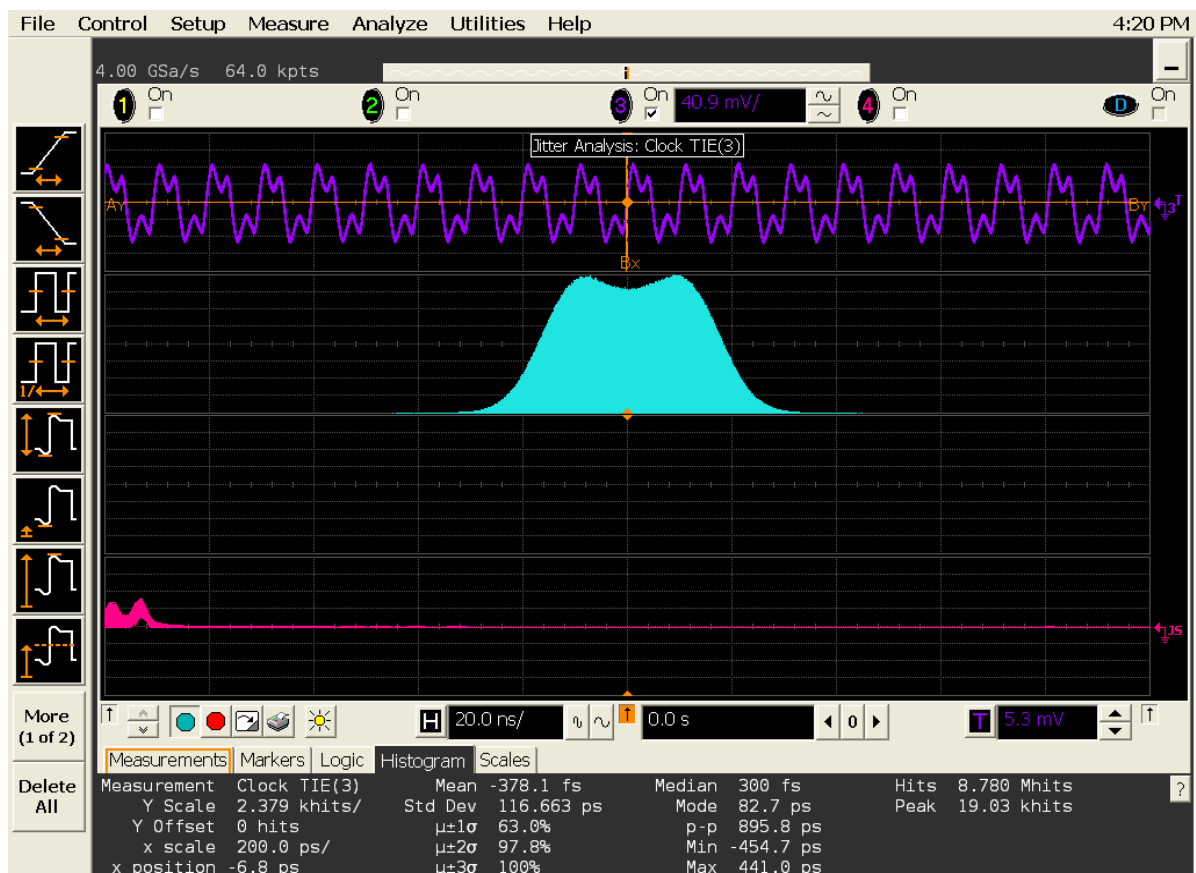


Figure 12: The TIE display for "Card A" with external PTH12060 DC-DC converter (ferrite beads at the output and the input)

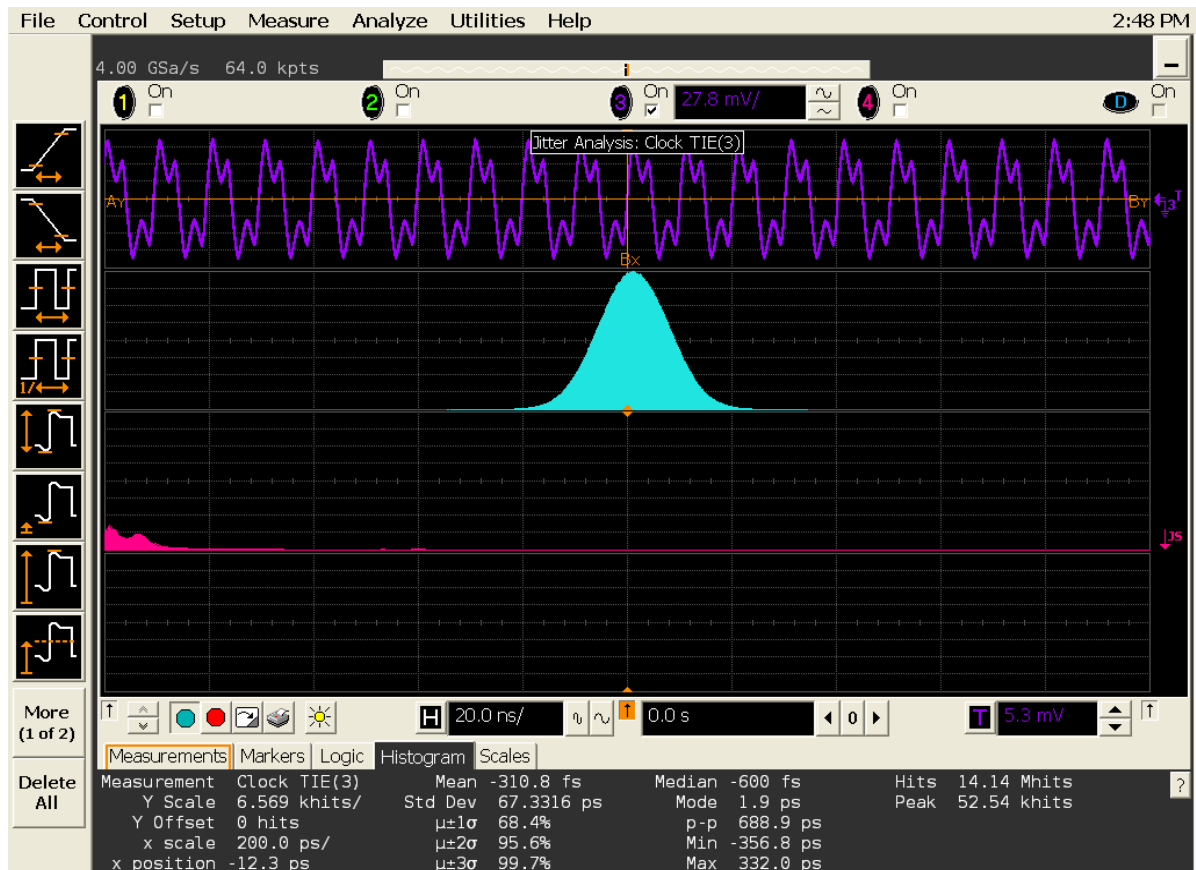


Figure 13: The TIE display for “Card A” with external PTH12060 DC-DC converter (1 uH/1 uF filter at the output)

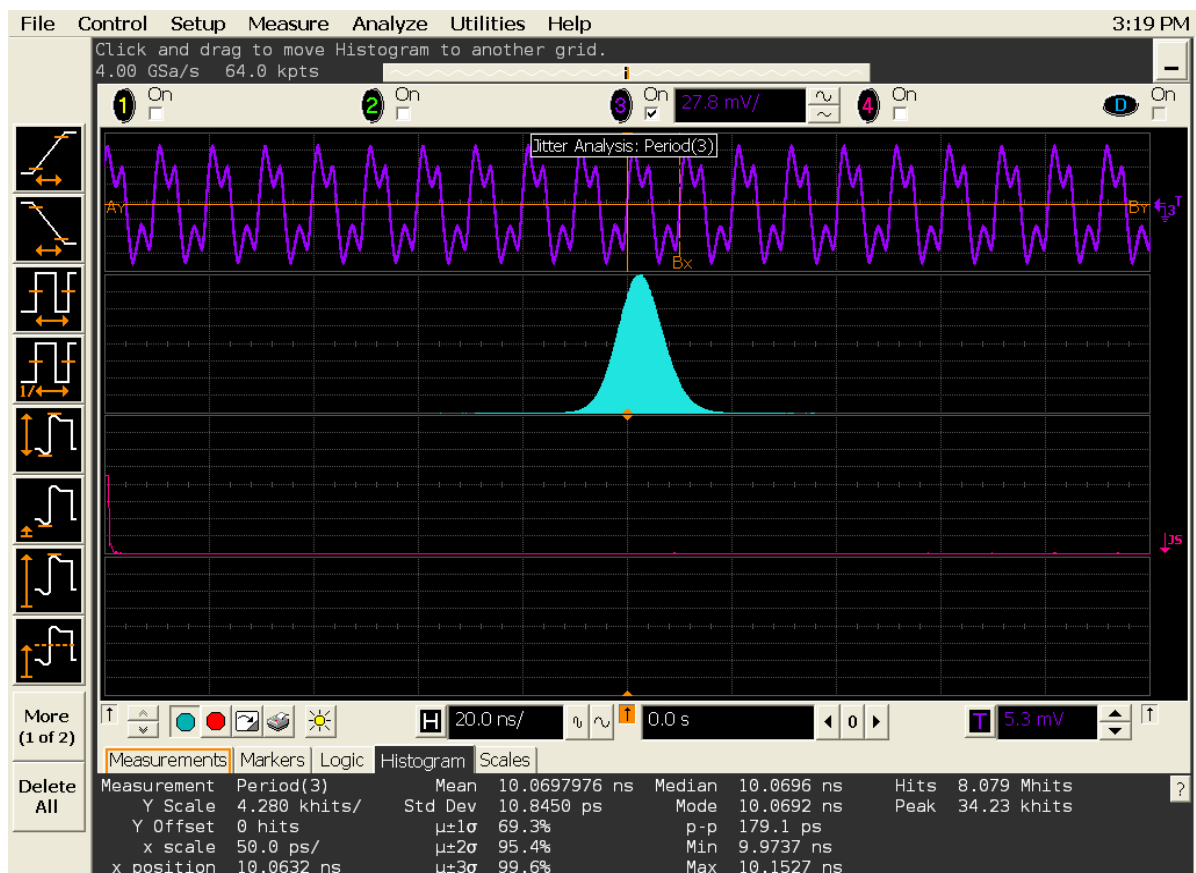


Figure 14: The period jitter display for “Card A” with external PTH12060 DC-DC converter (1 uH/1 uF filter at the output)

7. Card A with the LTM4600 mounted externally: In this experiment as in the case with the PTH12060, the LTM4600 and the corresponding circuitry are mounted on an external proto-board and attached to the CC RTM. Figure 15 shows the TIE measurement which shows a better jitter pattern than that of the PTH12060 which can be explained by having better noise characteristics than the PTH12060, the quality of the supporting resistors and the capacitors or even the circuit construction. Nevertheless, figures 16, 17 and 18 show much improved jitter characteristics, where figure 15 corresponds to using an output ferrite, figure 16 an output 1  $\mu\text{H}/1 \mu\text{F}$  filter and figure 17 having an input ferrite in addition to the output 1  $\mu\text{H}/1 \mu\text{F}$  filter.
8. Card A with the LTM4600 mounted on the board: In this case the LTM4600 and the corresponding circuitry are loosely mounted on the board (adding extra conducting layer to avoid soldering the LGA component on the board). The jitter results are similar to the case when LTM4600 is properly soldered on the board as shown in figure 19. In this case however we can add an output ferrite to the 3.3V rail for which case the results are shown in figure 20. (The case with the 1 $\mu\text{H}/1 \mu\text{F}$  filter couldn't be produced because of a pad damage to the LTM4600 chip used for tests.)



Figure 15: The TIE display for “Card A” with external LTM4600 DC-DC converter

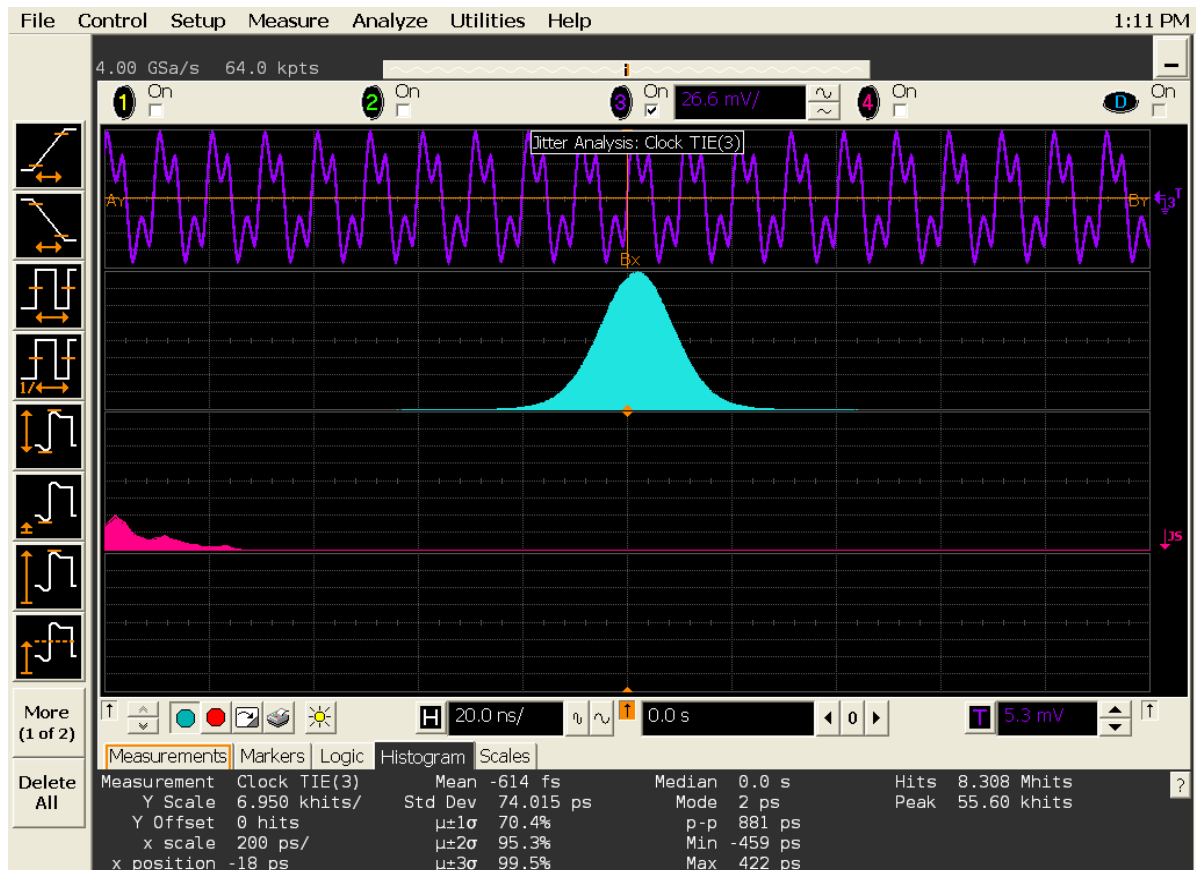


Figure 16: The TIE display for “Card A” with external LTM4600 DC-DC converter (ferrite bead at the output)



Figure 17: The TIE display for “Card A” with external LTM4600 DC-DC converter (1 uH/1 uF filter at the output)

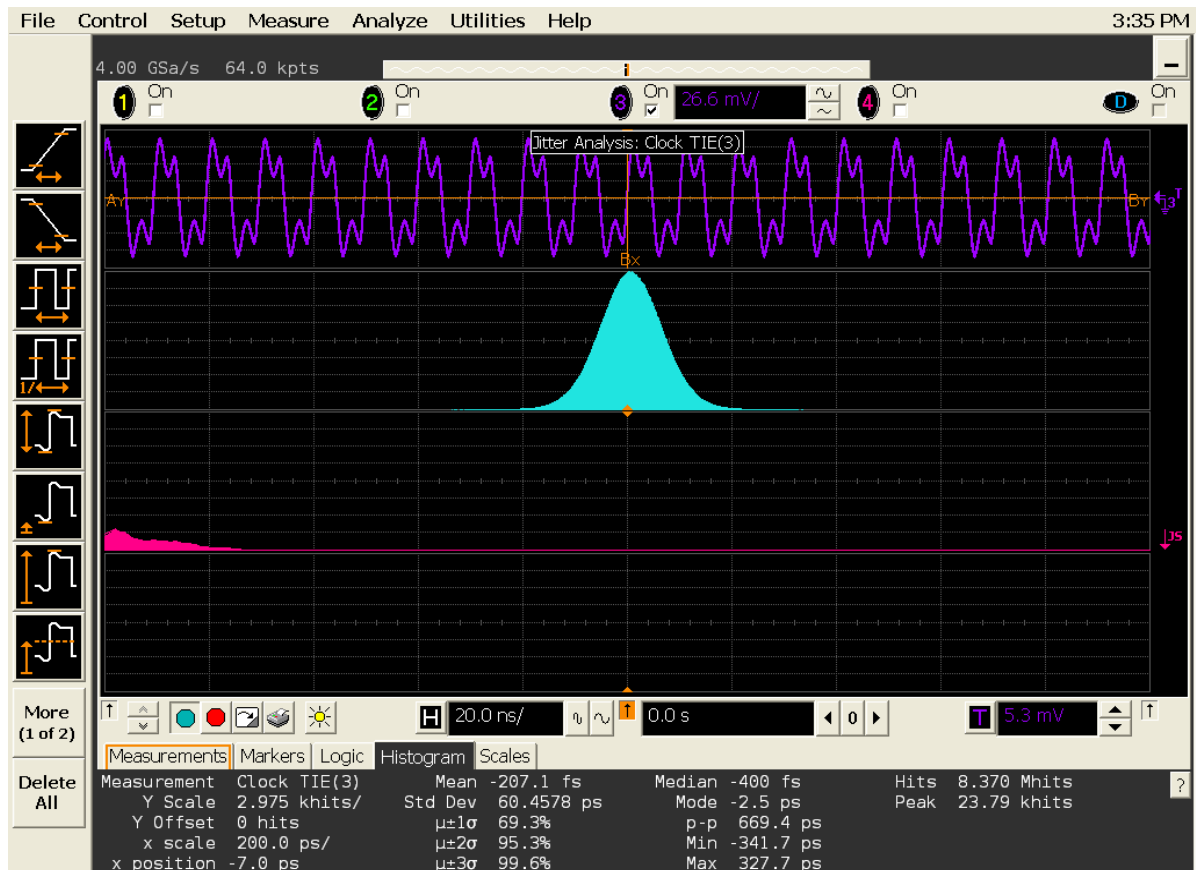


Figure 18: The TIE display for “Card A” with external LTM4600 DC-DC converter (1 uH/1 uF filter at the output, ferrite bead at the input)

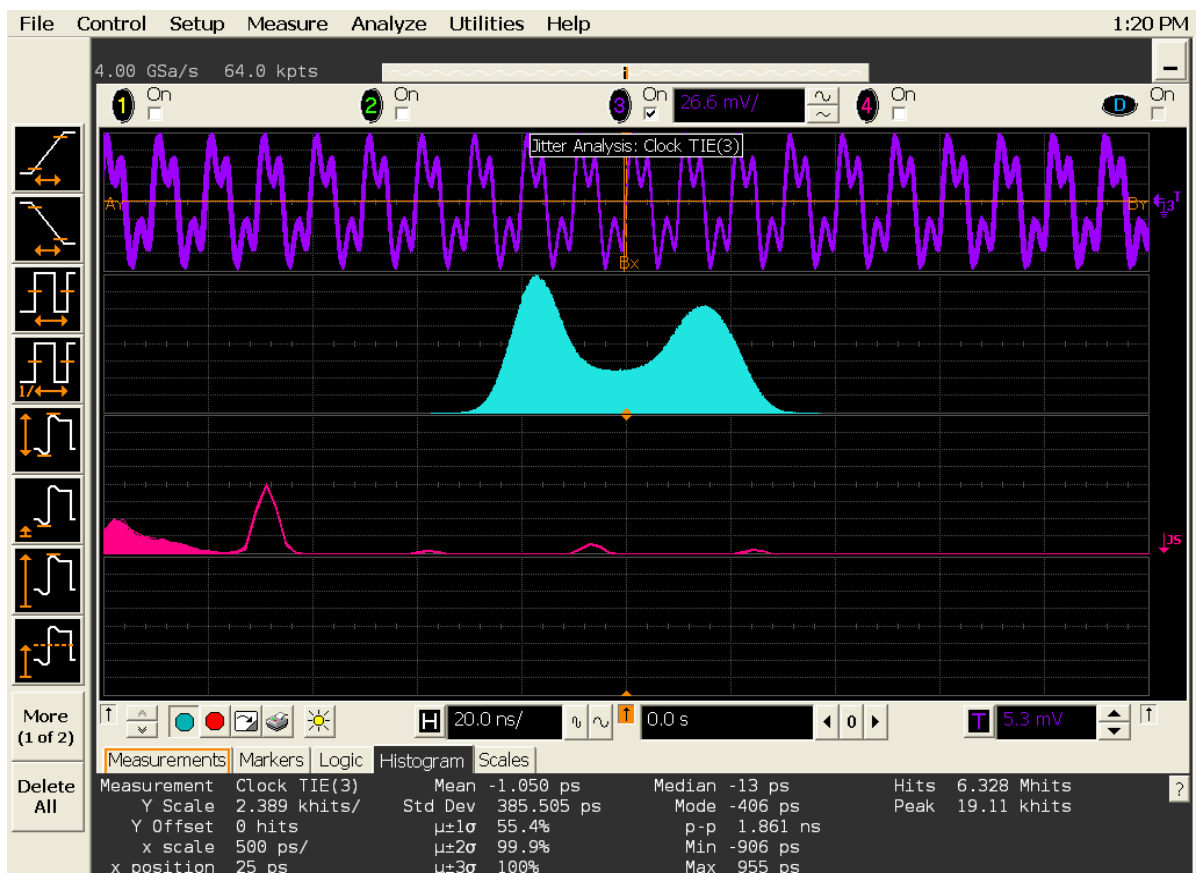


Figure 19: The TIE display for “Card A” with LTM4600 DC-DC converter mounted on the board



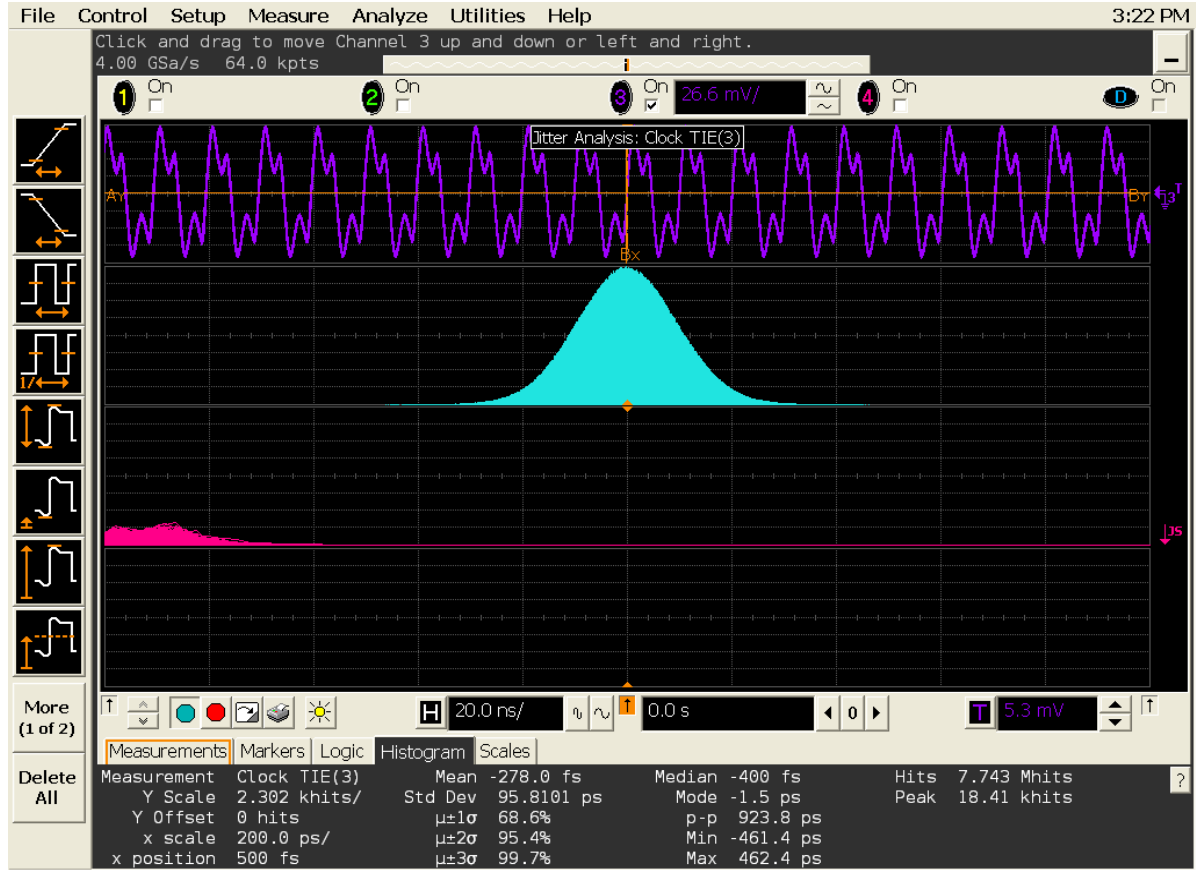


Figure 20: The TIE display for “Card A” with LTM4600 DC-DC converter mounted on the board (ferrite bead at the output)

## CONCLUSIONS

As mentioned in the previous experiment results and in [1], there is a jitter on the 99 MHz clock generated by the CC RTM. Furthermore, the most important type of jitter is the TIE (phase noise) which mainly results from the DC-DC converter switching noise. In order to reduce this jitter various power system topologies that include using another DC converter chip and power supply filtering at the input and output of the power system are investigated. Table 1 shows the measured p-p and rms TIE values for different board configurations.

Config. No.	CC RTM board configuration	TIE RMS	TIE p-p
1	RTM card with LTM4600EV (current config.)	426.83 ps	1901 ps
2	“Card A” with external power supply	59.38 ps	675.6 ps
3	“Card A” with ext. PTH12060	305.68 ps	1472 ps
4	“Card A” with ext. PTH12060 ferrite bead at the output	162.48 ps	1011 ps
5	“Card A” with ext. PTH12060 ferrite bead at the input and output	116.66 ps	895.8 ps
6	“Card A” with ext. PTH12060 1 uH/1 uF filter at the output	67.33 ps	688.9 ps
7	“Card A” with ext. LTM4600	132.87 ps	1255 ps
8	“Card A” with ext. LTM4600 ferrite bead at the output	74.02 ps	881 ps

9	“Card A” with ext. LTM4600 1 uH/1 uF filter at the output	61.15 ps	685.7 ps
10	“Card A” with ext. LTM4600 1 uH/1 uF filter at the output, ferrite bead at the input	60.46 ps	669.4 ps
11	“Card A” with LTM4600 mounted on-board	385.54 ps	1851 ps
12	“Card A” with LTM4600 mounted on board with ferrite bead at the output	95.81 ps	923.8 ps

Table 1: The measured p-p and RMS TIE corresponding to different CC RTM configurations

The result of these observations points to a need for filtering of the power supply at the output of the DC converter. Furthermore filtering at the input also seems to help the jitter results as well. The output filtering of the DC converter should ideally involve a choke inductor and a parallel capacitor (1 uH / 1 uF seem to give good results). Providing provision for adding extra ceramic capacitors to filter out the power supply noise also seem to be helpful. We aim to get a jitter value close to the best case (without an external power supply) which is the configuration 10 (~60 ps TIE rms) as a result of these modifications to the next RTM design iteration.

In addition to the power supply output filtering the power plane of the clocking circuitry on the CC RTM can also be separated and filtered by a ferrite bead. Obviously we have not been able to try out this configuration, however we believe this will contribute to improving the jitter performance further. The resulting layout topology can be seen in figure 21, where red rectangles represent the filters in ferrite bead/capacitor configuration for separating clock circuitry power plane and choke/capacitor power configuration for separating the main power plane from the DC-DC converter output power plane. The red rectangle at the input is a ferrite bead separating the 12V input trace from the 12V power plane on the board.

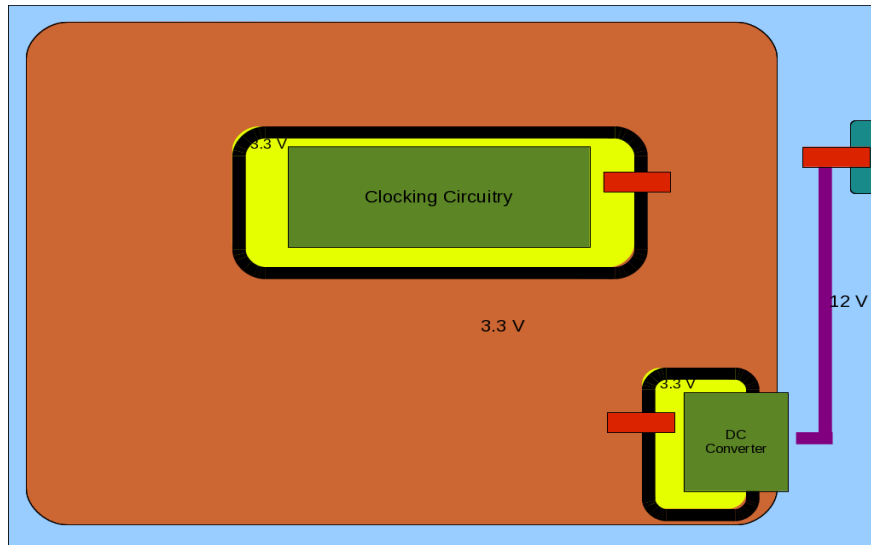


Figure 21: Proposed power layout for the next iteration of the CC RTM

## REFERENCES

- [1] T. Gerlach, P. Gessler, H. Kay, E. Motuk, V. Petrosyan, “Measurement Report: Phase noise and jitter at Clock and Control output”, 2011