

uRTM-DAMC2

Frequency Limit Test

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Outline

> Introduction

> Test Design

- Schematic
- DDR Data Generation
- Receiver Data Interface

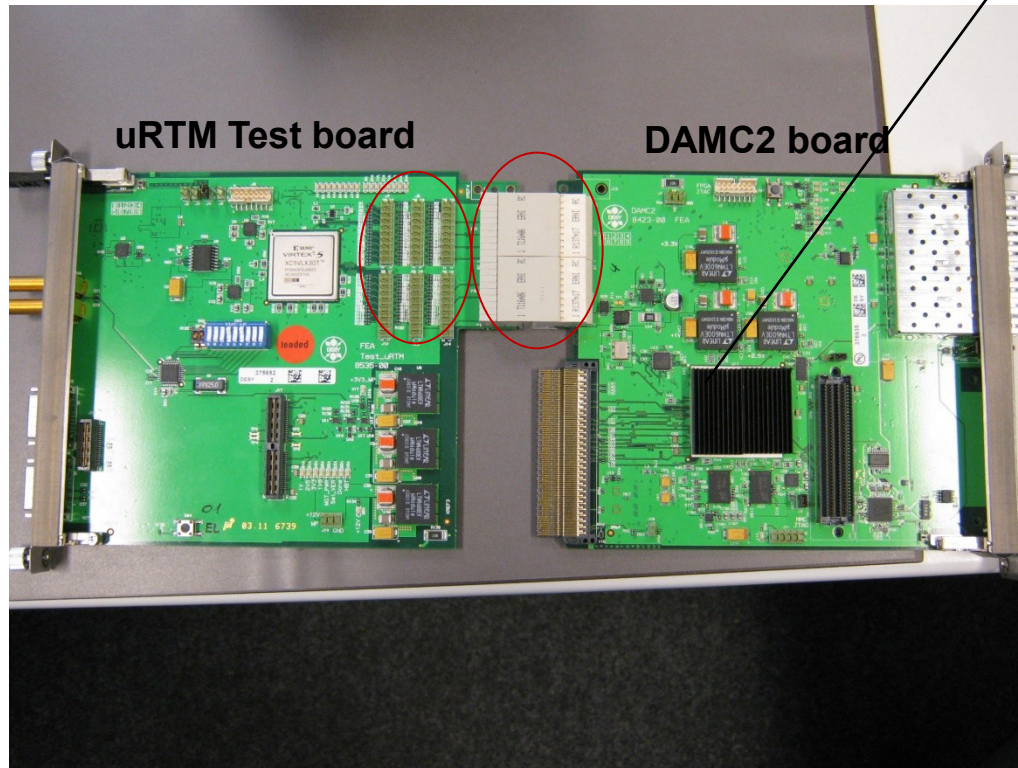
> Test Results



Introduction

> Hardware

Three I/O banks for uRTM-DAMC2 transmission

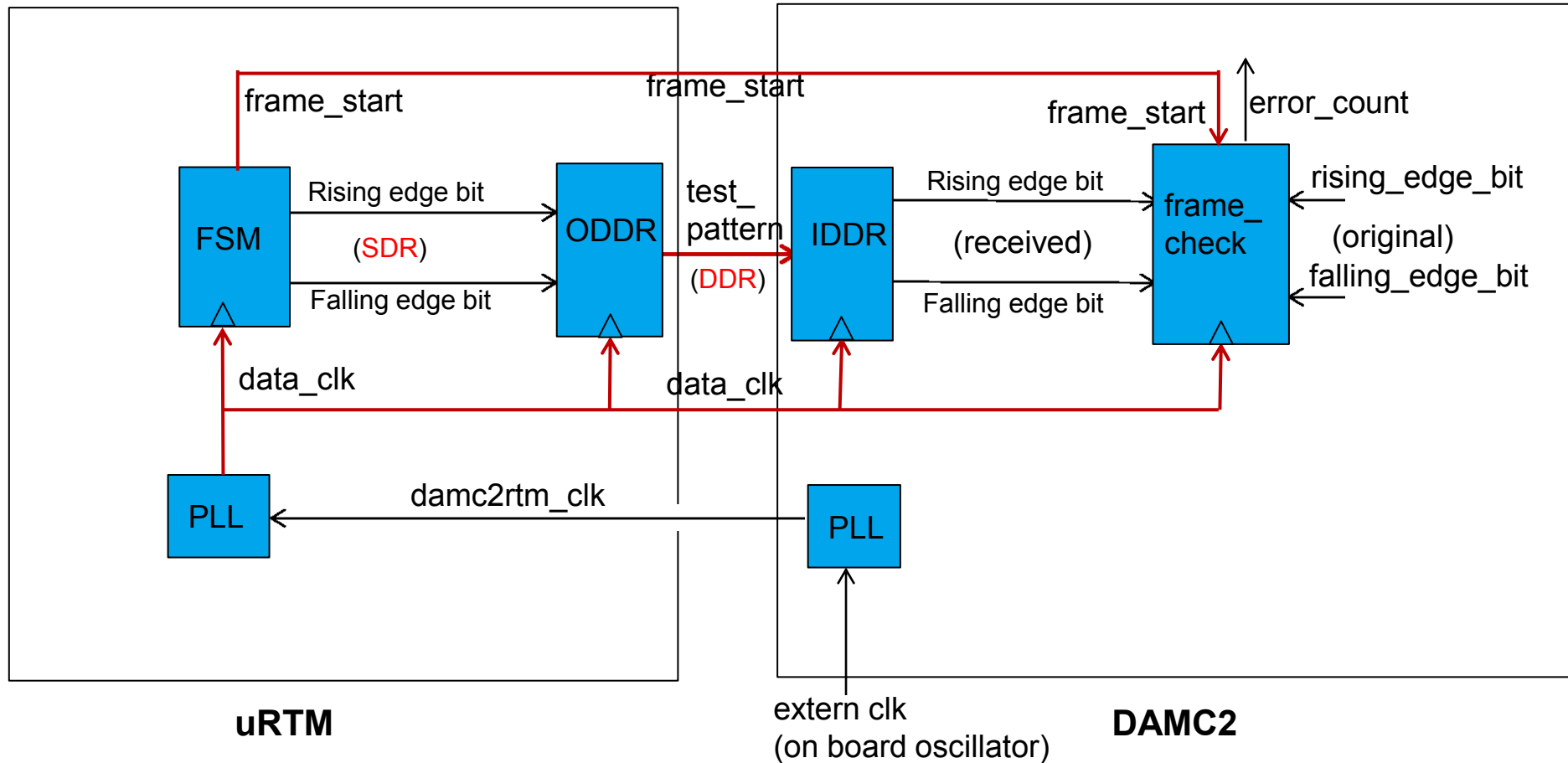


> Software Tool:

- Xilinx ISE 12.4
 - Mapping Properties → Optimization Strategy → Speed

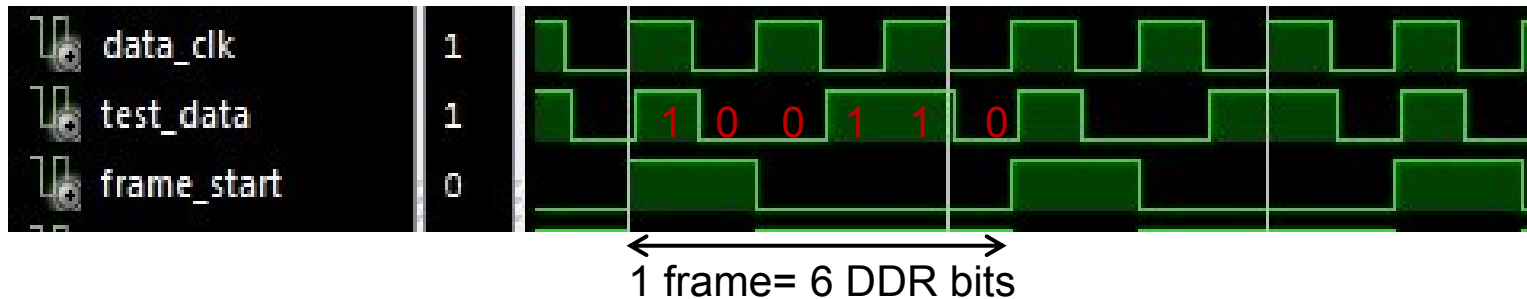
Test Design: Schematic

> All transferred signals use differential pair !!

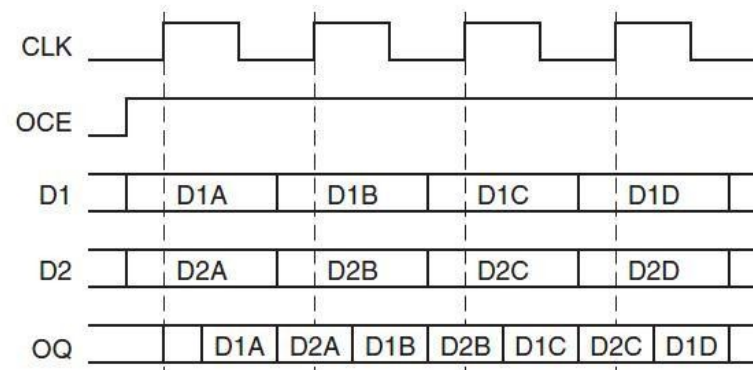
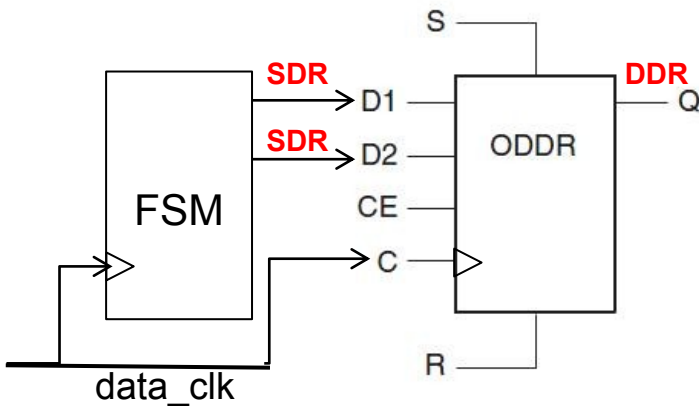


Test Design: DDR Data Generation

> DDR (***D**ouble **D**ata **R**ate*) data timing diagram

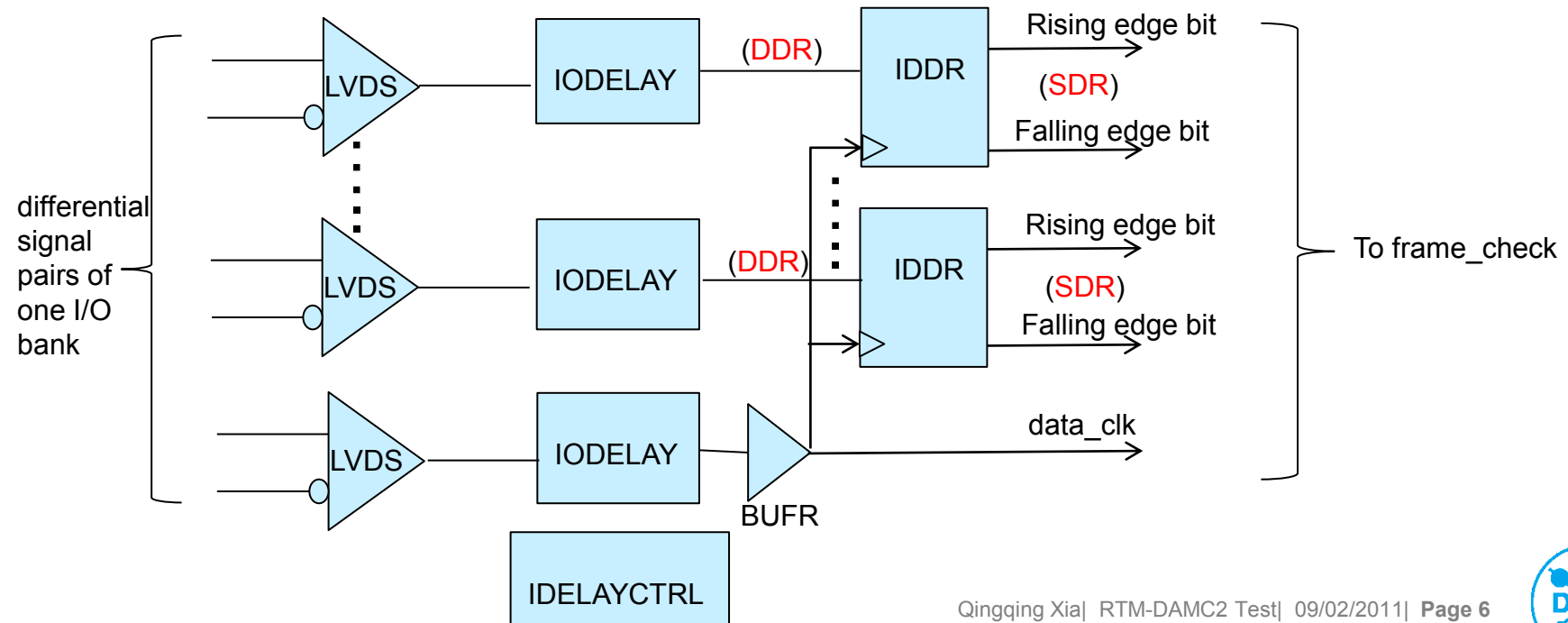


> Using ODDR Xilinx Primitive



Test Design: Receiver Data Interface

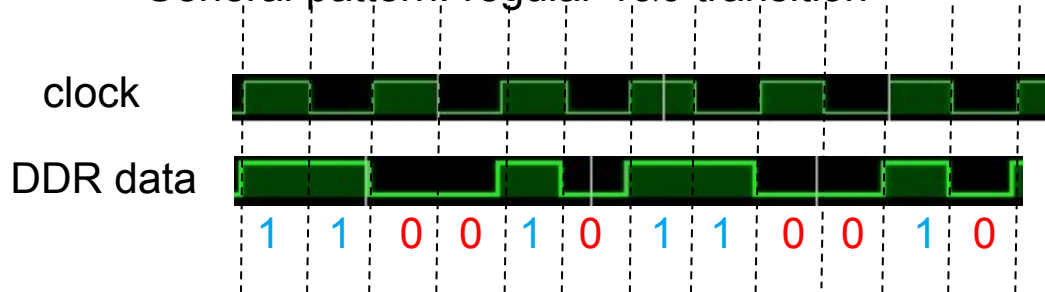
- Receiver Data Interface with Xilinx primitive IODELAY and IDDR
- IODELAY resolution = 1 tap ≈ 80 ps
- IODELAY: 0 to 63 taps (fixed or dynamic) \rightarrow max adjustable delay ≈ 5 ns
- IDELAYCTRL primitive must be instantiated. It continuously calibrates the individual IODELAY in its clock region



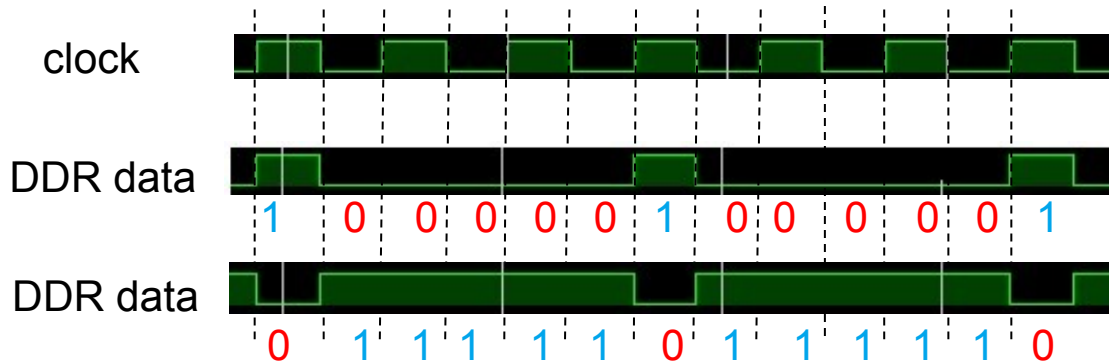
Test Results

> Test patterns for stability test (1 frame=6 data bits)

- General pattern: regular 1&0 transition



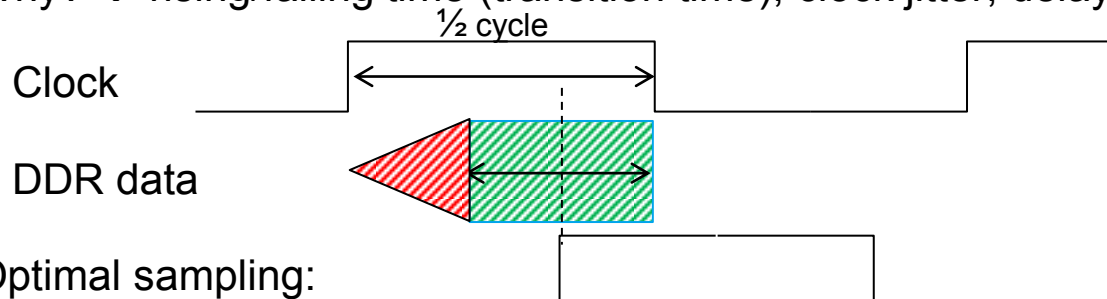
- Critical test pattern: Long-term DC-balance problem



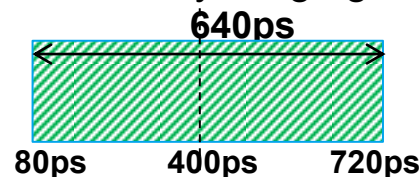
Test Results

> Single I/O Bank (16 parallel DDR data channels)

- Up to 450MHz clock (900Mbit/s per DDR data channel): **no** input delay is required for error-free transmission
- 500MHz clock (1Gbit/s per DDR data channel) : input delay is required
 - Input delay → optimal clock samples at center of the stable area of the data
 - Why? → rising/falling time (transition time), clock jitter, delay within FPGA ...



- Optimal sampling:
- 500MHz → $\frac{1}{2}$ cycle = 1ns. A delay ranging from 80ps to 720ps works for error-free



- Optimal delay for 500MHz: $(720\text{ps} - 80\text{ps}) / 2 + 80\text{ps} = 400\text{ps} = 5$ Taps



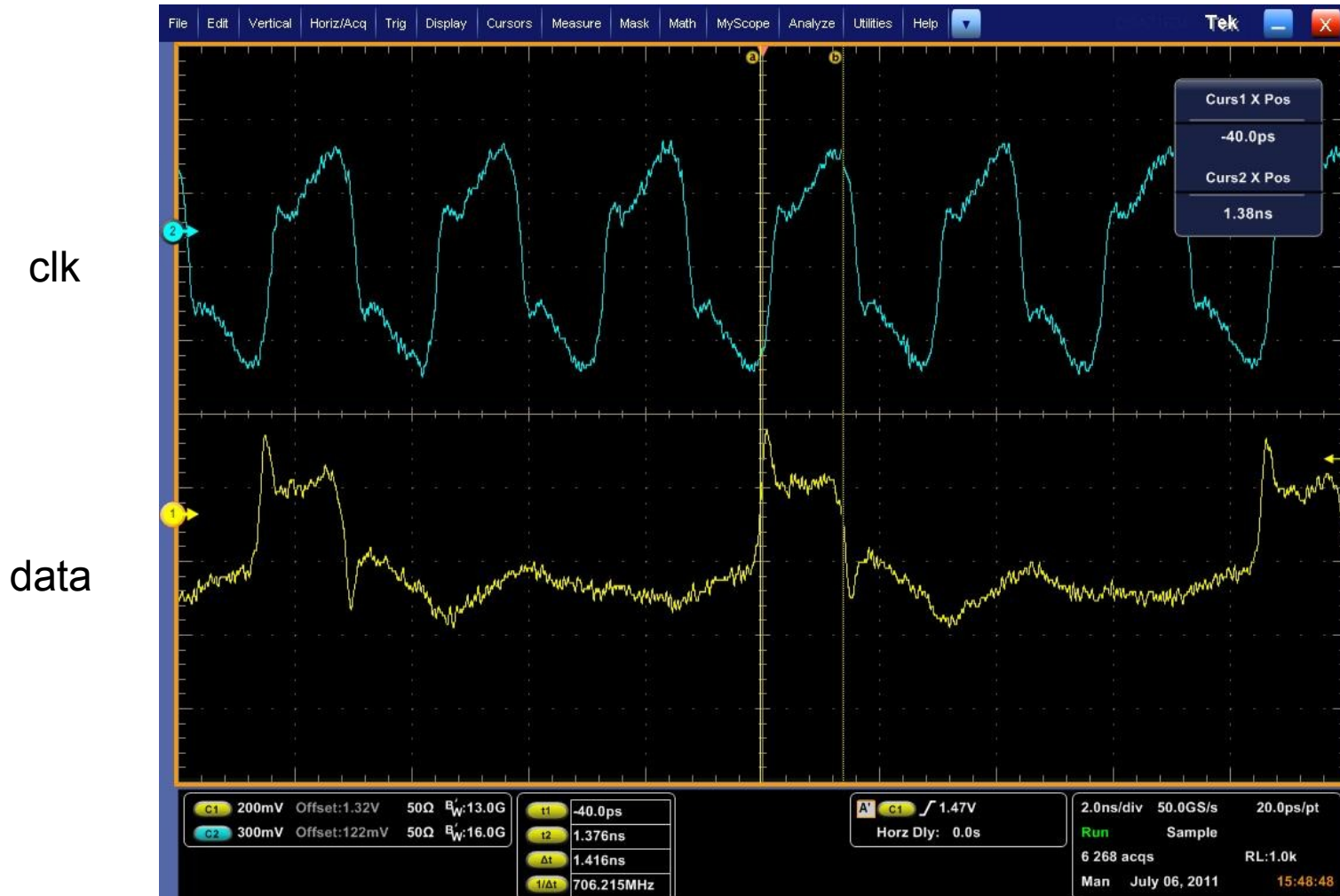
Test Results

- > Three I/O Banks parallel with separated data_clk and frame_start signal
 - The speed optimization for Mapping in ISE !!
- > In some cases you need individual data bit delay adjustment:
 - Significant wiring length difference of data transmission lines? Both of our test boards are optimal routed PCBs in term of wiring length .
 - FFs for capturing incoming DDR data bits have optimal distance to I/O Pad? Using IDDR is optimal in terms of this aspect, otherwise area constraint for FFs might be needed, in order to get a optimal mapping.
 - Signal integrity problem(cross-talk between data lines, ..)
 - ...
- > Limit of FPGA device ! (e.g.: PLL Primitive $f_{out,max} = 600\text{MHz}$ for Virtex5 Device with speed grade -1)



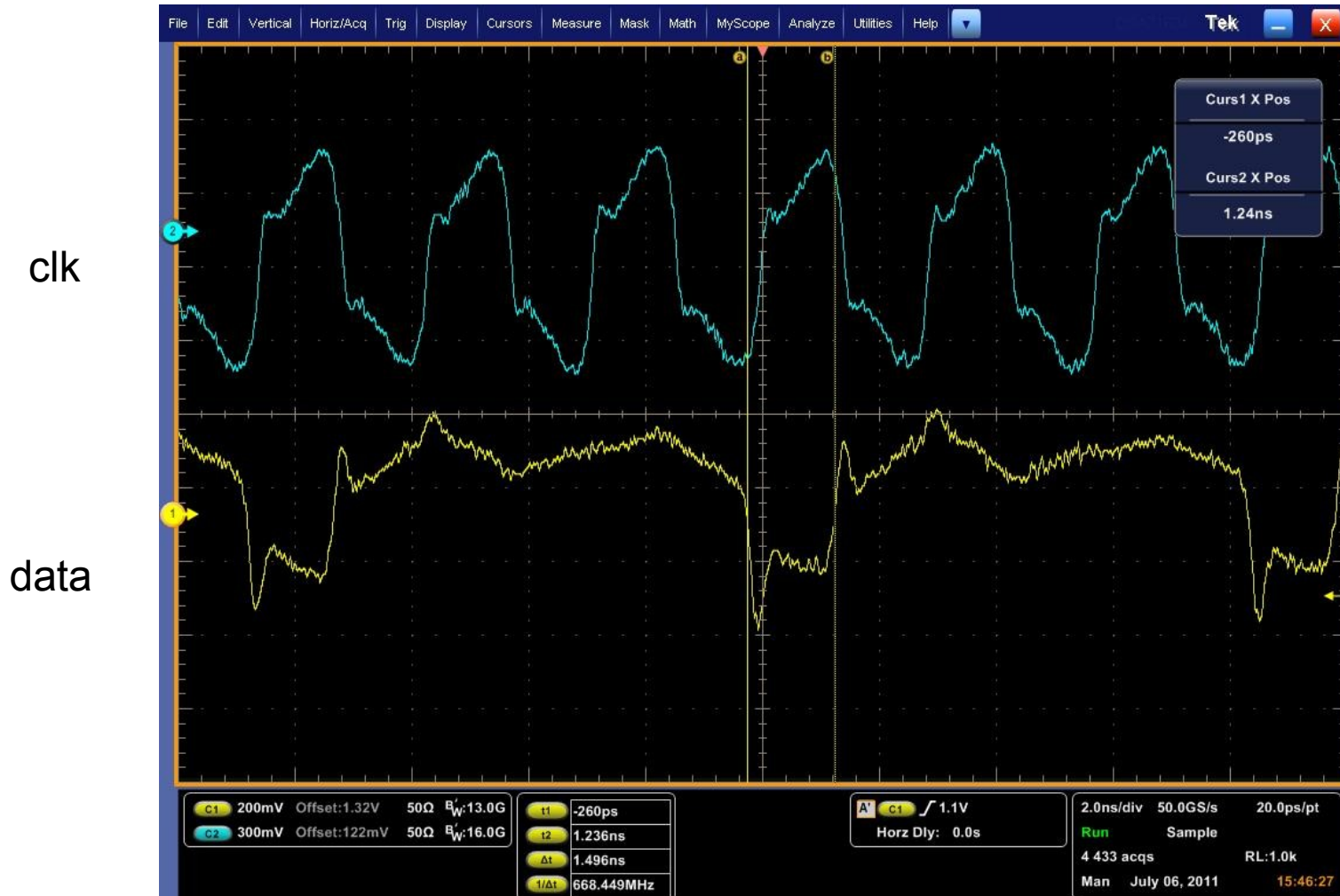
Test Results

➤ Screenshots from oscilloscope: 000001, 350MHz(clk), DDR



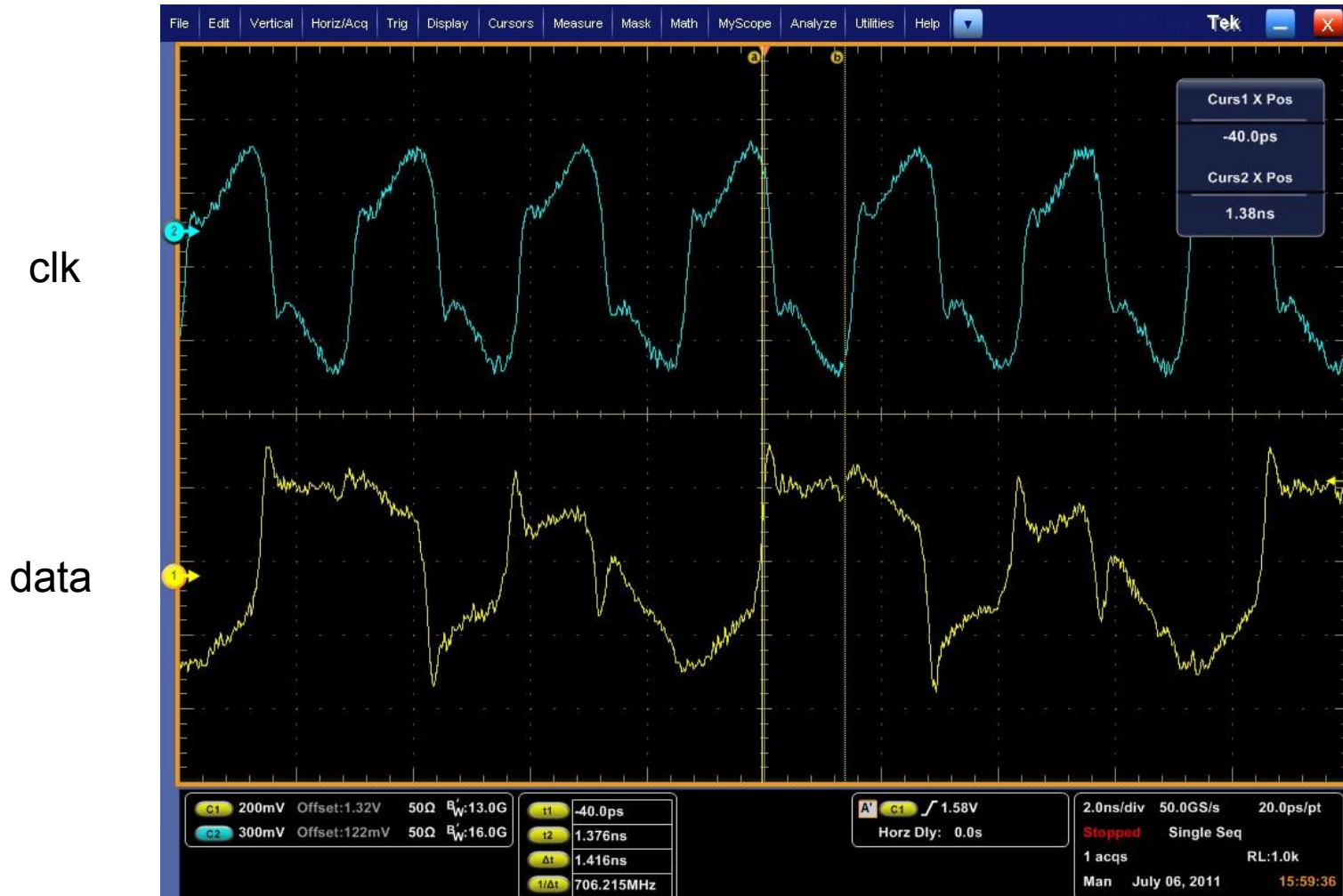
Test Results

- Screenshots from oscilloscope: 111110, 350MHz(clk), DDR



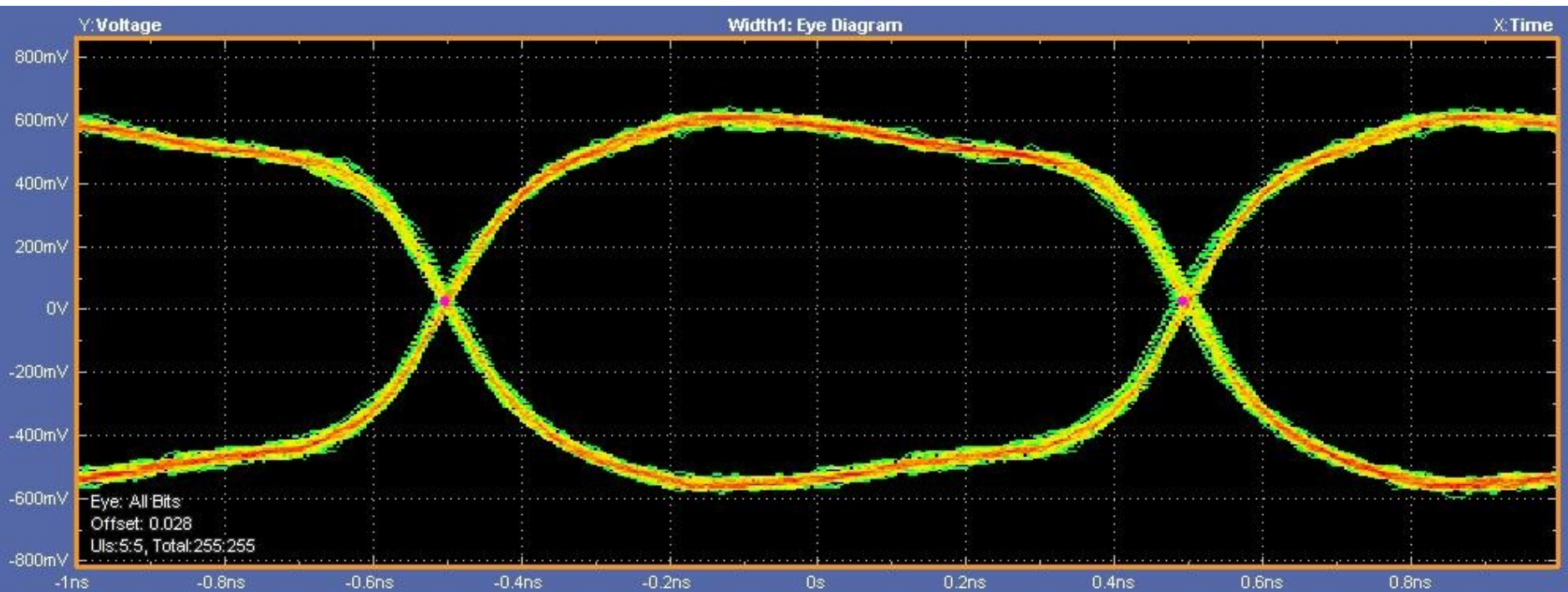
Test Results

- Screenshots from oscilloscope: 001101, 350MHz(clk), DDR



Test Results

- Screenshots from oscilloscope: 500M(clk) eye diagram



References

- (1) *Virtex-5 FPGA User Guide*
- (2) *Virtex-5 FPGA Data Sheet: DC and Switching Characteristics*
- (3) *LVDS Owner's Manual, Fourth Edition*
- (4) *Hardware Design Description (HDD) of the Double Advanced Mezzanine Card*
- (5) *Schematic Sheet of Double Advanced Mezzanine Card*
- (6) *Hardware Design Description (HDD) of the μ RTM Test Board*
- (7) *Schematic Sheet of μ RTM Test Board*
- (8) *AD9252 Data Sheet, Analog Devices*
- (9) *Xilinx® Constraints Guide*
- (10) *Xilinx MIG HDL Example*



Thanks!

